P10®

Reference Guide Volume IV - Physical Features

DRAFT

PROPRIETARY AND CONFIDENTIAL INFORMATION

3Dlabs®

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Issue 1

Proprietary Notice

Email: info@3dlabs.com
Web: http://www.3dlabs.com

3D*labs* Ltd.
Meadlake Place
Thorpe Lea Road, Egham
Surrey, TW20 8HE
United Kingdom
Tel: +44 (0) 1784 470555
Fax: +44 (0) 1784 470699

3D*labs* K.K.
Shiroyama JT Mori Bldg 16F
40301 Toranomon
Minato-ku, Tokyo, 105, Japan
Tel: +81-3-5403-4653
Fax: +91-3-5403-4646

3D*labs* Inc.
480 Potrero Avenue
Sunnyvale, CA 94086,
United States
Tel: +1 (408) 530-4700
Fax: +1 (408) 530-4701

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User Note

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Package Diagrams

P10 is an 820-ball thermally-enhanced HSBGA package:

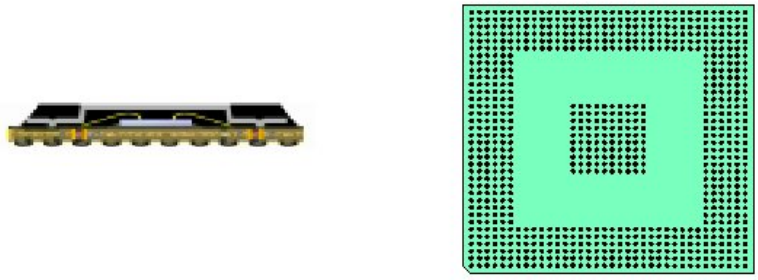

Figure 7-1 Cross-section and ball pattern of 820L HSBGA

Description	Dimension
Package Size	37.5 x 37.5 mm
Chip Size	14.28 x 14.28
Type	HSBGA
Body Height	2.23 mm
Substrate thickness	0.56 mm
Ball pitch	1.00 mm
Ball pad opening	0.6 mm

Table 7-1 Package dimensions and characteristics

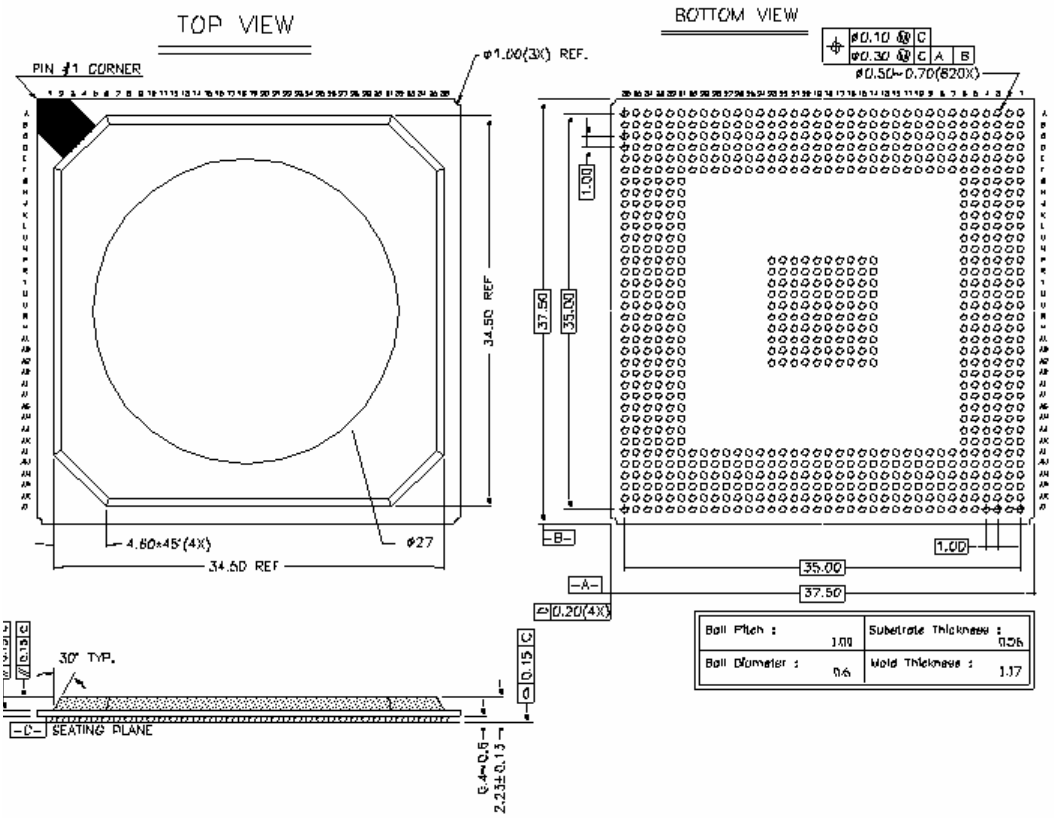

Figure 7-1 Package Diagram Views

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Pin Assignment

8.1 Pinlist by Number

The table below provides a brief description of each pin. It is organized alphabetically by pin number.

All pins are listed here. For specifics of pin electrical characteristics refer to chapter 10, Electrical Characteristics.

The pin type definitions used are:

I/O: Input Signal (tolerates 2.5 and 3.3 VDC PCI and AGP4X standards)
GND: Ground
PWR: Various power feed types
BIDIR: Bidirectional signals

BGA PAD	PIN NAME	TYPE	DESCRIPTION
A 1	MAData[74]		
A 2	MAData[73]		
A 3	MADqs[9]		
A 4	MAClk		
A 5	MAClkN		
A 6	MAAddr[5]		Memory Address signal
A 7	VCC2V5_1	PWR	
A 8	MAAddr[3]		Memory Address signal
A 9	MAAddrC[0]		
A10	MAAddrC[2]		
A11	MAAddr[6]		Memory Address signal
A12	MAAddr[7]		Memory Address signal
A13	MAAddrB[1]	BIDIR	Memory B Address signal
A14	GND_1	PWR	Core and IO ground supply = 0v
A15	MAAddr[1]		Memory Address signal
A16	MAAddr[0]		Memory Address signal
A17	MABa[0]		
A18	MACasN		
A19	MAData[35]		
A20	MADqs[3]		
A21	MAData[26]		
A22	MADqs[2]		
A23	GND_2	PWR	Core and IO ground supply = 0v
A24	MADqs[1]		
A25	VCC2V5_2	PWR	
A26	MADqs[0]		
A27	MAData[1]		
A28	MBDqs[0]		
A29	VCC2V5_3	PWR	
A30	MBDqs[1]		
A31	MBVref[0]		
A32	MBDqs[2]		
A33	MBData[21]		
A34	MBDqs[3]		
A35	MBData[25]		

BGA PAD	PIN NAME	TYPE	DESCRIPTION
A36	VCC2V5_4	PWR	
AA 1	VCC_DFP_3	PWR	3.30 vdc nominal
AA 2	GND_36	PWR	Core and IO ground supply = 0v
AA 3	DfpData[12]		
AA 4	DfpData[13]		
AA 5	DfpData[14]		
AA 6	DfpData[15]		
AA31	MBData[91]		
AA32	MBData[90]		
AA33	MBData[89]		
AA34	MBData[88]		
AA35	MBAddrC[2]		
AA36	MBAddrC[1]		
AB 1	DfpVref[1]		
AB 2	DfpBStrobe		
AB 3	DfpData[16]		
AB 4	DfpData[17]		
AB 5	DfpData[18]		
AB 6	VCC_DFP_4	PWR	3.30 vdc nominal
AB31	MBData[94]		
AB32	MBData[93]		
AB33	GND_37	PWR	Core and IO ground supply = 0v
AB34	MBData[92]		
AB35	MBAddrC[0]		
AB36	MBAddr[2]		
AC 1	DfpData[19]		
AC 2	DfpData[20]		
AC 3	DfpData[21]		
AC 4	DfpData[22]		
AC 5	DfpData[23]		
AC 6	DfpBBlank		
AC31	VCC1V2_21	PWR	3.30vdc nominal
AC32	MBData[96]		
AC33	MBData[95]		
AC34	MBDqs[11]		
AC35	MBAddr[3]		
AC36	MBAddr[4]		
AD 1	DfpBHSync		
AD 2	DfpBVSync		
AD 3	VCC_DFP_5	PWR	3.30 vdc nominal
AD 4	GND_38	PWR	Core and IO ground supply = 0v
AD 5	GND_39	PWR	Core and IO ground supply = 0v
AD 6	VCC1V2_20	PWR	1.20 vdc nominal
AD31	MBData[99]		
AD32	MBData[98]		
AD33	GND_40	PWR	Core and IO ground supply = 0v
AD34	MBData[97]		
AD35	MBAddr[5]		
AD36	MBCke		
AE 1	VDD_TTL_1	PWR	3.30 vdc nominal
AE 2	GND_41	PWR	Core and IO ground supply = 0v
AE 3	GND_42	PWR	Core and IO ground supply = 0v
AE 4	GND_43	PWR	Core and IO ground supply = 0v
AE 5	VDD_TTL_2	PWR	3.30 vdc nominal

BGA PAD	PIN NAME	TYPE	DESCRIPTION
AE 6	GND_44	PWR	Core and IO ground supply = 0v
AE31	VCC1V2_23	PWR	1.20 vdc nominal
AE32	MBData[101]		
AE33	GND_45	PWR	Core and IO ground supply = 0v
AE34	MBData[100]		
AE35	MBClkN		
AE36	MBClk		
AF 1	DacBBlue		
AF 2	DacBAG[2]		
AF 3	DacBFSAdj		
AF 4	GND_46	PWR	Core and IO ground supply = 0v
AF 5	DacBAG[3]		
AF 6	VCC1V2_22	PWR	1.20 vdc nominal
AF31	VCC2V5_23	PWR	3.30 vdc nominal
AF32	MBData[104]		
AF33	MBData[103]		
AF34	MBData[102]		
AF35	GND_47	PWR	Core and IO ground supply = 0v
AF36	MBDqs[12]		
AG 1	DacBGreen		
AG 2	DacBVAA[0]		
AG 3	DacBVref		
AG 4	DacBVAA[1]		
AG 5	DacBComp		
AG 6	DacBVAA[2]		
AG31	GND_48	PWR	Core and IO ground supply = 0v
AG32	GND_49	PWR	Core and IO ground supply = 0v
AG33	MBData[106]		
AG34	MBData[105]		
AG35	GND_50	PWR	Core and IO ground supply = 0v
AG36	VCC2V5_24	PWR	
AH 1	DacBRed		
AH 2	GND_51	PWR	Core and IO ground supply = 0v
AH 3	DacBAG[1]		
AH 4	GND_52	PWR	Core and IO ground supply = 0v
AH 5	GND_53	PWR	Core and IO ground supply = 0v
AH 6	VCC1V2_24	PWR	1.20 vdc nominal
AH31	VCC1V2_25	PWR	1.20 vdc nominal
AH32	MBData[110]		
AH33	MBData[109]		
AH34	MBData[108]		
AH35	MBData[107]		
AH36	MBDqs[13]		
AJ 1	VDD_TTL_3	PWR	3.30 vdc nominal
AJ 2	GND_54	PWR	Core and IO ground supply = 0v
AJ 3	GND_55	PWR	Core and IO ground supply = 0v
AJ 4	DacBAG[0]		
AJ 5	VDD_TTL_4	PWR	3.30 vdc nominal
AJ 6	VCC1V2_26	PWR	1.20 vdc nominal
AJ31	VCC1V2_27	PWR	1.20 vdc nominal
AJ32	MBData[113]		
AJ33	MBData[112]		
AJ34	MBData[111]		
AJ35	GND_56	PWR	Core and IO ground supply = 0v

BGA PAD	PIN NAME	TYPE	DESCRIPTION
AJ36	VCC2V5_25	PWR	
AK 1	DacAVAA[2]		
AK 2	DacABlue		
AK 3	DacAAG[2]		
AK 4	DacAFSAdj		
AK 5	DacAAG[3]		
AK 6	VCC1V2_28	PWR	1.20 vdc nominal
AK31	VCC1V2_29	PWR	1.20 vdc nominal
AK32	MBData[115]		
AK33	MBData[114]		
AK34	GND_57	PWR	Core and IO ground supply = 0v
AK35	GND_58	PWR	Core and IO ground supply = 0v
AK36	MBDqs[14]		
AL 1	DacAGreen		
AL 2	DacAVAA[0]		
AL 3	DacAVref		
AL 4	DacAVAA[1]		
AL 5	DacAComp		
AL 6	VCC1V2_30	PWR	1.20 vdc nominal
AL 7	VCC1V2_31	PWR	1.20 vdc nominal
AL 8	VCC1V2_32	PWR	1.20 vdc nominal
AL 9	VCC1V2_33	PWR	1.20 vdc nominal
AL10	GND_59	PWR	Core and IO ground supply = 0v
AL11	ExtIntr		
AL12	SBData	BIDIR	
AL13	SBClk	BIDIR	
AL14	TestMode	IN	Production test global enable (Active high)
AL15	TestSelect[2]	IN	Production test mode select
AL16	VCC1V2_34	PWR	1.20 vdc nominal
AL17	SENSEVCC1V2		
AL18	GND_60	PWR	Core and IO ground supply = 0v
AL19	GND_61	PWR	Core and IO ground supply = 0v
AL20	SENSEGND		
AL21	VCC1V2_35	PWR	1.20 vdc nominal
AL22	GND_62	PWR	Core and IO ground supply = 0v
AL23	GND_63	PWR	Core and IO ground supply = 0v
AL24	GND_64	PWR	Core and IO ground supply = 0v
AL25	GND_65	PWR	Core and IO ground supply = 0v
AL26	VCC1V2_36	PWR	1.20 vdc nominal
AL27	GND__66	PWR	Core and IO ground supply = 0v
AL28	VCC1V2_37	PWR	1.20 vdc nominal
AL29	VCC1V2_38	PWR	1.20 vdc nominal
AL30	VCC1V2_39	PWR	1.20 vdc nominal
AL31	VCC1V2_13	PWR	1.20 vdc nominal
AL32	VCC2V5_26	PWR	3.30 vdc nominal
AL33	MBData[119]		
AL34	MBData[118]		
AL35	MBData[117]		
AL36	MBData[116]		
AM 1	DacARed		
AM 2	GND_67	PWR	Core and IO ground supply = 0v
AM 3	DacAAG[1]		
AM 4	GND_68	PWR	Core and IO ground supply = 0v
AM 5	GND_69	PWR	Core and IO ground supply = 0v

BGA PAD	PIN NAME	TYPE	DESCRIPTION
AM 6	VDD_TTL_5	PWR	3.30 vdc nominal
AM 7	GND_70	PWR	Core and IO ground supply = 0v
AM 8	DfpBDDCData		
AM 9	DfpBDDCClk		
AM10	DfpADDCData		
AM11	PLLAG[1]	PWR	PLL analogue ground = 0v (isolated from GND)
AM12	GND_71	PWR	Core and IO ground supply = 0v
AM13	TestSelect[1]	IN	Production test mode select
AM14	TestSelect[0]	IN	Production test mode select
AM15	GND_72	PWR	Core and IO ground supply = 0v
AM16	GND_73	PWR	Core and IO ground supply = 0v
AM17	GND_74	PWR	Core and IO ground supply = 0v
AM18	VDDQ_1		
AM19	GND_75	PWR	Core and IO ground supply = 0v
AM20	GND_76	PWR	Core and IO ground supply = 0v
AM21	GND_77	PWR	Core and IO ground supply = 0v
AM22	PCIIdSel	IN	
AM23	AGP3V3[1]	PWR	3.30vdc nominal
AM24	VDDQ_2		
AM25	GND_78	PWR	Core and IO ground supply = 0v
AM26	AGPZSET	IN	Analog reference impedance(resistor)-connect to VDDQ via 37.5 ohms
AM27	GND_79	PWR	Core and IO ground supply = 0v
AM28	GND_80	PWR	Core and IO ground supply = 0v
AM29	GND_81	PWR	Core and IO ground supply = 0v
AM30	GND_82	PWR	Core and IO ground supply = 0v
AM31	AGPADSTB[0]	IN	AD_STB0 (agp only)
AM32	GND_83	PWR	Core and IO ground supply = 0v
AM33	MBData[122]		
AM34	MBData[121]		
AM35	MBData[120]		
AM36	MBVref[3]		
AN 1	GND_84	PWR	Core and IO ground supply = 0v
AN 2	GND_85	PWR	Core and IO ground supply = 0v
AN 3	GND_86	PWR	Core and IO ground supply = 0v
AN 4	DacAAG[0]		
AN 5	GND_87	PWR	Core and IO ground supply = 0v
AN 6	VidInData[5]		
AN 7	GenLockHSync		
AN 8	GenLockStereo		
AN 9	VidLock[0]		
AN10	PLLAG[2]	PWR	PLL analogue ground = 0v (isolated from GND)
AN11	GND_88	PWR	Core and IO ground supply = 0v
AN12	RefClkIn		
AN13	VDD_TTL_8	PWR	3.30 vdc nominal
AN14	AGPVDet		
AN15	GND_90	PWR	Core and IO ground supply = 0v
AN16	AGP3V3[3]	PWR	3.30vdc nominal
AN17	AGPPipeN	OUT	PIPE#-Pipelined request(agp only)[3.3V]
AN18	AGPSBA[1]	OUT	SBA(7-0) sideband address port (agp only) (1.5-3.3v)
AN19	AGPSBA[2]	OUT	SBA(7-0) sideband address port (agp only) (1.5-3.3v)
AN20	AGPSBA[7]	OUT	SBA(7:0)-Sideband address port(agp only)[1.5-3.3V]
AN21	PCIAD[30]	BIDIR	AD(31-0) address and data bus (1.5-3.3V)
AN22	PCIAD[26]	BIDIR	AD(31-0) address and data bus (1.5-3.3V)

BGA PAD	PIN NAME	TYPE	DESCRIPTION
AN23	PCIAD[24]	BIDIR	AD(31-0) address and data bus (1.5-3.3V)
AN24	PCIAD[22]	BIDIR	AD(31-0) address and data bus (1.5-3.3V)
AN25	PCIAD[18]	BIDIR	AD(31-0) address and data bus (1.5-3.3V)
AN26	PCIFrameN	BIDIR	Frame# Cycle Frame(3.3v)
AN27	PCITRdyN	BIDIR	TRDY# Target Ready[3.3v]
AN28	PCIPar	BIDIR	PAR Parity (3.3v)
AN29	PCIAD[13]	BIDIR	AD(31-0) address and data bus (1.5-3.3V)
AN30	PCIAD[9]	BIDIR	AD(31-0) address and data bus (1.5-3.3V)
AN31	AGPADSTBN[0]	IN	AD_STB0/1#(agp only)AD strobe-used in agp4x only[1.5V]
AN32	PCIAD[4]	BIDIR	AD(31-0) address and data bus (1.5-3.3V)
AN33	PCIAD[0]	BIDIR	AD(31-0) address and data bus (1.5-3.3V)
AN34	MBData[124]		
AN35	MBData[123]		
AN36	MBDqs[15]		
AP 1	VidAHSync	OUT	DAC Horizontal sync
AP 2	VidAVSync	OUT	DAC Vertical sync
AP 3	GND_91	PWR	Core and IO ground supply = 0v
AP 4	GND_92	PWR	Core and IO ground supply = 0v
AP 5	VidInStrobe		
AP 6	VidInData[4]		
AP 7	GenLockClkOut		
AP 8	GenLockStrobeIn		
AP 9	VidLock[1]		
AP10	PLLVAA[2]	PWR	PLL analogue power 3.3v
AP11	PLLVAA[1]	PWR	PLL analogue power 3.3v
AP12	D1ClkIn		
AP13	MClkIn	BIDIR	External M clock input
AP14	GND_93	PWR	Core and IO ground supply = 0v
AP15	GND_94	PWR	Core and IO ground supply = 0v
AP16	GND_96	PWR	Core and IO ground supply = 0v
AP17	AGPSt[1]	BIDIR	ST Status bus(agp only)[3.3V]
AP18	AGPWbfN		
AP19	AGPSBA[3]	OUT	SBA(7-0) sideband address port (agp only) (1.5-3.3v)
AP20	AGPSBA[5]	OUT	SBA(7:0)-Sideband address port(agp only)[1.5-3.3V]
AP21	AGP3V3[4]	PWR	3.30vdc nominal
AP22	PCIAD[28]	BIDIR	AD(31-0) address and data bus (1.5-3.3V)
AP23	AGPADSTBN[1]	IN	AD_STB0/1#(agp only)AD strobe-used in agp4x only[1.5V]
AP24	PCICBEN[3]	BIDIR	C/BE Command Bus Byte Enables{1.5V-3.3v]
AP25	PCIAD[20]	BIDIR	AD(31-0) address and data bus (1.5-3.3V)
AP26	PCIAD[16]	BIDIR	AD(31-0) address and data bus (1.5-3.3V)
AP27	AGP3V3[0]	PWR	3.30vdc nominal
AP28	PCIStopN	BIDIR	STOP# [3.3v]
AP29	PCIAD[15]	BIDIR	AD(31-0) address and data bus (1.5-3.3V)
AP30	PCIAD[11]	BIDIR	AD(31-0) address and data bus (1.5-3.3V)
AP31	PCICBEN[0]	BIDIR	C/BE Command Bus Byte Enables{1.5V-3.3v]
AP32	PCIAD[6]	BIDIR	AD(31-0) address and data bus (1.5-3.3V)
AP33	PCIAD[2]	BIDIR	AD(31-0) address and data bus (1.5-3.3V)
AP34	GND_95	PWR	Core and IO ground supply = 0v
AP35	MBData[126]		
AP36	MBData[125]		
AR 1	VidBHSync		
AR 2	VidBVSync		

BGA PAD	PIN NAME	TYPE	DESCRIPTION
AR 3	VidADDCClk		
AR 4	VidADDCData		
AR 5	VidInData[7]		
AR 6	VidInData[3]		
AR 7	VidInData[2]		
AR 8	GenLockVSync		
AR 9	ScanEnable		
AR10	DfpADDCClk		
AR11	GClkIn		
AR12	D0ClkIn		
AR13	PLLAG[0]	PWR	PLL analogue ground = 0v (islolated from GND)
AR14	PCIRstN	IN	RST# Reset (3.3v)
AR15	PCIClk	IN	Clk PciClk (3.3v)
AR16	PCIGntN	IN	Gnt# Grant (3.3v)
AR17	AGPSt[2]	BIDIR	ST Status bus (agp only) [3.3V]
AR19	AGPSBSTB	OUT	SB_STB Sideband strobe (agp only)-(differential in AGP4x)[1.5V-3.3V]
AR20	AGPSBA[6]	OUT	SBA(7:0)-Sideband address port(agp only)[1.5-3.3V]
AR21	GND_97	PWR	Core and IO ground supply = 0v
AR22	PCIAD[29]	BIDIR	AD(31-0) address and data bus (1.5-3.3V)
AR23	AGPADSTB[1]	IN	AD_STB0/1# (agp only) AD strobe - used in agp4x only (1.5v)
AR24	PCIAD[23]	BIDIR	AD(31-0) address and data bus (1.5-3.3V)
AR25	PCIAD[19]	BIDIR	AD(31-0) address and data bus (1.5-3.3V)
AR26	PCICBEN[2]	BIDIR	C/BE Command Bus Byte Enables{1.5V-3.3v]
AR27	GND_98	PWR	Core and IO ground supply = 0v
AR28	PCIDevSelN	BIDIR	DEVSEL# Device select[1.5V-3.3V]
AR29	PCIAD[14]	BIDIR	AD(31-0) address and data bus (1.5-3.3V)
AR30	PCIAD[10]	BIDIR	AD(31-0) address and data bus (1.5-3.3V)
AR31	AGP3V3[2]	PWR	3.30vdc nominal
AR32	PCIAD[5]	BIDIR	AD(31-0) address and data bus (1.5-3.3V)
AR33	PCIAD[1]	BIDIR	AD(31-0) address and data bus (1.5-3.3V)
AR34	VDDQ_3		
AR35	GND_99	PWR	Core and IO ground supply = 0v
AR36	MBData[127]		
AT 1	GND_100	PWR	Core and IO ground supply = 0v
AT 2	VDD_TTL_6	PWR	3.30 vdc nominal
AT 3	VidBDDCClk		
AT 4	VidBDDCData		
AT 5	VidInData[6]		
AT 6	GND_101	PWR	Core and IO ground supply = 0v
AT 7	VidInData[1]		
AT 8	VidInData[0]		
AT 9	GND_102	PWR	Core and IO ground supply = 0v
AT10	VDD_TTL_7	PWR	3.30 vdc nominal
AT11	Xtal	BIDIR	External crystal connections
AT12	GND_103	PWR	Core and IO ground supply = 0v
AT13	PLLVAA[0]	PWR	PLL analogue power = 3.3v
AT14	PCIIntAN	OUT	INTA# Interrupt A open drain
AT15	VDDQ_4		
AT16	PCIReqN	OUT	REQ# Request[3.3v]
AT17	AGPSt[0]	BIDIR	ST Status bus (agp only) (1.5-3.3v)
AT18	AGPRbfN	BIDIR	RGF# Read buffer full (AGP only) (3.3v)

BGA PAD	PIN NAME	TYPE	DESCRIPTION
AT19	AGPSBSTBN	OUT	SB_STB# Sideband strobe (agp only) differential strobe used in agp4x only (1.5v).
AT20	AGPSBA[4]	OUT	SBA(7:0)-Sideband address port(agp only)[1.5-3.3V]
AT21	VDDQ_5		
AT22	PCIAD[31]	BIDIR	AD(31-0) address and data bus (1.5-3.3V)
AT23	PCIAD[27]	BIDIR	AD(31-0) address and data bus (1.5-3.3V)
AT24	PCIAD[25]	BIDIR	AD(31-0) address and data bus (1.5-3.3V)
AT25	PCIAD[21]	BIDIR	AD(31-0) address and data bus (1.5-3.3V)
AT26	PCIAD[17]	BIDIR	AD(31-0) address and data bus (1.5-3.3V)
AT27	VDDQ_6		
AT28	PCIIRdyN	BIDIR	IRDY# Initiator ready (3.3v)
AT29	PCICBEN[1]	BIDIR	C/BE Command Bus Byte Enables{1.5V-3.3v]
AT30	PCIAD[12]	BIDIR	AD(31-0) address and data bus (1.5-3.3V)
AT31	PCIAD[8]	BIDIR	AD(31-0) address and data bus (1.5-3.3V)
AT32	PCIAD[7]	BIDIR	AD(31-0) address and data bus (1.5-3.3V)
AT33	PCIAD[3]	BIDIR	AD(31-0) address and data bus (1.5-3.3V)
AT34	AGPVREF	BIDIR	AGP I/O Reference voltage = VCCA 15/2 (1.67v or 0.75v)
AT35	GND_104	PWR	Core and IO ground supply = 0v
AT36	VCC2V5_27	PWR	
B 1	VCC2V5_5	PWR	
B 2	MAData[72]		
B 3	GND_3	PWR	Core and IO ground supply = 0v
B 4	VCC2V5_6	PWR	
B 5	MACke		
B 6	MAAddr[4]		Memory Address signal
B 7	GND_4	PWR	Core and IO ground supply = 0v
B 8	MAAddr[2]		Memory Address signal
B 9	MAAddrC[1]		
B10	MAAddrC[3]		
B11	MAAddr[8]		Memory Address signal
B12	MAAddrB[0]	BIDIR	Memory B Address signal
B13	MAAddrA		
B14	VCC2V5_7	PWR	
B15	MAAddr[9]		Memory Address signal
B16	MABa[1]		
B17	MARasN		
B18	MAWeN		
B19	MAData[34]		
B20	GND_5	PWR	Core and IO ground supply = 0v
B21	MAData[25]		
B22	MAVref[0]	PWR	Supplied from SSTL_Vref = VCC2V5/2
B23	MAData[18]		
B24	MAData[14]		
B25	MAData[10]		
B26	GND_6	PWR	Core and IO ground supply = 0v
B27	MAData[0]		
B28	MBData[3]		
B29	MBData[7]		
B30	MBData[11]		
B31	MBData[15]		
B32	MBData[18]		
B33	MBData[22]		
B34	MBData[24]		

BGA PAD	PIN NAME	TYPE	DESCRIPTION
B35	GND_7	PWR	Core and IO ground supply = 0v
B36	MBData[26]		
C 1	MAData[75]		
C 2	GND_8	PWR	Core and IO ground supply = 0v
C 3	GND_9	PWR	Core and IO ground supply = 0v
C 4	MAData[71]		
C 5	MAData[69]		
C 6	MADqs[8]		
C 7	MAData[65]		
C 8	MAData[62]		
C 9	MADqs[7]		
C10	MAData[58]		
C11	MAData[55]		
C12	MADqs[6]		
C13	MAData[50]		
C14	MAData[47]		
C15	MADqs[5]		
C16	MAData[43]		
C17	MAData[40]		
C18	MADqs[4]		
C19	MAData[33]		
C20	MAData[29]		
C21	MAData[24]		
C22	MAData[22]		
C23	MAData[17]		
C24	MAData[13]		
C25	MAData[9]		
C26	MAData[5]		
C27	MBData[0]		
C28	MBData[4]		
C29	MBData[8]		
C30	MBData[12]		
C31	GND_10	PWR	Core and IO ground supply = 0v
C32	MBData[19]		
C33	MBData[23]		
C34	MBData[29]		
C35	MBData[28]		
C36	MBData[27]		
D 1	MAData[78]		
D 2	MAData[77]		
D 3	MAData[76]		
D 4	MAData[70]		
D 5	MAData[68]		
D 6	MAData[67]		
D 7	MAData[64]		
D 8	MAData[61]		
D 9	GND_11	PWR	Core and IO ground supply = 0v
D10	MAData[57]		
D11	MAData[54]		
D12	GND_12	PWR	Core and IO ground supply = 0v
D13	MAData[49]		
D14	MAData[46]		
D15	GND_13	PWR	Core and IO ground supply = 0v
D16	MAData[42]		

BGA PAD	PIN NAME	TYPE	DESCRIPTION
D17	MAData[39]		
D18	GND_14	PWR	Core and IO ground supply = 0v
D19	MAData[32]		
D20	MAData[28]		
D21	MAData[23]		
D22	MAData[21]		
D23	MAData[16]		
D24	MAData[12]		
D25	MAData[8]		
D26	MAData[4]		
D27	MBData[1]		
D28	MBData[5]		
D29	MBData[9]		
D30	MBData[13]		
D31	MBData[16]		
D32	MBData[20]		
D33	MBData[32]		
D34	MBData[31]		
D35	MBData[30]		
D36	MBVref[1]		
E 1	MAVref[1]	PWR	Supplied from SSTL_Vref = VCC2V5/2
E 2	GND_15	PWR	Core and IO ground supply = 0v
E 3	MAData[79]		
E 4	VCC2V5_8	PWR	3.30vdc nominal
E 5	GND_16	PppWR	Core and IO ground supply = 0v
E 6	MAData[66]		
E 7	MAData[63]		
E 8	MAData[60]		
E 9	MAData[59]		
E10	MAData[56]		
E11	MAData[53]		
E12	MAData[52]		
E13	MAData[48]		
E14	MAData[45]		
E15	MAData[44]		
E16	MAData[41]		
E17	MAData[38]		
E18	MAData[37]		
E19	MAData[31]		
E20	MAData[27]		
E21	GND_17	PWR	Core and IO ground supply = 0v
E22	MAData[20]		
E23	MAData[15]		
E24	MAData[11]		
E25	MAData[7]		
E26	MAData[3]		
E27	MBData[2]		
E28	MBData[6]		
E29	MBData[10]		
E30	MBData[14]		
E31	MBData[17]		
E32	VCC2V5_9	PWR	3.30vdc nominal
E33	MBData[35]		
E34	MBData[34]		

BGA PAD	PIN NAME	TYPE	DESCRIPTION
E35	MBData[33]		
E36	MBDqs[4]		
F 1	MADqs[10]		
F 2	MAData[83]		
F 3	MAData[82]		
F 4	MAData[81]		
F 5	MAData[80]		
F 6	VCC1V2_1	PWR	1.20 vdc nominal
F 7	VCC1V2_2	PWR	1.20 vdc nominal
F 8	VCC1V2_3	PWR	1.20 vdc nominal
F 9	VCC1V2_4	PWR	1.20 vdc nominal
F10	GND_18	PWR	Core and IO ground supply = 0v
F11	VCC2V5_10	PWR	3.30vdc nominal
F12	MAData[51]		
F13	VCC1V2_5	PWR	1.20 vdc nominal
F14	VCC1V2_6	PWR	
F15	GND_19	PWR	Core and IO ground supply = 0v
F16	VCC2V5_11	PWR	3.30vdc nominal
F17	GND_20	PWR	Core and IO ground supply = 0v
F18	MAData[36]		
F19	MAData[30]		
F20	GND_21	PWR	Core and IO ground supply = 0v
F21	VCC2V5_12	PWR	3.30vdc nominal
F22	MAData[19]		
F23	VCC1V2_7	PWR	1.20 vdc nominal
F24	VCC1V2_8	PWR	1.20 vdc nominal
F25	MAData[6]		
F26	MAData[2]		
F27	GND_22	PWR	Core and IO ground supply = 0v
F28	VCC1V2_9	PWR	1.20 vdc nominal
F29	VCC1V2_10	PWR	1.20 vdc nominal
F30	VCC1V2_11	PWR	1.20 vdc nominal
F31	VCC1V2_12	PWR	1.20 vdc nominal
F32	MBData[39]		
F33	MBData[38]		
F34	MBData[37]		
F35	MBData[36]		
F36	VCC2V5_13	PWR	3.30vdc nominal
G 1	MAData[88]		
G 2	MAData[87]		
G 3	MAData[86]		
G 4	MAData[85]		
G 5	MAData[84]		
G 6	VCC1V2_14	PWR	1.20 vdc nominal
G31	VCC1V2_15	PWR	1.20 vdc nominal
G32	MBData[43]		
G33	MBData[42]		
G34	MBData[41]		
G35	MBData[40]		
G36	MBDqs[5]		
H 1	GND_23	PWR	Core and IO ground supply = 0v
H 2	VCC2V5_14	PWR	3.30vdc nominal
H 3	MAData[91]		
H 4	MAData[90]		

BGA PAD	PIN NAME	TYPE	DESCRIPTION
H 5	MAData[89]		
H 6	VCC1V2_16	PWR	1.20 vdc nominal
H31	VCC1V2_17	PWR	1.20 vdc nominal
H32	MBData[47]		
H33	MBData[46]		
H34	MBData[45]		
H35	MBData[44]		
H36	MBVref[2]		
J 1	MADqs[11]		
J 2	MAData[95]		
J 3	MAData[94]		
J 4	MAData[93]		
J 5	MAData[92]		
J 6	VCC1V2_18	PWR	1.20 vdc nominal
J31	VCC1V2_19	PWR	1.20 vdc nominal
J32	MBData[49]		
J33	VCC2V5_15	PWR	3.30 vdc nominal
J34	MBData[48]		
J35	GND_24	PWR	Core and IO ground supply = 0v
J36	MBDqs[6]		
K 1	MAVref[2]		
K 2	MAData[100]		
K 3	MAData[99]		
K 4	MAData[98]		
K 5	MAData[97]		
K 6	MAData[96]		
K31	GND_25	PWR	Core and IO ground supply = 0v
K32	MBData[54]		
K33	MBData[53]		
K34	MBData[52]		
K35	MBData[51]		
K36	MBData[50]		
L 1	MADqs[12]		
L 2	MAData[104]		
L 3	MAData[103]		
L 4	MAData[102]		
L 5	MAData[101]		
L 6	GND_26	PWR	Core and IO ground supply = 0v
L31	VCC2V5_16	PWR	3.30vdc nominal
L32	MBData[58]		
L33	MBData[57]		
L34	MBData[56]		
L35	MBData[55]		
L36	MBDqs[7]		
M 1	GND_27	PWR	Core and IO ground supply = 0v
M 2	VCC2V5_17	PWR	3.30vdc nominal
M 3	MAData[107]		
M 4	MAData[106]		
M 5	MAData[105]		
M 6	VCC2V5_18	PWR	3.30vdc nominal
M31	MBData[63]		
M32	MBData[62]		
M33	MBData[61]		
M34	MBData[60]		

BGA PAD	PIN NAME	TYPE	DESCRIPTION
M35	MBData[59]		
M36	MBWeN		
N 1	MADqs[13]		
N 2	MAData[112]		
N 3	MAData[111]		
N 4	MAData[110]		
N 5	MAData[109]		
N 6	MAData[108]		
N31	MBData[67]		
N32	MBData[66]		
N33	MBData[65]		
N34	MBData[64]		
N35	MBCasN		
N36	MBRasN		
P 1	MADqs[14]		
P 2	MAData[117]		
P 3	MAData[116]		
P 4	MAData[115]		
P 5	MAData[114]		
P 6	MAData[113]		
P31	MBData[70]		
P32	MBData[69]		
P33	MBData[68]		
P34	MBDqs[8]		
P35	MBBa[0]		
P36	MBBa[1]		
R 1	MAVref[3]		
R 2	MAData[122]		
R 3	MAData[121]		
R 4	MAData[120]		
R 5	MAData[119]		
R 6	MAData[118]		
R31	MBData[74]		
R32	MBData[73]		
R33	MBData[72]		
R34	MBData[71]		
R35	MBAddr[0]		
R36	MBAddr[9]		
T 1	MADqs[15]		
T 2	MAData[127]		
T 3	MAData[126]		
T 4	MAData[125]		
T 5	MAData[124]		
T 6	MAData[123]		
T31	MBData[78]		
T32	MBData[77]		
T33	MBData[76]		
T34	MBData[75]		
T35	MBAddr[1]		
T36	MBAddrA		
U 1	GND_28	PWR	Core and IO ground supply = 0v
U 2	VCC2V5_19	PWR	3.30vdc nominal
U 3	VCC_DFP_1	PWR	3.30 vdc nominal
U 4	GND_29	PWR	Core and IO ground supply = 0v

BGA PAD	PIN NAME	TYPE	DESCRIPTION
U 5	GND_30	PWR	Core and IO ground supply = 0v
U 6	VCC2V5_20	PWR	3.30vdc nominal
U31	VCC2V5_21	PWR	3.30vdc nominal
U32	MBData[79]		
U33	GND_31	PWR	Core and IO ground supply = 0v
U34	MBDqs[9]		
U35	MBAddrB[1]		
U36	MBAddrB[0]		
V 1	DfpData[0]		
V 2	DfpData[1]		
V 3	DfpData[2]		
V 4	DfpData[3]		
V 5	DfpData[4]		
V 6	DfpData[5]		
V31	GND_32	PWR	Core and IO ground supply = 0v
V32	MBData[82]		
V33	MBData[81]		
V34	MBData[80]		
V35	VCC2V5_22	PWR	
V36	GND_33	PWR	Core and IO ground supply = 0v
W 1	DfpVref[0]		
W 2	DfpAStrobe		
W 3	DfpData[6]		
W 4	DfpData[7]		
W 5	DfpData[8]		
W 6	DfpData[9]		
W31	GND_34	PWR	Core and IO ground supply = 0v
W32	MBData[84]		
W33	MBData[83]		
W34	GND_35	PWR	Core and IO ground supply = 0v
W35	MBAddr[7]		
W36	MBAddr[8]		
Y 1	DfpData[10]		
Y 2	DfpData[11]		
Y 3	DfpABlank		
Y 4	DfpAHSync		
Y 5	DfpAVSync		
Y 6	VCC_DFP_2	PWR	3.30 vdc nominal
Y31	MBData[87]		
Y32	MBData[86]		
Y33	MBData[85]		
Y34	MBDqs[10]		
Y35	MBAddr[6]		
Y36	MBAddrC[3]		

8.2 Pinlist by Name

The table below provides a brief description of each pin. It is organized alphabetically by pin name. The block of GND pins from M12 to V18 is not included - these are listed in section 8.3, *Ground Connections*.

BGA PAD	PIN NAME	TYPE	DESCRIPTION
AP27	AGP3V3[0]	PWR	3.30vdc nominal
AM23	AGP3V3[1]	PWR	3.30vdc nominal
AR31	AGP3V3[2]	PWR	3.30vdc nominal
AN16	AGP3V3[3]	PWR	3.30vdc nominal
AP21	AGP3V3[4]	PWR	3.30vdc nominal
AM31	AGPADSTB[0]	IN	AD_STB0 (agp only)
AR23	AGPADSTB[1]	IN	AD_STB0/1# (agp only) AD strobe - used in agp4x only (1.5v)
AN31	AGPADSTBN[0]	IN	AD_STB0/1#(agp only)AD strobe-used in agp4x only[1.5V]
AP23	AGPADSTBN[1]	IN	AD_STB0/1#(agp only)AD strobe-used in agp4x only[1.5V]
AN17	AGPPipeN	OUT	PIPE#-Pipelined request(agp only)[3.3V]
AT18	AGPRbfN	BIDIR	RGF# Read buffer full (AGP only) (3.3v)
AN18	AGPSBA[1]	OUT	SBA(7-0) sideband address port (agp only) (1.5-3.3v)
AN19	AGPSBA[2]	OUT	SBA(7-0) sideband address port (agp only) (1.5-3.3v)
AP19	AGPSBA[3]	OUT	SBA(7-0) sideband address port (agp only) (1.5-3.3v)
AT20	AGPSBA[4]	OUT	SBA(7:0)-Sideband address port(agp only)[1.5-3.3V]
AP20	AGPSBA[5]	OUT	SBA(7:0)-Sideband address port(agp only)[1.5-3.3V]
AR20	AGPSBA[6]	OUT	SBA(7:0)-Sideband address port(agp only)[1.5-3.3V]
AN20	AGPSBA[7]	OUT	SBA(7:0)-Sideband address port(agp only)[1.5-3.3V]
AR19	AGPSBSTB	OUT	SB_STB Sideband strobe (agp only)-(differential in AGP4x)[1.5V-3.3V]
AT19	AGPSBSTBN	OUT	SB_STB# Sideband strobe (agp only) differential strobe used in agp4x only (1.5v).
AT17	AGPSt[0]	BIDIR	ST Status bus (agp only) (1.5-3.3v)
AP17	AGPSt[1]	BIDIR	ST Status bus(agp only)[3.3V]
AR17	AGPSt[2]	BIDIR	ST Status bus (agp only) [3.3V]
AN14	AGPVDet		
AT34	AGPVREF	BIDIR	AGP I/O Reference voltage = VCCA 15/2 (1.67v or 0.75v)
AP18	AGPWbfN		
AM26	AGPZSET	IN	Analog reference impedance(resistor)-connect to VDDQ via 37.5 ohms
AR12	D0ClkIn		
AP12	D1ClkIn		
AN 4	DacAAG[0]		
AM 3	DacAAG[1]		
AK 3	DacAAG[2]		
AK 5	DacAAG[3]		
AK 2	DacABlue		
AL 5	DacAComp		
AK 4	DacAFSAdj		
AL 1	DacAGreen		
AM 1	DacARed		
AL 2	DacAVAA[0]		
AL 4	DacAVAA[1]		
AK 1	DacAVAA[2]		

BGA PAD	PIN NAME	TYPE	DESCRIPTION
AL 3	DacAVref		
AJ 4	DacBAG[0]		
AH 3	DacBAG[1]		
AF 2	DacBAG[2]		
AF 5	DacBAG[3]		
AF 1	DacBBlue		
AG 5	DacBComp		
AF 3	DacBFSAdj		
AG 1	DacBGreen		
AH 1	DacBRed		
AG 2	DacBVAA[0]		
AG 4	DacBVAA[1]		
AG 6	DacBVAA[2]		
AG 3	DacBVref		
Y 3	DfpABlank		
AR10	DfpADDCClk		
AM10	DfpADDCData		
Y 4	DfpAHSync		
W 2	DfpAStrobe		
Y 5	DfpAVSync		
AC 6	DfpBBlank		
AM 9	DfpBDDCClk		
AM 8	DfpBDDCData		
AD 1	DfpBHSync		
AB 2	DfpBStrobe		
AD 2	DfpBVSync		
V 1	DfpData[0]		
V 2	DfpData[1]		
Y 1	DfpData[10]		
Y 2	DfpData[11]		
AA 3	DfpData[12]		
AA 4	DfpData[13]		
AA 5	DfpData[14]		
AA 6	DfpData[15]		
AB 3	DfpData[16]		
AB 4	DfpData[17]		
AB 5	DfpData[18]		
AC 1	DfpData[19]		
V 3	DfpData[2]		
AC 2	DfpData[20]		
AC 3	DfpData[21]		
AC 4	DfpData[22]		
AC 5	DfpData[23]		
V 4	DfpData[3]		
V 5	DfpData[4]		
V 6	DfpData[5]		
W 3	DfpData[6]		
W 4	DfpData[7]		
W 5	DfpData[8]		
W 6	DfpData[9]		
W 1	DfpVref[0]		
AB 1	DfpVref[1]		
AL11	ExtIntr		
AR11	GClkIn		

BGA PAD	PIN NAME	TYPE	DESCRIPTION
AP 7	GenLockClkOut		
AN 7	GenLockHSync		
AN 8	GenLockStereo		
AP 8	GenLockStrobeIn		
AR 8	GenLockVSync		
AL27	GND_66	POWER	Core and IO ground supply = 0v
A14	GND_1	POWER	Core and IO ground supply = 0v
C31	GND_10	POWER	Core and IO ground supply = 0v
AT 1	GND_100	POWER	Core and IO ground supply = 0v
AT 6	GND_101	POWER	Core and IO ground supply = 0v
AT 9	GND_102	POWER	Core and IO ground supply = 0v
AT12	GND_103	POWER	Core and IO ground supply = 0v
AT35	GND_104	POWER	Core and IO ground supply = 0v
D 9	GND_11	POWER	Core and IO ground supply = 0v
D12	GND_12	POWER	Core and IO ground supply = 0v
D15	GND_13	POWER	Core and IO ground supply = 0v
D18	GND_14	POWER	Core and IO ground supply = 0v
E 2	GND_15	POWER	Core and IO ground supply = 0v
E 5	GND_16	POWER	Core and IO ground supply = 0v
E21	GND_17	POWER	Core and IO ground supply = 0v
F10	GND_18	POWER	Core and IO ground supply = 0v
F15	GND_19	POWER	Core and IO ground supply = 0v
A23	GND_2	POWER	Core and IO ground supply = 0v
F17	GND_20	POWER	Core and IO ground supply = 0v
F20	GND_21	POWER	Core and IO ground supply = 0v
F27	GND_22	POWER	Core and IO ground supply = 0v
H 1	GND_23	POWER	Core and IO ground supply = 0v
J35	GND_24	POWER	Core and IO ground supply = 0v
K31	GND_25	POWER	Core and IO ground supply = 0v
L 6	GND_26	POWER	Core and IO ground supply = 0v
M 1	GND_27	POWER	Core and IO ground supply = 0v
U 1	GND_28	POWER	Core and IO ground supply = 0v
U 4	GND_29	POWER	Core and IO ground supply = 0v
B 3	GND_3	POWER	Core and IO ground supply = 0v
U 5	GND_30	POWER	Core and IO ground supply = 0v
U33	GND_31	POWER	Core and IO ground supply = 0v
V31	GND_32	POWER	Core and IO ground supply = 0v
V36	GND_33	POWER	Core and IO ground supply = 0v
W31	GND_34	POWER	Core and IO ground supply = 0v
W34	GND_35	POWER	Core and IO ground supply = 0v
AA 2	GND_36	POWER	Core and IO ground supply = 0v
AB33	GND_37	POWER	Core and IO ground supply = 0v
AD 4	GND_38	POWER	Core and IO ground supply = 0v
AD 5	GND_39	POWER	Core and IO ground supply = 0v
B 7	GND_4	POWER	Core and IO ground supply = 0v
AD33	GND_40	POWER	Core and IO ground supply = 0v
AE 2	GND_41	POWER	Core and IO ground supply = 0v
AE 3	GND_42	POWER	Core and IO ground supply = 0v
AE 4	GND_43	POWER	Core and IO ground supply = 0v
AE 6	GND_44	POWER	Core and IO ground supply = 0v
AE33	GND_45	POWER	Core and IO ground supply = 0v
AF 4	GND_46	POWER	Core and IO ground supply = 0v
AF35	GND_47	POWER	Core and IO ground supply = 0v
AG31	GND_48	POWER	Core and IO ground supply = 0v

BGA PAD	PIN NAME	TYPE	DESCRIPTION
AG32	GND_49	POWER	Core and IO ground supply = 0v
B20	GND_5	POWER	Core and IO ground supply = 0v
AG35	GND_50	POWER	Core and IO ground supply = 0v
AH 2	GND_51	POWER	Core and IO ground supply = 0v
AH 4	GND_52	POWER	Core and IO ground supply = 0v
AH 5	GND_53	POWER	Core and IO ground supply = 0v
AJ 2	GND_54	POWER	Core and IO ground supply = 0v
AJ 3	GND_55	POWER	Core and IO ground supply = 0v
AJ35	GND_56	POWER	Core and IO ground supply = 0v
AK34	GND_57	POWER	Core and IO ground supply = 0v
AK35	GND_58	POWER	Core and IO ground supply = 0v
AL10	GND_59	POWER	Core and IO ground supply = 0v
B26	GND_6	POWER	Core and IO ground supply = 0v
AL18	GND_60	POWER	Core and IO ground supply = 0v
AL19	GND_61	POWER	Core and IO ground supply = 0v
AL22	GND_62	POWER	Core and IO ground supply = 0v
AL23	GND_63	POWER	Core and IO ground supply = 0v
AL24	GND_64	POWER	Core and IO ground supply = 0v
AL25	GND_65	POWER	Core and IO ground supply = 0v
AM 2	GND_67	POWER	Core and IO ground supply = 0v
AM 4	GND_68	POWER	Core and IO ground supply = 0v
AM 5	GND_69	POWER	Core and IO ground supply = 0v
B35	GND_7	POWER	Core and IO ground supply = 0v
AM 7	GND_70	POWER	Core and IO ground supply = 0v
AM12	GND_71	POWER	Core and IO ground supply = 0v
AM15	GND_72	POWER	Core and IO ground supply = 0v
AM16	GND_73	POWER	Core and IO ground supply = 0v
AM17	GND_74	POWER	Core and IO ground supply = 0v
AM19	GND_75	POWER	Core and IO ground supply = 0v
AM20	GND_76	POWER	Core and IO ground supply = 0v
AM21	GND_77	POWER	Core and IO ground supply = 0v
AM25	GND_78	POWER	Core and IO ground supply = 0v
AM27	GND_79	POWER	Core and IO ground supply = 0v
C 2	GND_8	POWER	Core and IO ground supply = 0v
AM28	GND_80	POWER	Core and IO ground supply = 0v
AM29	GND_81	POWER	Core and IO ground supply = 0v
AM30	GND_82	POWER	Core and IO ground supply = 0v
AM32	GND_83	POWER	Core and IO ground supply = 0v
AN 1	GND_84	POWER	Core and IO ground supply = 0v
AN 2	GND_85	POWER	Core and IO ground supply = 0v
AN 3	GND_86	POWER	Core and IO ground supply = 0v
AN 5	GND_87	POWER	Core and IO ground supply = 0v
AN11	GND_88	POWER	Core and IO ground supply = 0v
C 3	GND_9	POWER	Core and IO ground supply = 0v
AN15	GND_90	POWER	Core and IO ground supply = 0v
AP 3	GND_91	POWER	Core and IO ground supply = 0v
AP 4	GND_92	POWER	Core and IO ground supply = 0v
AP14	GND_93	POWER	Core and IO ground supply = 0v
AP15	GND_94	POWER	Core and IO ground supply = 0v
AP34	GND_95	POWER	Core and IO ground supply = 0v
AP16	GND_96	POWER	Core and IO ground supply = 0v
AR21	GND_97	POWER	Core and IO ground supply = 0v
AR27	GND_98	POWER	Core and IO ground supply = 0v
AR35	GND_99	POWER	Core and IO ground supply = 0v

BGA PAD	PIN NAME	TYPE	DESCRIPTION
A16	MAAddr[0]		Memory Address signal
A15	MAAddr[1]		Memory Address signal
B 8	MAAddr[2]		Memory Address signal
A 8	MAAddr[3]		Memory Address signal
B 6	MAAddr[4]		Memory Address signal
A 6	MAAddr[5]		Memory Address signal
A11	MAAddr[6]		Memory Address signal
A12	MAAddr[7]		Memory Address signal
B11	MAAddr[8]		Memory Address signal
B15	MAAddr[9]		Memory Address signal
B13	MAAddrA		
B12	MAAddrB[0]	BIDIR	Memory B Address signal
A13	MAAddrB[1]	BIDIR	Memory B Address signal
A 9	MAAddrC[0]		
B 9	MAAddrC[1]		
A10	MAAddrC[2]		
B10	MAAddrC[3]		
A17	MABa[0]		
B16	MABa[1]		
A18	MACasN		
B 5	MACke		
A 4	MAClk		
A 5	MAClkN		
B27	MAData[0]		
A27	MAData[1]		
B25	MAData[10]		
K 2	MAData[100]		
L 5	MAData[101]		
L 4	MAData[102]		
L 3	MAData[103]		
L 2	MAData[104]		
M 5	MAData[105]		
M 4	MAData[106]		
M 3	MAData[107]		
N 6	MAData[108]		
N 5	MAData[109]		
E24	MAData[11]		
N 4	MAData[110]		
N 3	MAData[111]		
N 2	MAData[112]		
P 6	MAData[113]		
P 5	MAData[114]		
P 4	MAData[115]		
P 3	MAData[116]		
P 2	MAData[117]		
R 6	MAData[118]		
R 5	MAData[119]		
D24	MAData[12]		
R 4	MAData[120]		
R 3	MAData[121]		
R 2	MAData[122]		
T 6	MAData[123]		
T 5	MAData[124]		
T 4	MAData[125]		

BGA PAD	PIN NAME	TYPE	DESCRIPTION
T 3	MAData[126]		
T 2	MAData[127]		
C24	MAData[13]		
B24	MAData[14]		
E23	MAData[15]		
D23	MAData[16]		
C23	MAData[17]		
B23	MAData[18]		
F22	MAData[19]		
F26	MAData[2]		
E22	MAData[20]		
D22	MAData[21]		
C22	MAData[22]		
D21	MAData[23]		
C21	MAData[24]		
B21	MAData[25]		
A21	MAData[26]		
E20	MAData[27]		
D20	MAData[28]		
C20	MAData[29]		
E26	MAData[3]		
F19	MAData[30]		
E19	MAData[31]		
D19	MAData[32]		
C19	MAData[33]		
B19	MAData[34]		
A19	MAData[35]		
F18	MAData[36]		
E18	MAData[37]		
E17	MAData[38]		
D17	MAData[39]		
D26	MAData[4]		
C17	MAData[40]		
E16	MAData[41]		
D16	MAData[42]		
C16	MAData[43]		
E15	MAData[44]		
E14	MAData[45]		
D14	MAData[46]		
C14	MAData[47]		
E13	MAData[48]		
D13	MAData[49]		
C26	MAData[5]		
C13	MAData[50]		
F12	MAData[51]		
E12	MAData[52]		
E11	MAData[53]		
D11	MAData[54]		
C11	MAData[55]		
E10	MAData[56]		
D10	MAData[57]		
C10	MAData[58]		
E 9	MAData[59]		
F25	MAData[6]		

BGA PAD	PIN NAME	TYPE	DESCRIPTION
E 8	MAData[60]		
D 8	MAData[61]		
C 8	MAData[62]		
E 7	MAData[63]		
D 7	MAData[64]		
C 7	MAData[65]		
E 6	MAData[66]		
D 6	MAData[67]		
D 5	MAData[68]		
C 5	MAData[69]		
E25	MAData[7]		
D 4	MAData[70]		
C 4	MAData[71]		
B 2	MAData[72]		
A 2	MAData[73]		
A 1	MAData[74]		
C 1	MAData[75]		
D 3	MAData[76]		
D 2	MAData[77]		
D 1	MAData[78]		
E 3	MAData[79]		
D25	MAData[8]		
F 5	MAData[80]		
F 4	MAData[81]		
F 3	MAData[82]		
F 2	MAData[83]		
G 5	MAData[84]		
G 4	MAData[85]		
G 3	MAData[86]		
G 2	MAData[87]		
G 1	MAData[88]		
H 5	MAData[89]		
C25	MAData[9]		
H 4	MAData[90]		
H 3	MAData[91]		
J 5	MAData[92]		
J 4	MAData[93]		
J 3	MAData[94]		
J 2	MAData[95]		
K 6	MAData[96]		
K 5	MAData[97]		
K 4	MAData[98]		
K 3	MAData[99]		
A26	MADqs[0]		
A24	MADqs[1]		
F 1	MADqs[10]		
J 1	MADqs[11]		
L 1	MADqs[12]		
N 1	MADqs[13]		
P 1	MADqs[14]		
T 1	MADqs[15]		
A22	MADqs[2]		
A20	MADqs[3]		
C18	MADqs[4]		

BGA PAD	PIN NAME	TYPE	DESCRIPTION
C15	MADqs[5]		
C12	MADqs[6]		
C 9	MADqs[7]		
C 6	MADqs[8]		
A 3	MADqs[9]		
B17	MARasN		
B22	MAVref[0]		
E 1	MAVref[1]		
K 1	MAVref[2]		
R 1	MAVref[3]		
B18	MAWeN		
R35	MBAddr[0]		
T35	MBAddr[1]		
AB36	MBAddr[2]		
AC35	MBAddr[3]		
AC36	MBAddr[4]		
AD35	MBAddr[5]		
Y35	MBAddr[6]		
W35	MBAddr[7]		
W36	MBAddr[8]		
R36	MBAddr[9]		
T36	MBAddrA		
U36	MBAddrB[0]		
U35	MBAddrB[1]		
AB35	MBAddrC[0]		
AA36	MBAddrC[1]		
AA35	MBAddrC[2]		
Y36	MBAddrC[3]		
P35	MBBa[0]		
P36	MBBa[1]		
N35	MBCasN		
AD36	MBCke		
AE36	MBClk		
AE35	MBClkN		
C27	MBData[0]		
D27	MBData[1]		
E29	MBData[10]		
AE34	MBData[100]		
AE32	MBData[101]		
AF34	MBData[102]		
AF33	MBData[103]		
AF32	MBData[104]		
AG34	MBData[105]		
AG33	MBData[106]		
AH35	MBData[107]		
AH34	MBData[108]		
AH33	MBData[109]		
B30	MBData[11]		
AH32	MBData[110]		
AJ34	MBData[111]		
AJ33	MBData[112]		
AJ32	MBData[113]		
AK33	MBData[114]		
AK32	MBData[115]		

BGA PAD	PIN NAME	TYPE	DESCRIPTION
AL36	MBData[116]		
AL35	MBData[117]		
AL34	MBData[118]		
AL33	MBData[119]		
C30	MBData[12]		
AM35	MBData[120]		
AM34	MBData[121]		
AM33	MBData[122]		
AN35	MBData[123]		
AN34	MBData[124]		
AP36	MBData[125]		
AP35	MBData[126]		
AR36	MBData[127]		
D30	MBData[13]		
E30	MBData[14]		
B31	MBData[15]		
D31	MBData[16]		
E31	MBData[17]		
B32	MBData[18]		
C32	MBData[19]		
E27	MBData[2]		
D32	MBData[20]		
A33	MBData[21]		
B33	MBData[22]		
C33	MBData[23]		
B34	MBData[24]		
A35	MBData[25]		
B36	MBData[26]		
C36	MBData[27]		
C35	MBData[28]		
C34	MBData[29]		
B28	MBData[3]		
D35	MBData[30]		
D34	MBData[31]		
D33	MBData[32]		
E35	MBData[33]		
E34	MBData[34]		
E33	MBData[35]		
F35	MBData[36]		
F34	MBData[37]		
F33	MBData[38]		
F32	MBData[39]		
C28	MBData[4]		
G35	MBData[40]		
G34	MBData[41]		
G33	MBData[42]		
G32	MBData[43]		
H35	MBData[44]		
H34	MBData[45]		
H33	MBData[46]		
H32	MBData[47]		
J34	MBData[48]		
J32	MBData[49]		
D28	MBData[5]		

BGA PAD	PIN NAME	TYPE	DESCRIPTION
K36	MBData[50]		
K35	MBData[51]		
K34	MBData[52]		
K33	MBData[53]		
K32	MBData[54]		
L35	MBData[55]		
L34	MBData[56]		
L33	MBData[57]		
L32	MBData[58]		
M35	MBData[59]		
E28	MBData[6]		
M34	MBData[60]		
M33	MBData[61]		
M32	MBData[62]		
M31	MBData[63]		
N34	MBData[64]		
N33	MBData[65]		
N32	MBData[66]		
N31	MBData[67]		
P33	MBData[68]		
P32	MBData[69]		
B29	MBData[7]		
P31	MBData[70]		
R34	MBData[71]		
R33	MBData[72]		
R32	MBData[73]		
R31	MBData[74]		
T34	MBData[75]		
T33	MBData[76]		
T32	MBData[77]		
T31	MBData[78]		
U32	MBData[79]		
C29	MBData[8]		
V34	MBData[80]		
V33	MBData[81]		
V32	MBData[82]		
W33	MBData[83]		
W32	MBData[84]		
Y33	MBData[85]		
Y32	MBData[86]		
Y31	MBData[87]		
AA34	MBData[88]		
AA33	MBData[89]		
D29	MBData[9]		
AA32	MBData[90]		
AA31	MBData[91]		
AB34	MBData[92]		
AB32	MBData[93]		
AB31	MBData[94]		
AC33	MBData[95]		
AC32	MBData[96]		
AD34	MBData[97]		
AD32	MBData[98]		
AD31	MBData[99]		

BGA PAD	PIN NAME	TYPE	DESCRIPTION
A28	MBDqs[0]		
A30	MBDqs[1]		
Y34	MBDqs[10]		
AC34	MBDqs[11]		
AF36	MBDqs[12]		
AH36	MBDqs[13]		
AK36	MBDqs[14]		
AN36	MBDqs[15]		
A32	MBDqs[2]		
A34	MBDqs[3]		
E36	MBDqs[4]		
G36	MBDqs[5]		
J36	MBDqs[6]		
L36	MBDqs[7]		
P34	MBDqs[8]		
U34	MBDqs[9]		
N36	MBRasN		
A31	MBVref[0]		
D36	MBVref[1]		
H36	MBVref[2]		
AM36	MBVref[3]		
M36	MBWeN		
AP13	MClkIn	BIDIR	External M clock input
AN33	PCIAD[0]	BIDIR	AD(31-0) address and data bus (1.5-3.3V)
AR33	PCIAD[1]	BIDIR	AD(31-0) address and data bus (1.5-3.3V)
AR30	PCIAD[10]	BIDIR	AD(31-0) address and data bus (1.5-3.3V)
AP30	PCIAD[11]	BIDIR	AD(31-0) address and data bus (1.5-3.3V)
AT30	PCIAD[12]	BIDIR	AD(31-0) address and data bus (1.5-3.3V)
AN29	PCIAD[13]	BIDIR	AD(31-0) address and data bus (1.5-3.3V)
AR29	PCIAD[14]	BIDIR	AD(31-0) address and data bus (1.5-3.3V)
AP29	PCIAD[15]	BIDIR	AD(31-0) address and data bus (1.5-3.3V)
AP26	PCIAD[16]	BIDIR	AD(31-0) address and data bus (1.5-3.3V)
AT26	PCIAD[17]	BIDIR	AD(31-0) address and data bus (1.5-3.3V)
AN25	PCIAD[18]	BIDIR	AD(31-0) address and data bus (1.5-3.3V)
AR25	PCIAD[19]	BIDIR	AD(31-0) address and data bus (1.5-3.3V)
AP33	PCIAD[2]	BIDIR	AD(31-0) address and data bus (1.5-3.3V)
AP25	PCIAD[20]	BIDIR	AD(31-0) address and data bus (1.5-3.3V)
AT25	PCIAD[21]	BIDIR	AD(31-0) address and data bus (1.5-3.3V)
AN24	PCIAD[22]	BIDIR	AD(31-0) address and data bus (1.5-3.3V)
AR24	PCIAD[23]	BIDIR	AD(31-0) address and data bus (1.5-3.3V)
AN23	PCIAD[24]	BIDIR	AD(31-0) address and data bus (1.5-3.3V)
AT24	PCIAD[25]	BIDIR	AD(31-0) address and data bus (1.5-3.3V)
AN22	PCIAD[26]	BIDIR	AD(31-0) address and data bus (1.5-3.3V)
AT23	PCIAD[27]	BIDIR	AD(31-0) address and data bus (1.5-3.3V)
AP22	PCIAD[28]	BIDIR	AD(31-0) address and data bus (1.5-3.3V)
AR22	PCIAD[29]	BIDIR	AD(31-0) address and data bus (1.5-3.3V)
AT33	PCIAD[3]	BIDIR	AD(31-0) address and data bus (1.5-3.3V)
AN21	PCIAD[30]	BIDIR	AD(31-0) address and data bus (1.5-3.3V)
AT22	PCIAD[31]	BIDIR	AD(31-0) address and data bus (1.5-3.3V)
AN32	PCIAD[4]	BIDIR	AD(31-0) address and data bus (1.5-3.3V)
AR32	PCIAD[5]	BIDIR	AD(31-0) address and data bus (1.5-3.3V)
AP32	PCIAD[6]	BIDIR	AD(31-0) address and data bus (1.5-3.3V)
AT32	PCIAD[7]	BIDIR	AD(31-0) address and data bus (1.5-3.3V)
AT31	PCIAD[8]	BIDIR	AD(31-0) address and data bus (1.5-3.3V)

BGA PAD	PIN NAME	TYPE	DESCRIPTION
AN30	PCIAD[9]	BIDIR	AD(31-0) address and data bus (1.5-3.3V)
AP31	PCICBEN[0]	BIDIR	C/BE Command Bus Byte Enables{1.5V-3.3v]
AT29	PCICBEN[1]	BIDIR	C/BE Command Bus Byte Enables{1.5V-3.3v]
AR26	PCICBEN[2]	BIDIR	C/BE Command Bus Byte Enables{1.5V-3.3v]
AP24	PCICBEN[3]	BIDIR	C/BE Command Bus Byte Enables{1.5V-3.3v]
AR15	PCIClk	IN	Clk PciClk (3.3v)
AR28	PCIDevSelN	BIDIR	DEVSEL# Device select[1.5V-3.3V]
AN26	PCIFrameN	BIDIR	Frame# Cycle Frame(3.3v)
AR16	PCIGntN	IN	Gnt# Grant (3.3v)
AM22	PCIIdSel	IN	
AT14	PCIIntAN	OUT	INTA# Interrupt A open drain
AT28	PCIIRdyN	BIDIR	IRDY# Initiator ready (3.3v)
AN28	PCIPar	BIDIR	PAR Parity (3.3v)
AT16	PCIReqN	OUT	REQ# Request[3.3v]
AR14	PCIRstN	IN	RST# Reset (3.3v)
AP28	PCIStopN	BIDIR	STOP# [3.3v]
AN27	PCITRdyN	BIDIR	TRDY# Target Ready[3.3v]
AR13	PLLAG[0]	POWER	PLL analogue ground = 0v (islolated from GND)
AM11	PLLAG[1]	POWER	PLL analogue ground = 0v (isolated from GND)
AN10	PLLAG[2]	POWER	PLL analogue ground = 0v (isolated from GND)
AT13	PLLVAA[0]	POWER	PLL analogue power = 3.3v
AP11	PLLVAA[1]	POWER	PLL analogue power 3.3v
AP10	PLLVAA[2]	POWER	PLL analogue power 3.3v
AN12	RefClkIn		
AL13	SBClk	BIDIR	
AL12	SBData	BIDIR	
AR 9	ScanEnable		
AL20	SENSEGND		
AL17	SENSEVCC1V2	PWR	1.20 vdc nominal
AL14	TestMode	IN	Production test global enable (Active high)
AM14	TestSelect[0]	IN	Production test mode select
AM13	TestSelect[1]	IN	Production test mode select
AL15	TestSelect[2]	IN	Production test mode select
U 3	VCC_DFP_1	PWR	3.30 vdc nominal
Y 6	VCC_DFP_2	PWR	3.30 vdc nominal
AA 1	VCC_DFP_3	PWR	3.30 vdc nominal
AB 6	VCC_DFP_4	PWR	3.30 vdc nominal
AD 3	VCC_DFP_5	PWR	3.30 vdc nominal
F 6	VCC1V2_1	PWR	1.20 vdc nominal
F29	VCC1V2_10	PWR	1.20 vdc nominal
F30	VCC1V2_11	PWR	1.20 vdc nominal
F31	VCC1V2_12	PWR	1.20 vdc nominal
AL31	VCC1V2_13	PWR	1.20 vdc nominal
G 6	VCC1V2_14	PWR	1.20 vdc nominal
G31	VCC1V2_15	PWR	1.20 vdc nominal
H 6	VCC1V2_16	PWR	1.20 vdc nominal
H31	VCC1V2_17	PWR	1.20 vdc nominal
J 6	VCC1V2_18	PWR	1.20 vdc nominal
J31	VCC1V2_19	PWR	1.20 vdc nominal
F 7	VCC1V2_2	PWR	1.20 vdc nominal
AD 6	VCC1V2_20	PWR	1.20 vdc nominal
AC31	VCC1V2_21	PWR	1.20 vdc nominal
AF 6	VCC1V2_22	PWR	1.20 vdc nominal
AE31	VCC1V2_23	PWR	1.20 vdc nominal

BGA PAD	PIN NAME	TYPE	DESCRIPTION
AH 6	VCC1V2_24	PWR	1.20 vdc nominal
AH31	VCC1V2_25	PWR	1.20 vdc nominal
AJ 6	VCC1V2_26	PWR	1.20 vdc nominal
AJ31	VCC1V2_27	PWR	1.20 vdc nominal
AK 6	VCC1V2_28	PWR	1.20 vdc nominal
AK31	VCC1V2_29	PWR	1.20 vdc nominal
F 8	VCC1V2_3	PWR	1.20 vdc nominal
AL 6	VCC1V2_30	PWR	1.20 vdc nominal
AL 7	VCC1V2_31	PWR	1.20 vdc nominal
AL 8	VCC1V2_32	PWR	1.20 vdc nominal
AL 9	VCC1V2_33	PWR	1.20 vdc nominal
AL16	VCC1V2_34	PWR	1.20 vdc nominal
AL21	VCC1V2_35	PWR	1.20 vdc nominal
AL26	VCC1V2_36	PWR	1.20 vdc nominal
AL28	VCC1V2_37	PWR	1.20 vdc nominal
AL29	VCC1V2_38	PWR	1.20 vdc nominal
AL30	VCC1V2_39	PWR	1.20 vdc nominal
F 9	VCC1V2_4	PWR	1.20 vdc nominal
F13	VCC1V2_5	PWR	1.20 vdc nominal
F14	VCC1V2_6	PWR	1.20 vdc nominal
F23	VCC1V2_7	PWR	1.20 vdc nominal
F24	VCC1V2_8	PWR	1.20 vdc nominal
F28	VCC1V2_9	PWR	1.20 vdc nominal
A 7	VCC2V5_1	PWR	3.30vdc nominal
F11	VCC2V5_10	PWR	3.30vdc nominal
F16	VCC2V5_11	PWR	3.30vdc nominal
F21	VCC2V5_12	PWR	3.30vdc nominal
F36	VCC2V5_13	PWR	3.30vdc nominal
H 2	VCC2V5_14	PWR	3.30vdc nominal
J33	VCC2V5_15	PWR	3.30vdc nominal
L31	VCC2V5_16	PWR	3.30vdc nominal
M 2	VCC2V5_17	PWR	3.30vdc nominal
M 6	VCC2V5_18	POWER	
U 2	VCC2V5_19	POWER	
A25	VCC2V5_2	POWER	
U 6	VCC2V5_20	POWER	
U31	VCC2V5_21	POWER	
V35	VCC2V5_22	POWER	
AF31	VCC2V5_23	POWER	
AG36	VCC2V5_24	POWER	
AJ36	VCC2V5_25	POWER	
AL32	VCC2V5_26	POWER	
AT36	VCC2V5_27	POWER	
A29	VCC2V5_3	POWER	
A36	VCC2V5_4	POWER	
B 1	VCC2V5_5	POWER	
B 4	VCC2V5_6	POWER	
B14	VCC2V5_7	POWER	
E 4	VCC2V5_8	POWER	
E32	VCC2V5_9	POWER	

BGA PAD	PIN NAME	TYPE	DESCRIPTION
AE 1	VDD_TTL_1	PWR	3.30 vdc nominal
AE 5	VDD_TTL_2	PWR	3.30 vdc nominal
AJ 1	VDD_TTL_3	PWR	3.30 vdc nominal
AJ 5	VDD_TTL_4	PWR	3.30 vdc nominal
AM 6	VDD_TTL_5	PWR	3.30 vdc nominal
AT 2	VDD_TTL_6	PWR	3.30 vdc nominal
AT10	VDD_TTL_7	PWR	3.30 vdc nominal
AN13	VDD_TTL_8	PWR	3.30 vdc nominal
AM18	VDDQ_1		3.3vdc
AM24	VDDQ_2		3.3vdc
AR34	VDDQ_3		3.3vdc
AT15	VDDQ_4		3.3vdc
AT21	VDDQ_5		3.3vdc
AT27	VDDQ_6		3.3vdc
AR 3	VidADDCClk		
AR 4	VidADDCData		
AP 1	VidAHSync	OUT	DAC Horizontal sync
AP 2	VidAVSync	OUT	DAC Vertical sync
AT 3	VidBDDCClk		
AT 4	VidBDDCData		
AR 1	VidBHSync		
AR 2	VidBVSync		
AT 8	VidInData[0]		
AT 7	VidInData[1]		
AR 7	VidInData[2]		
AR 6	VidInData[3]		
AP 6	VidInData[4]		
AN 6	VidInData[5]		
AT 5	VidInData[6]		
AR 5	VidInData[7]		
AP 5	VidInStrobe		
AN 9	VidLock[0]		
AP 9	VidLock[1]		
AT11	Xtal	BIDIR	External crystal connections

8.3 Ground Connections

GND designates pins where core and IO ground supply = 0v

The following pins are GND: AL27, A14, C31, AT 1, AT 6, AT 9, AT12, AT35, D 9, D12, D15, D18, E 2, E 5, E21, F10, F15, A23, F17, F20, F27, H 1, J35, K31, L 6, M 1, U 1, U 4, B 3, U 5, U33, V31, V36, W31, W34, AA 2, AB33, AD 4, AD 5, B 7, AD33, AE 2, AE 3, AE 4, AE 6, AE33, AF 4, AF35, AG31, AG32, B20, AG35, AH 2, AH 4, AH 5, AJ 2, AJ 3, AJ35, AK34, AK35, AL10, B26, AL18, AL19, AL22, AL23, AL24, AL25, AM 2, AM 4, AM 5, B35, AM 7, AM12, AM15, AM16, AM17, AM19, AM20, AM21, AM25, AM27, C 2, AM28, AM29, AM30, AM32, AN 1, AN 2, AN 3, AN 5, AN11, C 3, AN15, AP 3, AP 4, AP14, AP15, AP34, AP16, AR21, AR27, AR35.

8.4 Schematics

Refer to the supplied PDF or ZIP file for P10 Typical Board Layouts and Data.

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Memory

10 Reset

In earlier 3Dlabs bus interface designs, a number of parameters for the bus interface were initialised at reset time using pull-up or pull-down resistors connected to *configuration pins*. These pins were normally tri-state at reset, and their state was sampled on the trailing edge of reset. These configuration signals were then loaded into the *ChipConfig* register, which was used to control the initialisation and operation of the device. This approach becomes less practical as external signal speeds increase, and so this design loads all but the most critical initialisation information from the external Expansion ROM. Loading from the ROM is enabled using a single “RomConfig” configuration pin, and default initialisation values are used for registers when loading is disabled.

Following a hardware reset from the PCI Bus, the internal configuration state machine reads the 32-bit word at what would be the highest location in a 64KByte ROM, and interprets this as a pointer to a Configuration Table, as shown in the ROM Layout diagram below.

Note: The vector address is 0xFFFC but the offsets are in dwords.

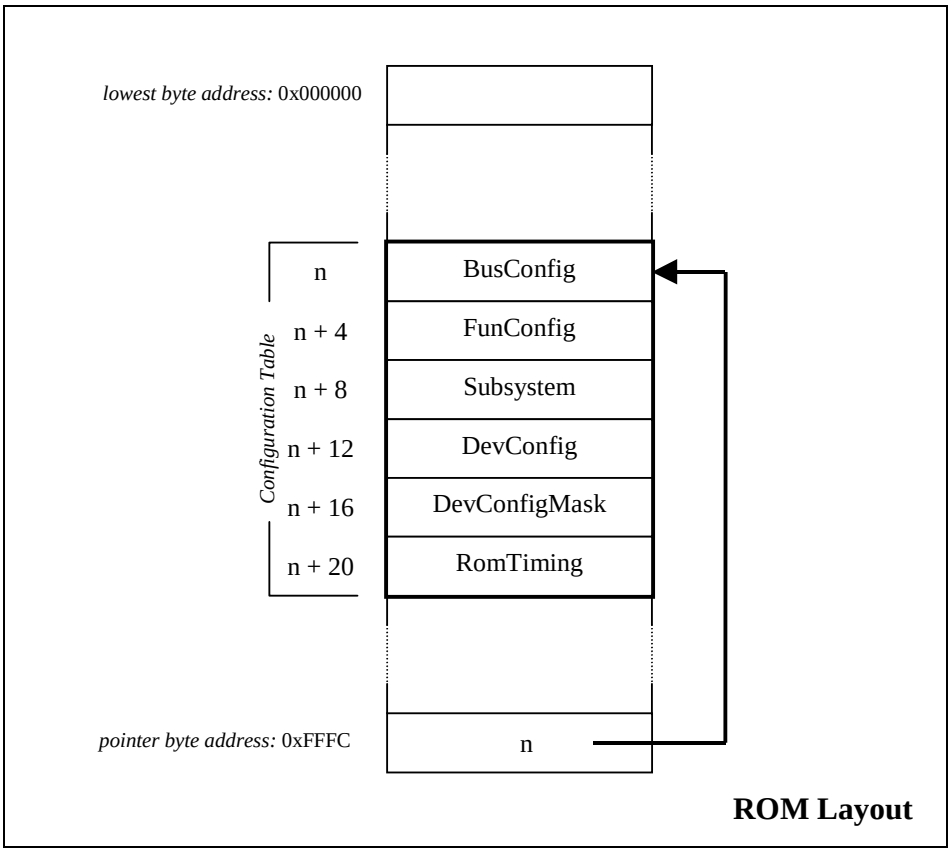

Figure 10.1 ROM Layout

Once the Configuration Table pointer has been read, a sequence of 32-bit words are loaded from it into configuration space registers in the PCI Config unit and control registers in the ROM Controller unit:

Table Offset	Table Field	Destination Unit	Destination Register
00h	BusConfig	PCI Config	CFGBusConfig
04h	FunConfig	PCI Config	CFGFunConfig
08h	Subsystem	PCI Config	CFGSubsystemID *and* CFGSubsystemVendorID
0Ch	DevConfig	PCI Config	CFGDevConfig
10h	DevConfigMask	PCI Config	CFGDevConfigMask
14h	RomTiming	ROM Controller	ROMTiming

The **CFGBusConfig**, **CFGFunConfig**, **CFGDevConfig**, and **CFGDevConfigMask** registers are described below. Each of these four user-defined registers is shared between all functions in a multi-function device, and accesses through any function are mapped to the same underlying register hardware by the bus interface.

10.1 RAMDAC Resets

RAMDAC signals are reset on either program soft resets or hard (power-on) reset, with exceptions. The following signals are reset following power-on only:

RDDClkSetup[1-2]
RDDClkControl
RDDClk0PreScale
RDDClk0FeedBackScale
RDDClk0PostScale
RDDClk1PreScale
RDDClk1FeedBackScale
RDDClk1PostScale
RDDClk2PreScale
RDDClk2FeedBackScale
RDDClk2PostScale
RDDClk3PreScale
RDDClk3FeedBackScale
RDDClk3PostScale
RDDKClkControl
RDKClkPreScale
RDKClkSetup[1-2]
RDKClkFeedBackScale
RDKClkPostScale
RDMClkControl
RDSClkControl
RDTClkControl
RDTClkPreScale
RDTClkFeedbackScale
RDTClkPostScale

Three phase locked loops (PLLs) are included in the RAMDAC unit, dedicated to generating DClk (Pixel clock) and a derived Video clock (VClk) as well as the Core and Timing (Kclk and TClk) Plls.

The DClk PLL has four sets of control registers (e.g. **RDDclk3Prescale**). The set selection is defined by two control bits from outside the unit.

The reset states for the DClk PLL control regsiters are:

Register set	Frequency
0	25.057MHz
1	28.278MHz
2	Undefined
3	Undefined

The KClk and TClk PLLs reset to approximately 50MHz. All figures assume a 14.31818MHz external reference.

An external signal can put the PLLs into bypass mode. In this mode Tclk, KClk and DClk are taken from pins and the PLLs have no effect.

11 Thermal

In operation, the P10 chip generates heat as a function of the power consumed, which in turn depends on frequency, the number of Texture pipes and other factors. This heat must be dissipated through the package to avoid exceeding the chip's design heat limit ($T_{j(max)}$, typically 125°C) and damaging the chip. This can be accomplished by improving thermal flow:

- through the chip (junction to ambient air, or θj_a) and
- from junction to top-of-case (θj_c).

These figures describe thermal resistance – lower is better. The top-of-case figure is significant where heatsinks are considered.

11.1 Thermal Performance

The thermal performance of the chip is described in JEDEC standard JESD 51-2, 51-6:

$\theta_{ja} = (T_j - T_a) / P_h$

$\theta_{jc} = (T_j - T_c) / P_h$

where:

- Junction Temperature = Tj
- Ambient Temperature = Ta
- Top-of-case Temperature = Tc
- Power Dissipation = Ph

Working assumptions are:

Maximum Power Dissipation (provisional)	$P_{h(max)}$	=	8 Watts
Maximum Junction Temperature	$T_{j(max)}$	=	125 °C.
Nominal memory clock frequency	f_{MClk}	=	TBA (MHz DDR)
Nominal core clock frequency	f_{KClk}	=	TBA (MHz)

11.2 Thermal Resistivity Equations

These are taken from Ellison's *Thermal Computations for Electronic Equipment.*[1]

11.2.1 Natural Convection

$$h_c = 0.83 f \left(\frac{\Delta T}{L_{ch}} \right)^n (W / m^2 - {}^0C)$$

where ΔT is the temperature difference in C^0, and the constants f and n are given as

f =1.22 and n = 0.35 for a vertical plate;

f=1.00 and n = 0.33 for a horizontal plate facing upward; and

f =0.50 and n =0.33 for a horizontal plate facing downward

L_{ch} is the characteristic length in meters.

For a horizontal plate, $L_{ch} = \frac{WL}{2(W + L)}$

For a vertical plate, $L_{ch} = H$

where W, H and L are the width, height and length of the plate, respectively

1 G. N. Ellison, Thermal Computations for Electronic Equipment, R. E. Krieger Publishing Company, Malabar, FL., 1989.

11.2.2 Forced convection

$$h_c = 3.786(V/L)^{1/2} \quad (W/m^2 -^0 C)$$

where V is the air speed in m/s, and L is the total length in meters in the flow direction.

Data shown below are provisional for P10 pending the availability of actual test results.

820L HSBGA	Thermal Resistance				
	(deg.C/Watt) = θ_{ja}			Psi jt (C/W)	θ_{jc} C/W
	0 m/s	*1 m/s*	*2 m/s*		
No heatsink, 4L PCB	10.3	9.2	7.9	1.2	2.1
No heatsink, 4L PCB with 2oz. Copper plane	9.9	8.8	7.5	1.1	2.0
Heatsink (37mm sq.x 6mm such as AAVID 373324)	9.3	6.7	5.4		

Table 10-1 P10 Package (820L HSBGA) Thermal Performance

11.3 Cooling

From this analysis, relying on natural convection alone the junction temperature increases 90.4°C under normal operating conditions. Given a maximum junction temperature of 125°C the maximum ambient would be 34.6°C. This is in practice inadequate without air circulation and a heatsink would normally be recommended.

11.4 Operation with Heatsink

11.4.1 Heatsink Attachment

The following method has been approved for the purpose of attaching a heatsink directly onto the HSBGA package:

Thermally conductive epoxy using either Loctite Output 315 with Loctite 7386 or type EG 7655 from A.I. Technology Inc. The thickness of the epoxy layer should be between 0.05mm and 0.15mm with 95% coverage of the contact area.

Typical achievable θ_{cs} using this method is 1.0 °C/Watt

11.4.2 Calculating cooling requirements

With a heatsink attached to the device the junction temperature will depend on θcs and θsa where θcs is the thermal resistance of the join between the heatsink and the case and θsa is the thermal resistance of the heatsink, which will be a function of system airflow. Typically,

$$Tj = Ta + Pd\ (\theta_{jt} + \theta_{cs} + \theta_{sa})$$

11.4.3 Temperature Range (Commercial/Embedded Applications)

P10 is operational in embedded use under a wide range of ambient air temperatures:

- Storage Range: -65°C to 150°C (suitably packed)
- Operating Range: 0°C to $T_{j(max)}$ [2]

[2] The operating range minima and maxima depend on the cooling configuration and whether any warm-up period is allowed. The chip will not boot at -5°C junction temperature. However with sufficient warmup or during continuing operation the thermal resistance would allow reliable operaton under much colder ambient conditions. Similarly with a suitable fan the ambient temperature could be as much as 81°C or higher without exceeding $T_{j(max)}$.

12

Electrical

Provisional values may be subject to change and should be checked against current values on the 3Dlabs website[3].

Note: SSTL VCC2V5, P VDDQ and others are capable of dual voltage operation. This shows standard TTL level for simplicity.

12.1 Absolute Maximum Ratings

Junction Temperature	**125°C**
Storage Temperature	-65°C to 150°C
Operating Temperature	0°C to $T_{j(max)}$ (=125°C) [4]
VDD_TTL, VCC_DFP, VCC2.5 DC Supply Voltages	3.6vdc [5]
VCC1.2 DC Supply Voltage	1.32vdc
VDDQ, PLLVAA, DacVAA, AGP3V3 DC Supply Voltages	3.6vdc [6]
SSTL_Vref	VCC2V5/2
DFP_Vref	VCC_DFP/2
DacVREF, DacComp, DacFSAdj	Open
AGPVREF	VDDQ/2
I/O Pin Voltage with respect to GND	-0.5V to VDDQ + 0.3V

12.2 DC Specifications

Symbol/ PAD	**Parameter**	**Min**	**Nominal**	**Unit**
GND	Ground	0.00	0.00	Vdc
VCC1V2	Power at 1.20 vdc	1.08	1.20	Vdc
VDD_TTL	TTL Logic feed at 3.30 vdc	3.00	3.30	Vdc
VCC_DFP	DFP power at 3.30 vdc	3.00	3.30	Vdc
VCC2V5 VDDQ PLLVAA DacVAA AGP3V3	Power at 3.20 vdc	3.00	3.30	Vdc
SSTL_VRef	VCC2V5/2	1.5	1.8	Vdc
DFP_Vref	VCC_DFP/2	1.5	1.8	Vdc
DacVRef DacCOMP DacFSAdj		Open	Open	Vdc
AGPVRef	VDDQ / 2		VDDQ / 2	
LPIN	Pin Inductance		2.807	nH
	Pin Capacitance		0.6023	pF

[3] At: http://www.3dlabs.com

[4] This is the maximum junction temperature – normally maximum ambient temperature will be much lower. Maximum ambient temperature depends on thermal path characteristics such as heatsink and air flow.

[5] SSTL VCC2V5 is capable of dual voltage operation. This shows standard TTL level for simplicity.

[6] AGP VDDQ is capable of dual voltage operation. This shows standard TTL level for simplicity.

	Pin Resistance		107	mOhm
ICC (3V)	Power Supply Current			A
ICC (2.5V)	Power Supply Current			A

12.2.1 PCI Signal DC Specifications

Symbol	Parameter	Min	Max	Unit
V_{PIL}	Input Low Voltage			V
V^{PIH}	Input High Voltage			V
V_{POL}	Output Low Voltage			V
V_{POH}	Output High Voltage			V
I_{PIL}	Input Low Current			UA
I_{PIH}	Input High Current			UA
C_{PIN}	Input Capacitance			PF
C_{CLK}	PCI Clock Input Capacitance			PF
C_{IDSEL}	PCI Idsel Input Capacitance			PF

12.2.2 Non-PCI Signal DC Specifications

Symbol	Parameter	Min	Max	Unit
V_{IL}	Input Low Voltage		--	V
V_{IH}	Input High Voltage	-		V
V_{OL}	Output Low Voltage	0.4	0.4	V
V_{OH}	Output High Voltage	2.5	3.1	V
I_{OH}	Input Low Current	-4 [-8]	-4 [-8]	uA

12.3 SSTL_2 Class I Signals (DDR Memory Interface Only)

Symbol	Parameter	Min	Max	Units
IOL	Low Level Output Current	4 [8]	4 [8]	mA
IOH	High Level Output Current		16	mA
IIL	Low Level Input Current		2	uA
IIH	High Level Input Current		2	uA
Cin	Input Capacitance		20	pF

12.4 AC Specifications

Pin Name	Capacitive Load
PCIAD[31:0], PCICBEN[3:0], PCIPar, PCIFrameN,PCIIRdyN, PCITRdyN, PCIStopN, PCIIdsel, PCIDevselN, PCIReqN, PCIGntN, PCIIntAN ,AGPPipeN, AGPRbfN, AGPSBA[7:0],	
All other outputs	

12.4.1 Clock Timing

Symbol	Parameter	Min	Max	Units	Notes
T_{PCyc}	PCIClk Cycle Time		-	ns	
T_{PHigh}	PCIClk High Time	-	-	ns	
T_{SLow}	PCIClk Low Time	-	-	ns	
T_{MCyc}	MClkin Cycle Time		-	ns	
T_{MHigh}	MClkin High Time	-	-	ns	
T_{MLow}	MClkin Low Time	-	-	ns	
T_{SCyc}	SClkin Cycle Time		-	ns	
T_{SHigh}	SClkin High Time		-	ns	

T_{SLow}	SClkin Low Time		-	ns	
T_{DCyc}	DClk Cycle Time		-	ns	
T_{DHigh}	DClk High Time	-	-	ns	
T_{DLow}	DClk Low Time	-	-	ns	

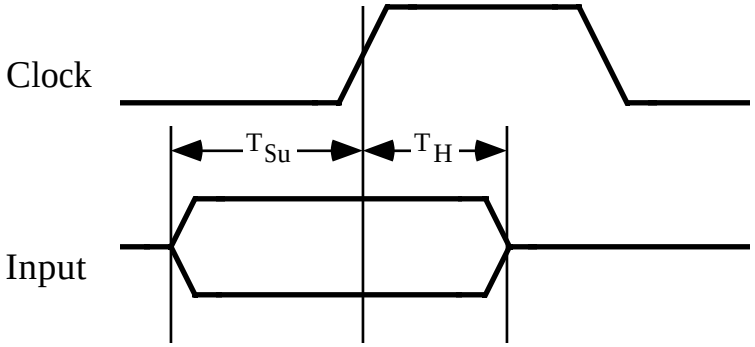

Figure 12.1 Input Timing Parameters

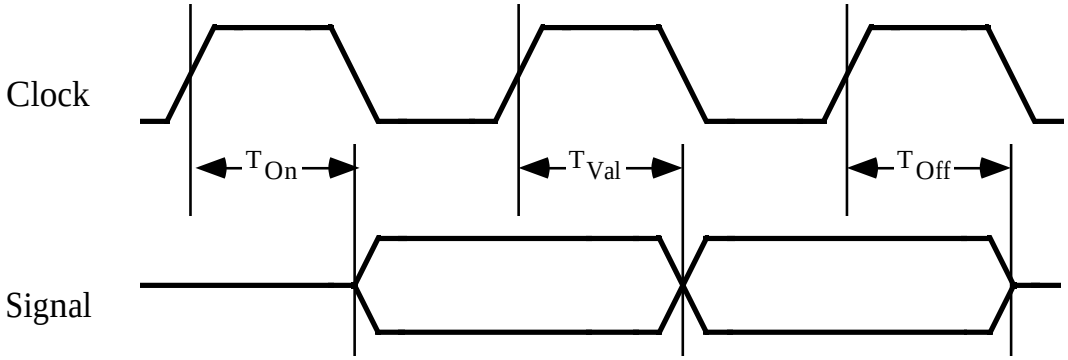

Figure 12.2 Output Timing Parameters

12.4.2 PCI Clock Referenced Input Timing

Parameter	T_{Su} Min	T_H Min	Units
PCIAD(31:0), PCICBEN(3:0), PCIPar, PCIFrameN, PCIIRdyN, PCITRdyN, PCIStopN, PCIIdsel, PCIDevselN, AGPSt0-2			ns
PCIGntN			ns
PCIRstN			ns

Note: PCIRstN is resynchronised internally. The timings given, when met, ensure that the reset is detected in the current cycle.

12.4.3 PCI-Referenced Output Timing

	T_{Val}		T_{On}		T_{Off}		
Parameter	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Units**
PCIAD(31:0), PCICBEN(3:0), PCIPar, PCIFrameN, PCIIRdyN, PCITRdyN, PCIStopN, PCIIdsel, PCIDevselN							ns
PCIReqN							ns
PCIIntAN							ns

Note: Timings given are for falling edges of the open drain signal. Rise times are dependent on the external pull-up resistor.

12.4.4 AGP Referenced Output Timing

	T_{Val}		T_{On}		T_{Off}		
Parameter	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Units**
PCIAD(31:0), PCICBEN(3:0), PCIPar, PCIFrameN, PCIIRdyN, PCITRdyN, PCIStopN, PCIIdsel, PCIDevselN							ns
PCIReqN							ns
PCIIntAN							ns

Note: Timings given are for falling edges of the open drain signal. Rise times are dependent on the external pull-up resistor.

12.4.5 MEMCKOUT Referenced Input Timing

All timings below are with respect to MEMCKOUT, which is a delayed version of MClk.

Parameter	**TSu Min**	**TH Min**	**Units**
MDAT[63:0]			ns

12.4.6 MEMCKOUT Referenced Output Timing

All timings below are with respect to MEMCKOUT, which is a delayed version of MClk.

	T_{Val}		T_{On}		T_{Off}			
Parameter	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Units**	**Notes**
All memory control, data and address lines							ns	

13

Errata and Alerts

Alerts are part of 3Dlabs' commitment to providing comprehensive and useful information about chipset products. Alerts describe issues arising when the chip is used outside normal operating parameters and may be of interest to driver programmers.

13.1 ALERT001

13.1.1 Problem

When handling a page fault, the fault data is recovered from the MemoryPageControlFIFO with the **FaultID** in word 0, bit positions as follows:

0 – graphics process
1 – VGA
2 – command
3 – bypass
4 – page handler
5 – translation lookaside buffer
6 – video 0
7 – video 1

However the bitmask used to Suspend or Restart an addressing source has bits 1 and 2 reversed.

13.1.2 Software Workaround

There are no functional implications if the programmer remembers to swap the Suspend mask *VGA* and *command* bit positions.

13.2 P10ERN001

13.2.1 Problem

When using the **Restart** mask in operations such as Table Update Page DMA etc. where commands are sent to the memory controller's MemoryPageControlFifo, a **Suspend** mask must also be used. The **Suspend** mask must include reference to every currently suspended source.

13.2.2 Software Workaround

Use a Suspend mask as appropriate.

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