

I-128 Series 4 (SilverHammer)

High-Performance

128-Bit Graphics and

Multimedia Processor

Technical Reference Manual



Number Nine Visual Technology

©1998 Number Nine Visual Technology Corporation, all rights reserved.



Contents

Notice	ii
Trademarks	ii
Copyrights.....	ii

Section 1: General Information

1.1 Overview.....	1-2
1.2 Key Device Features.....	1-2

Section 2: Functional Description

2.1 Overview.....	2-2
2.2 Addressing Scheme	2-3
2.2.1 Display Buffer	2-3
2.2.2 Virtual Buffer	2-3
2.3 Register Map	2-4
2.3.1 I/O Mapped VGA DAC Registers	2-4
2.3.2 I/O Mapped Configuration Registers	2-4
2.3.3 Memory Mapped Global Registers	2-6
2.3.4 Memory Mapped Global Control Registers.....	2-7
2.3.5 Memory Windows Registers	2-8
2.3.6 Memory Mapped Drawing Registers.	2-9
2.4 Diagram	2-12
2.5 Coordinate System.....	2-14

Section 3: IMAGINE 128[™] I/O Information

3.1 Signal Descriptions.....	3-2
3.2 Pin Assignments.....	3-6
3.2.1 Imagine 128 [™] (Bottom View)	3-18
3.3 EDO Configuration (TopView).....	3-19
3.4 SGRAM Configuration (TopView)	3-20
3.5 WINDOW RAM Configuration (Top View)	3-21
3.6 Configuration Pins.....	3-22

Section 4: PCI Configuration

4.1 PCI Configuration Space	4-2
4.2 IMAGINE 128 [™] PCI Registers	4-2
4.2.1 PCI Configuration Register 0	4-2
4.2.2 PCI Configuration Register 1	4-4
4.2.3 PCI Configuration Register 2	4-5
4.2.4 PCI Configuration Register 3	4-5
4.3 IMAGINE 128 [™] PCI Base Address Registers	4-6
4.3.1 PCI Base Address Register 0	4-8
4.3.2 PCI Base Address Register 1	4-8
4.3.3 PCI Base Address Register 2.....	4-9
4.3.4 PCI Base Address Register 3.....	4-9
4.3.5 PCI Base Address Register 4.....	4-10
4.3.6 SUBSYSTEM ID/SUBSYSTEM VENDOR ID.....	4-10
4.3.7 PCI ROM Base Address Register	4-11
4.3.8 Capabilities Register	4-11
4.3.9 PCI Configuration Register 4	4-12
4.3.10 Capabilities ID.....	4-12
4.3.11 AGP Status.....	4-13
4.3.12 AGP Command.....	4-13

Section 5: Register Set

5.1	Addressing Configuration Registers.....	5-2
5.1.1	Register Base Address for the Global Register Block.....	5-2
5.1.2	Memory Windows Register Block Base Address Register.....	5-3
5.1.3	Register Base Address Drawing Engine.....	5-3
5.1.4	Register Base Address Global Interrupt Registers.....	5-4
5.1.5	Register Base Address/Size EPROM Registers.....	5-4
5.2	VGA DAC Shadow Registers.....	5-5
5.2.1	Pixel Mask Registers.....	5-5
5.2.2	Read Address Register.....	5-5
5.2.3	Write Address Register.....	5-6
5.2.4	Palette Data Register.....	5-6
5.3	Miscellaneous I/O Registers.....	5-7
5.3.1	ID Register.....	5-7
5.3.2	Configuration Register One.....	5-10
5.3.3	Configuration Register Two.....	5-11
5.3.4	SGRAM Configuration Register.....	5-15
5.3.5	Soft Switch Register.....	5-18
5.3.6	DDC Register.....	5-19
5.4	Global Interrupt Registers.....	5-20
5.4.1	Global Interrupt Registers.....	5-20
5.4.2	Global Interrupt Mask Register.....	5-20
5.5	DMA Registers.....	5-21
5.5.1	DMA Source Register.....	5-21
5.5.2	DMA Destination Address.....	5-21
5.5.3	DMA Command.....	5-21
5.6	PCI Bus Master Registers.....	5-23
5.6.1	PCI Bus Master Write Address.....	5-23
5.6.2	PCI Bus Master Trigger Mask.....	5-23
5.7	RAM DAC Registers.....	5-25
5.7.1	Write Address Register.....	5-25
5.7.2	Palette Data Register.....	5-25
5.7.3	Pixel Mask Registers.....	5-25
5.7.4	Read Address Register.....	5-26
5.7.5	DAC Register 4.....	5-26
5.7.6	DAC Register 5.....	5-26
5.7.7	DAC Register 6.....	5-27
5.7.8	DAC Register 7.....	5-23
5.7.9	DAC Register 8.....	5-23
5.7.10	DAC Register 9.....	5-24
5.7.11	DAC Register 10.....	5-24
5.7.12	DAC Register 11.....	5-24
5.7.13	DAC Register 12.....	5-25
5.7.14	DAC Register 13.....	5-25
5.7.15	DAC Register 14.....	5-25
5.7.16	DAC Register 15.....	5-26
5.6	CRT Registers.....	5-27
5.6.1	Vertical Interrupt Count Register.....	5-27
5.6.2	Horizontal Interrupt Count Register.....	5-27
5.6.3	CRT Display Start Address.....	5-28
5.6.4	Display Buffer Pitch.....	5-29
5.6.5	CRT Horizontal Active Line.....	5-29
5.6.6	CRT Horizontal Blank Width.....	5-30
5.6.7	CRT Horizontal Front Porch Width.....	5-30
5.6.8	CRT Horizontal Sync Width.....	5-30

5.6.9	CRT Vertical Field Active.....	5-31
5.6.10	CRT Vertical Blank Width.....	5-31
5.6.11	CRT Vertical Front Porch Width.....	5-32
5.6.12	CRT Vertical Sync Width.....	5-32
5.6.13	CRT Line Counter.....	5-33
5.6.14	CRT Display Buffer Zoom Factor.....	5-34
5.6.15	CRT Configuration Register 1.....	5-35
5.6.16	CRT Configuration Register 2.....	5-36
5.7	Memory Windows Configuration Registers.....	5-38
5.7.1	Memory Window Control Register.....	5-38
5.7.2	Memory Window Address Registers.....	5-42
5.7.3	Memory Window Size.....	5-43
5.7.4	Memory Window Origin.....	5-44
5.7.5	Memory Window Plane Mask.....	5-45
5.7.6	Memory Window Cache Flush Counter.....	5-46
5.7.7	Memory Window Flush Trigger.....	5-46
5.7.8	YUV LUT Index Register.....	5-47
5.7.9	YUV LUT Data Register.....	5-48
5.7.10	Memory Window Shared Control Register.....	5-48
5.8	Drawing Engine Command and Parameter Registers.....	5-49
5.8.1	Interrupt Register.....	5-49
5.8.2	Interrupt Mask Register.....	5-49
5.8.3	Flow Control Register.....	5-50
5.8.4	BUSY Register.....	5-51
5.8.5	XY Window Address.....	5-51
5.8.6	Buffer Control Register.....	5-52
5.8.7	Drawing Engine Source Origin.....	5-56
5.8.8	Drawing Engine Destination Origin.....	5-57
5.8.9	DE Source Source Pitch.....	5-57
5.8.10	DE Source Pitch.....	5-58
5.8.11	DE Destination Pitch.....	5-58
5.8.12	Command Register.....	5-59
5.8.13	Command Opcode.....	5-59
5.8.14	Command Raster Operation.....	5-60
5.8.15	Line/Fill Style Register.....	5-61
5.8.16	Patterning Register.....	5-62
5.8.17	Clipping Control Register.....	5-63
5.8.18	Host Data Format Register.....	5-63
5.8.19	Foreground.....	5-64
5.8.20	Background.....	5-64
5.8.21	Plane Mask.....	5-65
5.8.22	Raster Operation Mask.....	5-65
5.8.23	Line Pattern Register.....	5-65
5.8.24	Line Pattern Control Register.....	5-66
5.8.25	Top Left of Clip Area.....	5-67
5.8.26	Bottom Right of Clip Area.....	5-67
5.8.27	Drawing Engine Z Origin.....	5-68
5.8.28	Drawing Engine MipMap Origin.....	5-68
5.8.29	Drawing Engine Palette Origin.....	5-69
5.8.30	HITHER Clip Plane.....	5-69
5.8.31	YON Clip Plane.....	5-69
5.8.32	Fog Color Register.....	5-70
5.8.33	Alpha Register.....	5-70
5.8.34	Command Register.....	5-71
5.8.35	Command Register.....	5-72
5.8.36	3D Control Register.....	5-74

5.8.37	Texture Mapping Control Register	5-76
5.8.38	3D Command Trigger Register.....	5-79
5.8.39	OpenGL Blend Color Register.....	5-79
5.8.40	XY Parameter Registers	5-79
5.8.41	CP Parameter Registers	5-80
5.9	Display List Processor Registers	5-80
5.9.1	Display List Processor Address Register	5-80
5.9.2	Display List Processor Control Register.....	5-81
5.9.3	Display List Instruction Word, Format Zero No DMA	5-82
5.9.4	Display List Instruction Word, Format Zero DMA.....	5-83
5.9.5	Display List Instruction Word, Format Zero Text.....	5-84
5.9.6	Text Table Format.....	5-85
5.9.7	Display List Instruction Word, Format One.....	5-86
5.9.8	DLP Notes	5-86

Section 6: Drawing Engine Command Set

6.1	Noop.....	6-2
6.2	BITBLT	6-4
6.2.1	XY4 Register Zoom Data Format	6-6
6.3	LINE.....	6-7
6.4	PLINE.....	6-9
6.5	Line with Initial Error.....	6-11
6.6	3D Lines with Setup	6-13
6.7	3D Triangle with Full Setup and Vertex Sorting.....	6-16
6.8	Load Texture.....	6-20
6.9	Load Texture Palette.....	6-22
6.10	Read Transfer	6-24
6.11	Write Transfer	6-26

Appendix A: Imagine 128[™] Theory of Operation

A.1	Buffer Control.....	A-2
A.2	Linear Memory Windows Operation.....	A-3
A.3	X-Y Windows Operation.....	A-4
A.3.1	XY Registers for X-Y Windows	A-5
A.3.2	Drawing Parameter Registers for X-Y Windows	A-6
A.3.3	XY Window Example	A-7
A.4	Control of the Command Pipeline.....	A-8
A.5	Draw Style and Patterning	A-10
A.6	Fill Style and Patterning	A-11
A.7	Display List Processor.....	A-11
A.8	Texel Cache.....	A-12
A.8.1	TC Sizes	A-12
A.8.2	Texture Formats	A-13
A.8.3	Special Commands.....	A-13
A.9	Blending.....	A-13
A.10	Programming Imagine 128 [™] , 3D Operations	A-14
A.10.1	Control and Mode Setup.....	A-14
A.10.2	Parameter Load.....	A-15
A.10.3	Trigger.....	A-15
A.11	3D Operational Modes and Control	A-16
A.11.1	Gouraud Shading Mode.....	A-16
A.11.2	Specular Highlighting Mode.....	A-16
A.11.3	Z Buffer Mode	A-16
A.11.4	Fog Mode	A-17
A.11.4.1	Vertex Fog Mode.....	A-17
A.11.4.2	Table Fog Mode.....	A-17



A.11.5	Alpha Modes and Control	A-17
A.11.5.1	Alpha Comparison	A-17
A.11.5.2	Alpha Select, Alpha Modulation and Alpha Blend Select.....	A-18
A.11.5.3	Decal Alpha Mode	A-18
A.11.6	Rectangle Mode	A-18
A.11.7	Dither Mode	A-18
A.11.8	Backface Cull Mode.....	A-19
A.11.9	Texture Map Modes and Control	A-19
A.11.9.1	Texture Map	A-19
A.11.9.2	MipMap Modes	A-19
A.11.9.3	Texture Modes.....	A-19
A.11.9.4	Texture Image Pixel Format	A-20
A.11.10	Pixel Color Table A-20
A.11.11	OpenGL Compatibility.....	A-20
 Appendix B: External Interfaces		
B.1	RAM DAC	B-2
B.2	Soft Switches.....	B-3
B.3	EPROM	B-4
 Appendix C: Imagine 128[™] Programming Examples		
C.1	Programming Imagine 128 [™] 3D Operations.....	C-2
 Appendix D: Imagine 128[™] VGA Specification		
D.1	Internal VGA.....	D-2
D.1.1	Supported Modes	D-2
D.2	IMAGINE [™] VGA Architecture	D-3
D.2.1	Imagine [™] VGA Architecture	D-4
D.2.2	Imagine [™] VGA Operation.....	D-4
D.2.3	VGA Decode.....	D-5
 Appendix E: Imagine 128[™] Errata		
E.1	Errata	E-2