3

IMAGINE 128 I/O Information

Section 3: IMAGINE 128™ I/O Information

3.1 Signal Descriptions

IMAGINE 128™ signal pins are categorized into the following five groups: **PCI/AGP Bus Interface, Display Buffer Interface, Peripheral Devices Interface, CRT Control**, and miscellaneous. The "#" indicates an active low signal.

PCI/AGP BUS INTERFACE SIGNALS

NAME	I/O	DESCRIPTION
AD[31:0]	I/O	Multiplexed address and data bus
C_BE[3:0]	I/O	Command and Byte enables
HCLK	I	Host Bus Clock
RST#	I	System Reset
FRAME#	I/O	PCI cycle FRAME
PRDY#	I/O	Processor Ready (IRDY#, Initiator Ready)
TRDY#	I/O	Target Ready
DEVSEL#	I/O	PCI Device Select
STOP#	I/O	PCI cycle stop
INTRP#	O	Interrupt Pin
PAR	I/O	PCI Parity indicator
IDSEL	I	PCI Configuration Select
REQ#	O	Request bus mastering
GNT#	I	Grant bus mastering

DISPLAY BUFFER CONTROL SIGNALS

The local memory buffers of Imagine4 may be built using one of two types of memory:

WINDOW RAM
SGRAM

Names and/or function of some signals in this group change accordingly with selected type of memories.

Window RAM configuration:

NAME	I/O	DESCRIPTION
MCLK	I	Memory Controller Clock
RAD [8:0]	O	Display Buffer Address
PDAT [127:0]	I/O	Display Buffer Data Bus
RAS# [3:0]	O	Display Buffer Row Address Strobes
BEL# [15:0]	O	Display Buffer Low Byte Enable
BEH# [15:0]	O	Display Buffer High Byte Enable (Used only with Interleaved WRAM)
CAS#	O	Display Buffer Column Address Strobes
OE#_SF	O	Output enable for Display Buffer
SF[2:0]	O	Display Buffer Special Function Signal
SOE# [3:0]	O	Display Buffer Serial Output enable

SGRAM configuration:

NAME	I/O	DESCRIPTION
MCLK	I	Memory Controller Clock
RAD [10:0]	O	Display Address RAD[9] is used as SGRAM bank select
PDAT [127:0]	I/O	Display Buffer Data Bus
CS# [3:0]	O	Display Buffer Chip Select D_SC#[3:2] are used as RAD[11:10] in case of 16Mbit SGRAM
DQM# [15:0]	O	Display Buffer Byte Enable
CJ[15:0]	I	Placeholders for SGRAM only.
WE#	O	Display_Buffer Write Enable
DSF	O	Display Buffer Special Function Signal
RAS#	O	Display Buffer Row Address Strobe Enable
CAS#	O	Display Buffer Column Address Strobe Enable
PWE#	O	Peripheral Write Enable
POE#	O	Peripheral Output Enable

PERIPHERAL DEVICES CONTROL SIGNALS

NAME	I/O	DESCRIPTION
PA [7:0]	O	Address
PD [7:0]	I/O	Data Bus
PWE#	O	Write Strobe
POE#	O	EPROM Output Enable
PCS#	O	EPROM Chip Select
PWR#	O	Peripheral Port (DAC) Write
PRD#	O	Peripheral Port (DAC) Read
PSFT	O	Load Soft Switch

CRT CONTROLLER SIGNALS

NAME	I/O	DESCRIPTION
VCLK	I	Video Timing Clock
SCLK	I/O	Serial Clock
HSYNC	O	Horizontal Sync
VSYNC	O	Vertical Sync
CBLANK	O	Composite Blank
DDC_DAT	I/O	DDC Data to/from monitor (SDA)
DDC_CLK	I/O	DDC clock (SCL)
EXV#	I	Enable External Video
LD_CLK	O	RAMDAC Load Clock
DDAT[31:0]	O	DRAM Controller/ VGA data

MISCELLANEOUS SIGNALS

NAME	I/O	DESCRIPTION
DECLK	I	Drawing Engine Clock
VCSEL	0	VGA Clock Frequency Select
TOUT	O	Factory Test

3.2 Pin Assignments

IMAGINE 128™ is packaged in a 388 pin Plastic Ball Grid Array (PBGA).

NAME	NUMBER	I/O	DRIVE (mA)
AD [31]	C10	I/O	
AD [30]	A9	I/O	
AD [29]	D8	I/O	
AD [28]	B8	I/O	
AD [27]	A7	I/O	
AD [26]	D7	I/O	
AD [25]	B7	I/O	
AD [24]	A5	I/O	
AD [23]	C6	I/O	
AD [22]	D5	I/O	
AD [21]	B5	I/O	
AD [20]	B1	I/O	
AD [19]	C1	I/O	
AD [18]	C2	I/O	
AD [17]	D1	I/O	
AD [16]	D3	I/O	
AD [15]	G1	I/O	
AD [14]	G2	I/O	
AD [13]	G3	I/O	
AD [12]	G4	I/O	
AD [11]	H1	I/O	
AD [10]	H2	I/O	
AD [09]	H3	I/O	
AD [08]	J1	I/O	
AD [07]	J4	I/O	
AD [06]	K1	I/O	
AD [05]	K2	I/O	
AD [04]	K3	I/O	
AD [03]	K4	I/O	

NAME	NUMBER	I/O	DRIVE (mA)
AD [02]	L1	I/O	
AD [01]	L2	I/O	
AD [00]	G4	I/O	
C_BE [3]	A6	I	
C_BE [2]	D2	I	
C_BE [1]	F3	I	
C_BE [0]	J2	I	
HCLK	C11	I	
RST#	D12	I	
FRAME#	E2	I	
PRDY#	E1	I	
TRDY#	E4	O	
DEVSEL#	E3	O	
INTRP#	C8	O	
STOP#	F1	O	
PAR	F2	O	
IDSEL	B4	O	
REQ#	C9	O	
GNT#	F3	I	
MCLK	F26	I	
RAD [9]	D18	O	12
RAD [8]	K26	O	12
RAD [7]	L26	O	12
RAD [6]	M26	O	12
RAD [5]	N26	O	12
RAD [4]	P26	O	12
RAD [3]	AE26	O	12
RAD [2]	AD26	O	12
RAD [1]	AC26	O	12
RAD [0]	AB26	O	12
PDAT [127]	R25	I/O	4
PDAT [126]	R24	I/O	4
PDAT [125]	R23	I/O	4

NAME	NUMBER	I/O	DRIVE (mA)
PDAT [124]	T24	I/O	4
PDAT [123]	T25	I/O	4
PDAT [122]	T26	I/O	4
PDAT [121]	U24	I/O	4
PDAT [120]	U23	I/O	4
PDAT [119]	AD22	I/O	4
PDAT [118]	AF23	I/O	4
PDAT [117]	AF24	I/O	4
PDAT [116]	AE22	I/O	4
PDAT [115]	AE23	I/O	4
PDAT [114]	AE24	I/O	4
PDAT [113]	AD23	I/O	4
PDAT [112]	AD25	I/O	4
PDAT [111]	AF21	I/O	4
PDAT [110]	AE21	I/O	4
PDAT [109]	AD21	I/O	4
PDAT [108]	AF20	I/O	4
PDAT [107]	AE20	I/O	4
PDAT [106]	AD20	I/O	4
PDAT [105]	AC20	I/O	4
PDAT [104]	AE19	I/O	4
PDAT [103]	AE11	I/O	4
PDAT [102]	AF11	I/O	4
PDAT [101]	AE12	I/O	4
PDAT [100]	AD12	I/O	4
PDAT [99]	AC12	I/O	4
PDAT [98]	AD13	I/O	4
PDAT [97]	AE13	I/O	4
PDAT [96]	AF14	I/O	4
PDAT [95]	AD11	I/O	4
PDAT [94]	AE10	I/O	4
PDAT [93]	AD10	I/O	4
PDAT [92]	AC9	I/O	4

NAME	NUMBER	I/O	DRIVE (mA)
PDAT [91]	AD9	I/O	4
PDAT [90]	AE9	I/O	4
PDAT [89]	AF9	I/O	4
PDAT [88]	AE8	I/O	4
PDAT [87]	AC1	I/O	4
PDAT [86]	AB2	I/O	4
PDAT [85]	AB3	I/O	4
PDAT [84]	AB4	I/O	4
PDAT [83]	AC2	I/O	4
PDAT [82]	AC3	I/O	4
PDAT [81]	AD1	I/O	4
PDAT [80]	AD2	I/O	4
PDAT [79]	AA3	I/O	4
PDAT [78]	AA2	I/O	4
PDAT [77]	AA1	I/O	4
PDAT [76]	Y4	I/O	4
PDAT [75]	Y3	I/O	4
PDAT [74]	Y2	I/O	4
PDAT [73]	W4	I/O	4
PDAT [72]	W3	I/O	4
PDAT [71]	L1	I/O	4
PDAT [70]	K3	I/O	4
PDAT [69]	L3	I/O	4
PDAT [68]	M3	I/O	4
PDAT [67]	M4	I/O	4
PDAT [66]	N1	I/O	4
PDAT [65]	N2	I/O	4
PDAT [64]	N3	I/O	4
PDAT [63]	U26	I/O	4
PDAT [62]	V25	I/O	4
PDAT [61]	V24	I/O	4
PDAT [60]	V23	I/O	4

NAME	NUMBER	I/O	DRIVE (mA)
PDAT [59]	W24	I/O	4
PDAT [58]	W25	I/O	4
PDAT [57]	Y24	I/O	4
PDAT [56]	Y25	I/O	4
PDAT [55]	AC24	I/O	4
PDAT [54]	AC25	I/O	4
PDAT [53]	AB23	I/O	4
PDAT [52]	AB24	I/O	4
PDAT [51]	AB25	I/O	4
PDAT [50]	AA24	I/O	4
PDAT [49]	AA25	I/O	4
PDAT [48]	Y26	I/O	4
PDAT [47]	AD19	I/O	4
PDAT [46]	AC19	I/O	4
PDAT [45]	AF18	I/O	4
PDAT [44]	AE18	I/O	4
PDAT [43]	AD18	I/O	4
PDAT [42]	AE17	I/O	4
PDAT [41]	AD17	I/O	4
PDAT [40]	AC17	I/O	4
PDAT [39]	AE14	I/O	4
PDAT [38]	AD14	I/O	4
PDAT [37]	AF15	I/O	4
PDAT [36]	AE15	I/O	4
PDAT [35]	AD15	I/O	4
PDAT [34]	AE16	I/O	4
PDAT [33]	AD16	I/O	4
PDAT [32]	AF17	I/O	4
PDAT [31]	AD8	I/O	4
PDAT [30]	AE7	I/O	4
PDAT [29]	AD7	I/O	4
PDAT [28]	AC7	I/O	4

NAME	NUMBER	I/O	DRIVE (mA)
PDAT [27]	AD6	I/O	4
PDAT [26]	AE6	I/O	4
PDAT [25]	AF6	I/O	4
PDAT [24]	AE5	I/O	4
PDAT [23]	AF2	I/O	4
PDAT [22]	AF3	I/O	4
PDAT [21]	AE3	I/O	4
PDAT [20]	AD4	I/O	4
PDAT [19]	AE4	I/O	4
PDAT [18]	AF4	I/O	4
PDAT [17]	AC5	I/O	4
PDAT [16]	AD5	I/O	4
PDAT [15]	W2	I/O	4
PDAT [14]	W1	I/O	4
PDAT [13]	V3	I/O	4
PDAT [12]	V2	I/O	4
PDAT [11]	V1	I/O	4
PDAT [10]	U4	I/O	4
PDAT [09]	U3	I/O	4
PDAT [08]	U2	I/O	4
PDAT [07]	P3	I/O	4
PDAT [06]	P4	I/O	4
PDAT [05]	R2	I/O	4
PDAT [04]	R3	I/O	4
PDAT [03]	R4	I/O	4
PDAT [02]	T1	I/O	4
PDAT [01]	T2	I/O	4
PDAT [00]	T3	I/O	4
D_CS#[3] (SGRAM) DRAS# [3] (WRAM, EDO)	N25	O	6
D_CS#[2] (SGRAM) DRAS# [2] (WRAM, EDO)	L25	O	6
D_CS#[1] (SGRAM) DRAS# [1] (WRAM, EDO)	D26	O	6

NAME	NUMBER	I/O	DRIVE (mA)
D_CS#[0] (SGRAM) DRAS# [0] (WRAM, EDO)	J26	O	6
V_CS#[1] (SGRAM) VRAS# [1] (WRAM, EDO)	E25	O	6
V_CS#[0] (SGRAM) VRAS# [0] (WRAM, EDO)	U25	O	6
DQM[15] (SGRAM) BE#[15] (WINRAM) CAS# [15] (EDO)	R26	O	6
DQM[14] (SGRAM) BE#[14] (WINRAM) CAS# [14] (EDO)	AA26	O	6
DQM[13] (SGRAM) BE#[13] (WINRAM) CAS# [13] (EDO)	AF22	O	6
DQM[12] (SGRAM) BE#[12] (WINRAM) CAS# [12] (EDO)	AF13	O	6
DQM[11] (SGRAM) BE#[11] (WINRAM) CAS# [11] (EDO)	AF10	O	6
DQM[10] (SGRAM) BE#[10] (WINRAM) CAS# [10] (EDO)	AF5	O	6
DQM[09] (SGRAM) BE#[09] (WINRAM) CAS# [09] (EDO)	AB1	O	6
DQM[08] (SGRAM) BE#[08] (WINRAM) CAS# [08] (EDO)	P1	O	6
DQM[07] (SGRAM) BE#[07] (WINRAM) CAS# [07] (EDO)	V26	O	6
DQM[06] (SGRAM) BE#[06] (WINRAM) CAS# [06] (EDO)	W26	O	6

DQM[05] (SGRAM) BE#[05] (WINRAM) CAS# [05] (EDO)	AF19	O	6
DQM[04] (SGRAM) BE#[04] (WINRAM) CAS# [04] (EDO)	AF16	O	6
DQM[03] (SGRAM) BE#[03] (WINRAM) CAS# [03] (EDO)	AF8	O	6
DQM[02] (SGRAM) BE#[02] (WINRAM) CAS# [02] (EDO)	AF7	O	6
DQM[01] (SGRAM) BE#[01] (WINRAM) CAS# [01] (EDO)	Y1	O	6
DQM[00] (SGRAM) BE#[00] (WINRAM) CAS# [00] (EDO)	U1	O	6
WE [1] (SGRAM) CAS# [1] (WINRAM) WB_WE [1] (EDO)	AF12	O	8
WE [0] (SGRAM) CAS# [0] (WINRAM) WB_WE [0] (EDO)	P25	O	8
D_SF (SGRAM) D_OE# (WINRAM) DT_OE# (EDO)	H26	O	8
V_SF (SGRAM) V_OE# (WINRAM) V_OE# (EDO)	AC22	O	8
CAS# (SGRAM) SF[2] (WINRAM) (EDO N/A)	M23	O	12
RAS# (SGRAM) SF[1] (WINRAM) (EDO N/A)	Y23	O	12

SF[0] (SGRAM N/A) SF[0] (WINRAM) (EDO)	F24	O	12
SOE[3]# (SGRAM) (WINRAM,)	R1	O	2
SOE[2]# (SGRAM) (WINRAM,)	P2	O	2
POE# SOE[1]# (SGRAM) (WINRAM,)	M2	O	2
SOE[0]# (SGRAM) (WINRAM,)	M1	O	2
(?)	C16	O	2
(?)	C17	O	2
PA [7]	A10	O	2
PA [6]	B11	O	2
PA [5]	A11	O	2
PA [4]	B12	O	2
PA [3]	A12	O	2
PA [2]	B13	O	2
PA [1]	A13	O	2
PA [0]	B14	O	2

NAME	NUMBER	I/O	DRIVE (mA)
PD [07]	A18	I/O	4
PD [06]	A17	I/O	4
PD [05]	B17	I/O	4
PD [04]	A16	I/O	4
PD [03]	B16	I/O	4
PD [02]	A15	I/O	4
PD [01]	B15	I/O	4
PD [00]	A14	I/O	4
PWE#	C26	O	2
POE#	E26	O	2
VCLK	B23	I	
SCLK	G26	I/O	8
HSYNC	B24	O	4
VSYNC	A24	O	4
CBLANK	A23	O	4
DECLK	K25	I	
SENSE#	A22	I	
RST_OUT#	B21	O	2
PWR#	D20	O	2
PRD#	C21	O	2
PCS#	B22	O	2
PSFT	C15	O	2

NAME	NUMBER	I/O	DRIVE (mA)
EXV#	B10	I	
DDC_DAT	A25	I/O	4
DDC_CLK	B20	I/O	4
VCSEL	C20	O	4
LD_CLK	A21	O	4
DDAT[31]	B18	O	4
DDAT[30]	C18	O	4
DDAT[29]	A19	O	4
DDAT[28]	A20	O	4
DDAT[27]	B19	O	4
DDAT[26]	C19	O	4
DDAT[25]	C22	O	4
DDAT[24]	D22	O	4
DDAT[23]	C23	O	4
DDAT[22]	H23	O	4
DDAT[21]	D17	O	4
DDAT[20]	C25	O	4
DDAT[19]	D24	O	4
DDAT[18]	D25	O	4
DDAT[17]	E24	O	4
DDAT[16]	E23	O	4
DDAT[15]	F25	O	4
DDAT[14]	G25	O	4
DDAT[13]	G23	O	4
DDAT[12]	G24	O	4
DDAT[11]	H25	O	4
DDAT[10]	H24	O	4
DDAT[9]	J25	O	4
DDAT[8]	J24	O	4
DDAT[7]	K24	O	4
DDAT[6]	K23	O	4
DDAT[5]	L24	O	4

NAME	NUMBER	I/O	DRIVE (mA)
DDAT[4]	M25	O	4
DDAT[3]	M24	O	4
DDAT[2]	N23	O	4
DDAT[1]	N24	O	4
DDAT[0]	P24	O	4
TOUT	AC10	O	4

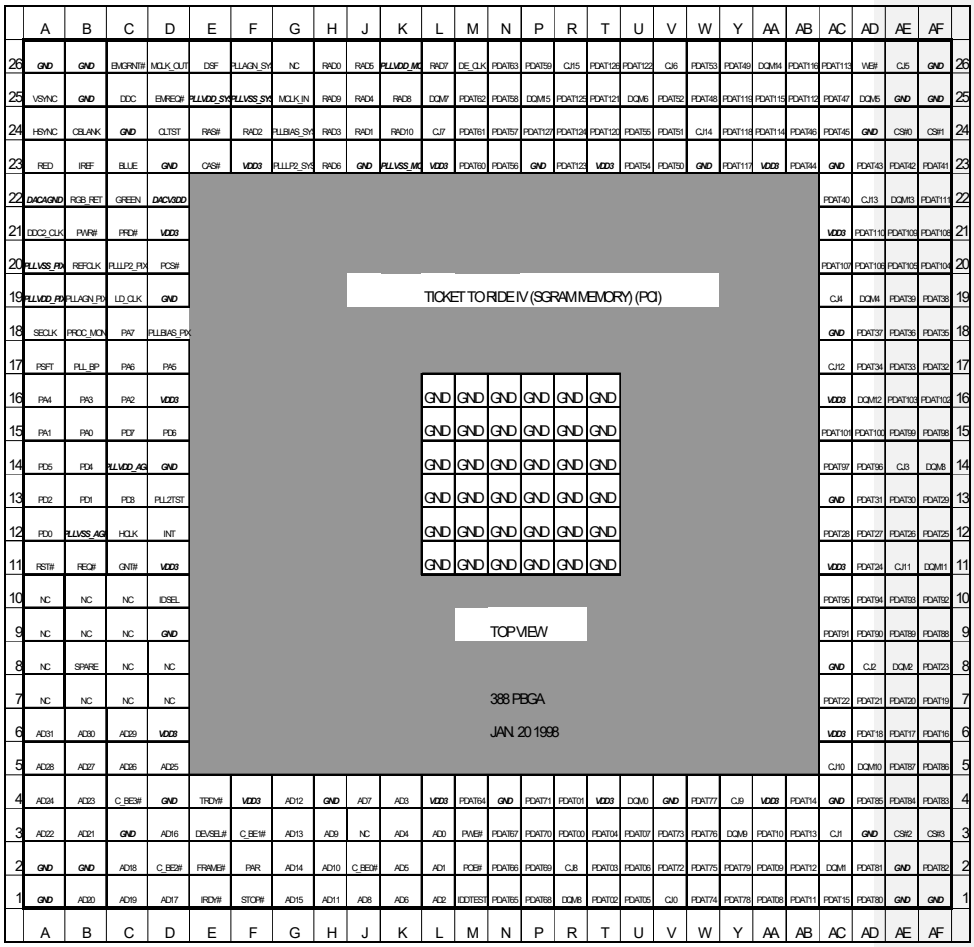
Power Pins

NAME	NUMBER
VDD (+5 volts)	A4, A8, B6, D3, F1, J1
VDD (+3.3 volts)	D6, D11, D16, D21, F4, F23, L4, L23, T4, T23, AA4, AC6, AC11, AC16, AC21, AA23
VSS	A1, A2, A26, B2, B25, B26, C3, C12, C13, C14, C24, D4, D9, D13, D14, D15, D19, D23, H4, J23, N4, P23, V4, W23, AC4, AC8, AC13, AC14, AC15, AC18, AC23, AD3, AD24, AE1, AE2, AE25, AF1, AF25, AF26

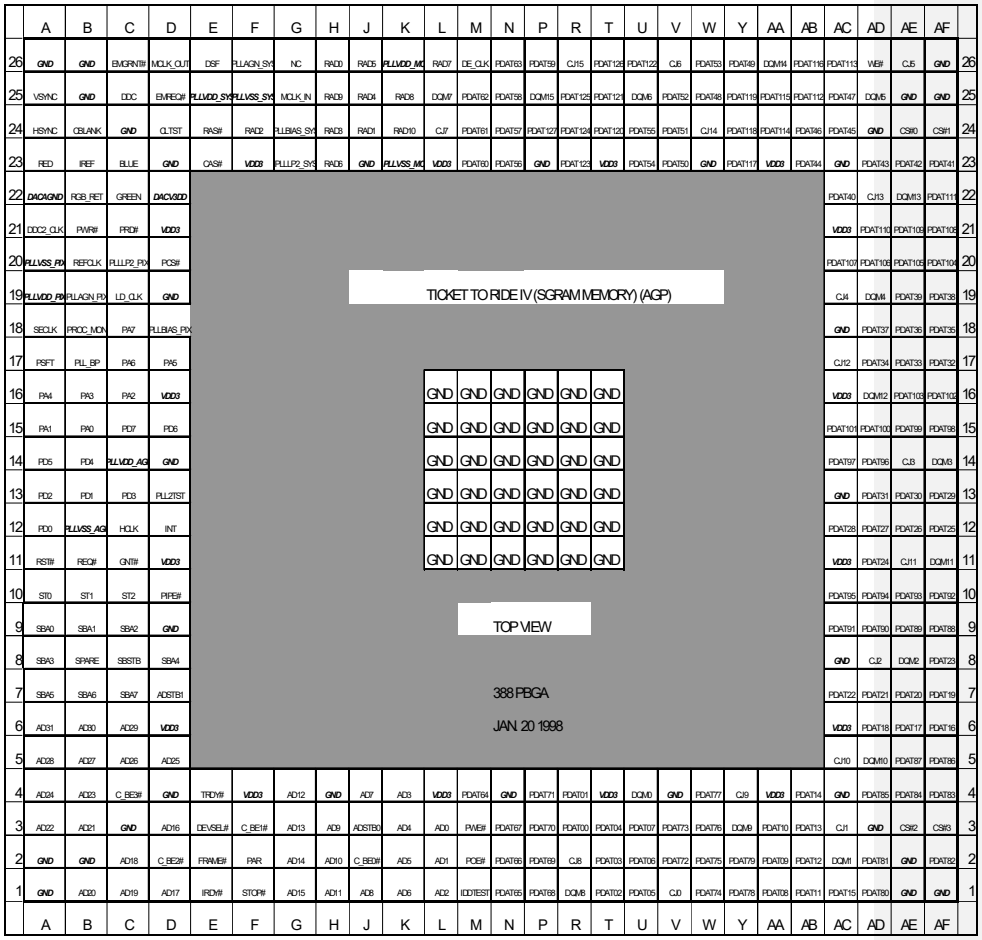
Note: D10 and all pins N/C or N/A are unconnected pins.

(Bottom View of 388)

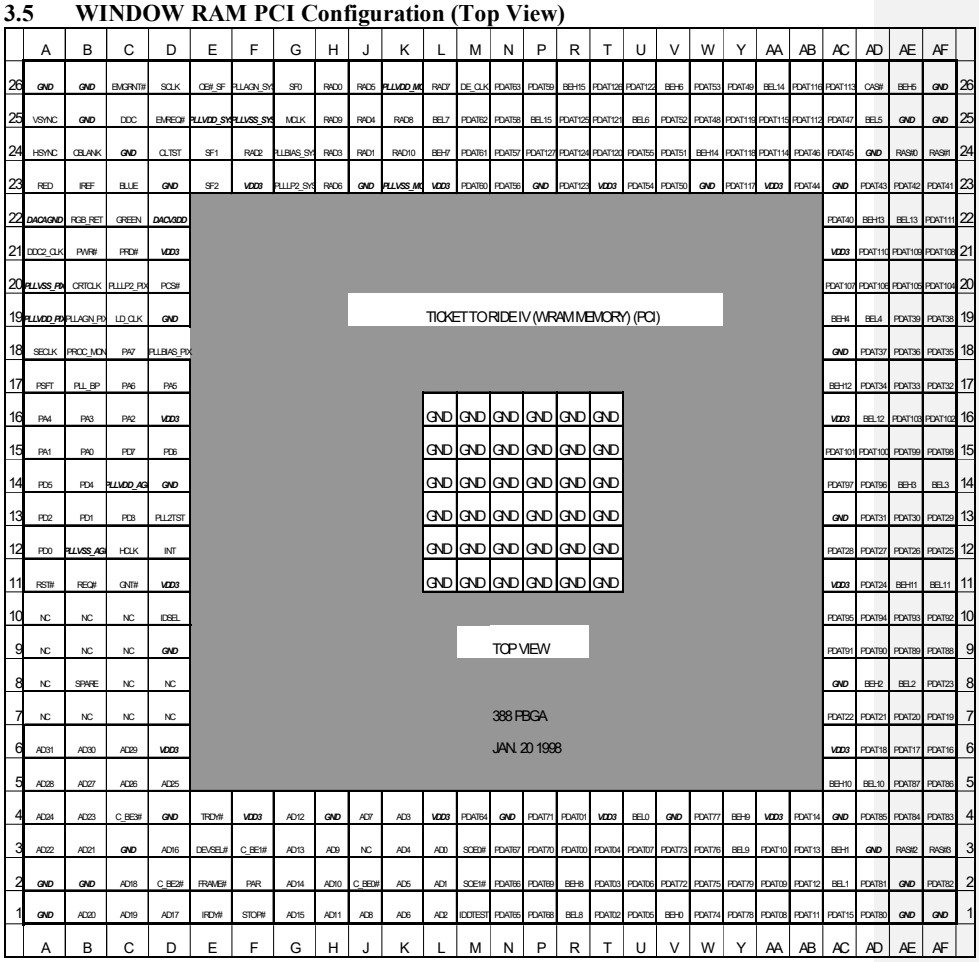
3.3 SGRAM PCI Configuration (Top View)



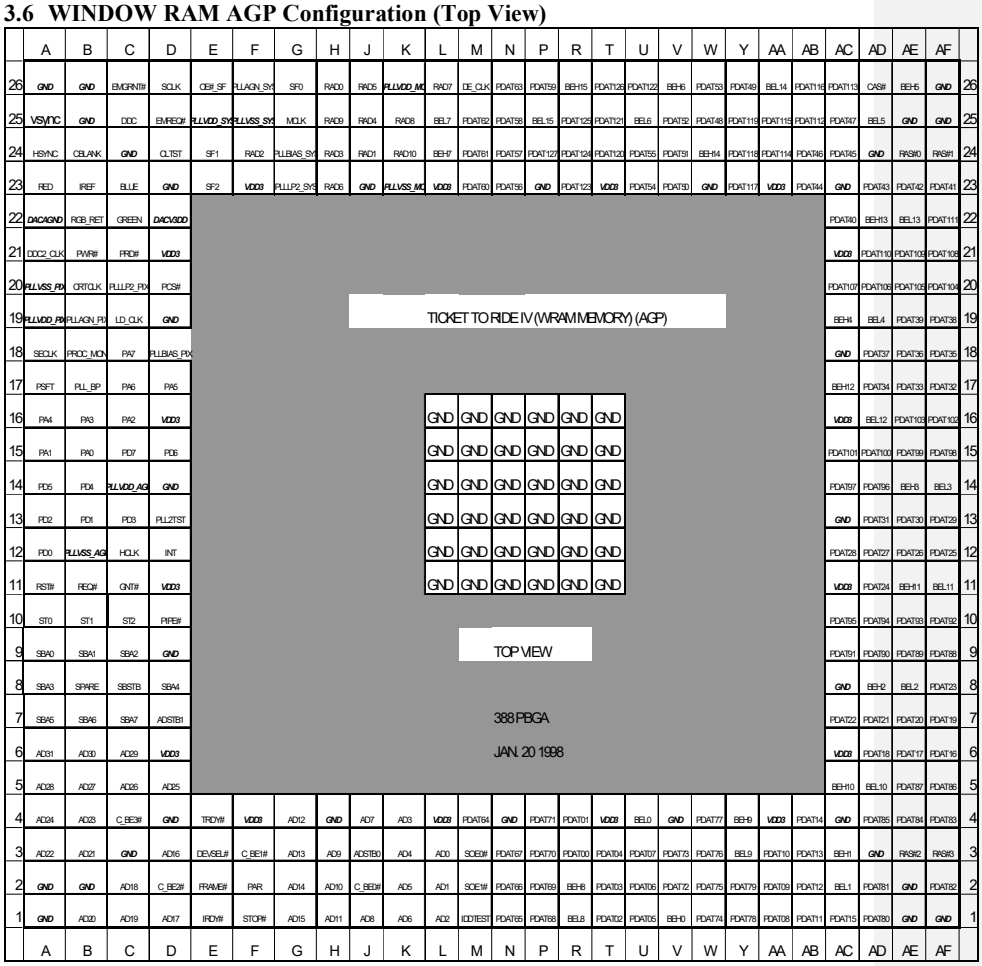
3.4 SGRAM AGP Configuration (Top View)



3.5 WINDOW RAM PCI Configuration (Top View)



3.6 WINDOW RAM AGP Configuration (Top View)



3.6 Configuration Pins

As IMAGINE 128™ is being reset during the power up sequence, the logic states of **32 configuration pins** are used to configure specific functions. The values on configuration pins are latched into XXXX™ on the rising edge of the RST# signal and may be read at any time in the ID or CONFIG registers. The notation "CP[0]" corresponds to the logic state on CONFIGURATION_PIN[0] at the rising edge of RST#. Likewise, CP[27:26] would correspond to CONFIGURATION_PIN[27:26].

Добавлено примечание ([NNCC1]):

The configuration pins **are not** dedicated pins. They actually correspond to other functional pins of the chip as follows:

CONFIGURATION_PIN[15:0] use BEh[15:0] pins
CONFIGURATION_PIN[23:16] use PD[7:0] pins
CONFIGURATION_PIN[31:24] use PA[7:0] pins

The PA and PD pins are internally pulled down to logic zero. A value of logic one can be achieved on CP[31:16] through the use of an external pull up resistor.

The BEh pins are internally pulled up to logic one. A value of logic zero can be achieved on CP[15:0] through the use of an external pull down resistor.

PINS	NAME	VALUE	DESCRIPTION
CP[15:0]	SVID		Subsystem Vendor ID This 16 bit field is the PCI Subsystem Vendor ID. It can be read at address 0x2C in PCI configuration space. This field will correspond to CP[15:0] unless CP[16] is set to zero, in which case the SVID will be set to 0x105D; the vendor ID for Number Nine Visual Technology
CP[16]	SSEL		Subsystem Vendor ID Select This bit allows the Subsystem Vendor ID fields in PCI configuration space to be set according to CP[15:0].
		0 1	Subsystem Vendor ID = 0x105D; Subsystem Vendor ID selected by CP[15:0]
CP[22:17]	SID		Subsystem ID This **6 bit** field corresponds to the lower 6 bits of the PCI Subsystem ID; the upper 10 bits of the SID will always be zero. It can be read at address 0x2E in PCI configuration space. This field will **always** correspond to CP[22:17] (regardless of the value of CP[16]). .
CP[23]	HBT		Host Bus Type
		0 1	AGP Bus PCI Bus
			It can be read in ID register bit[3]

PINS	NAME	VALUE	DESCRIPTION
CP[24]	SGR		Local memory type:
		1	SGRAM
		0	WINDOW RAM
			It can be read in CONFIG2 REGISTER bit[1]
CP[25]	IDAC		Internal RAMDAC enable
		0	External RAMDAC enabled
		1	Internal RAMDAC enabled
			It can be read in CONFIG2 REGISTER bit[0]
			This configuration pin selects default value (after reset) of CONFIG2 REGISTER bit[0].
CP[27:26]	DDEN		Local buffer memory density/type
		00	reserved
		01	256K bits by N memory chips
		10	16MBit chips (512K bits by 32) - if SGRAM memory 256K bits in interleaved mode - if WINDOW RAM
		11	Reserved
			It can be read in ID REGISTER bits[9:8]
CP[28]	CLASS		PCI Device Sub-Class
		0	VGA
		1	Other
			It can be read in ID REGISTER bit[28]
			Setting this configuration pin to a 1 disables the VGA component (i.e., VGA decodes will never occur regardless of VGA_CTRL settings).
CP[29]	EE		EPROM Boot Enable:
			This pin provides the power-on default value for CONFIG1[13], which is the EPROM (RBASE_E) decode enable.
		0	EPROM Boot Decode disabled
		1	EPROM Boot Decode Enabled
			It can be read in ID REGISTER bit[30]

CP[31:30]	BASE0/1		PCI Base 0 Address Register Size and PCI Base 1 Address Register Size
		00	4 Megabyte Memory Space Requested
		01	8 Megabyte Memory Space Requested
		10	16 Megabyte Memory Space Requested
		11	32 Megabyte Memory Space Requested
			These two bits select memory space requested for Linear Memory Window 0 and 1. **Both memory windows request same amount of memory**.
			Value of CP[31:30] can be read in ID REGISTER bits[7:6] or ID REGISTER bits[12:11]