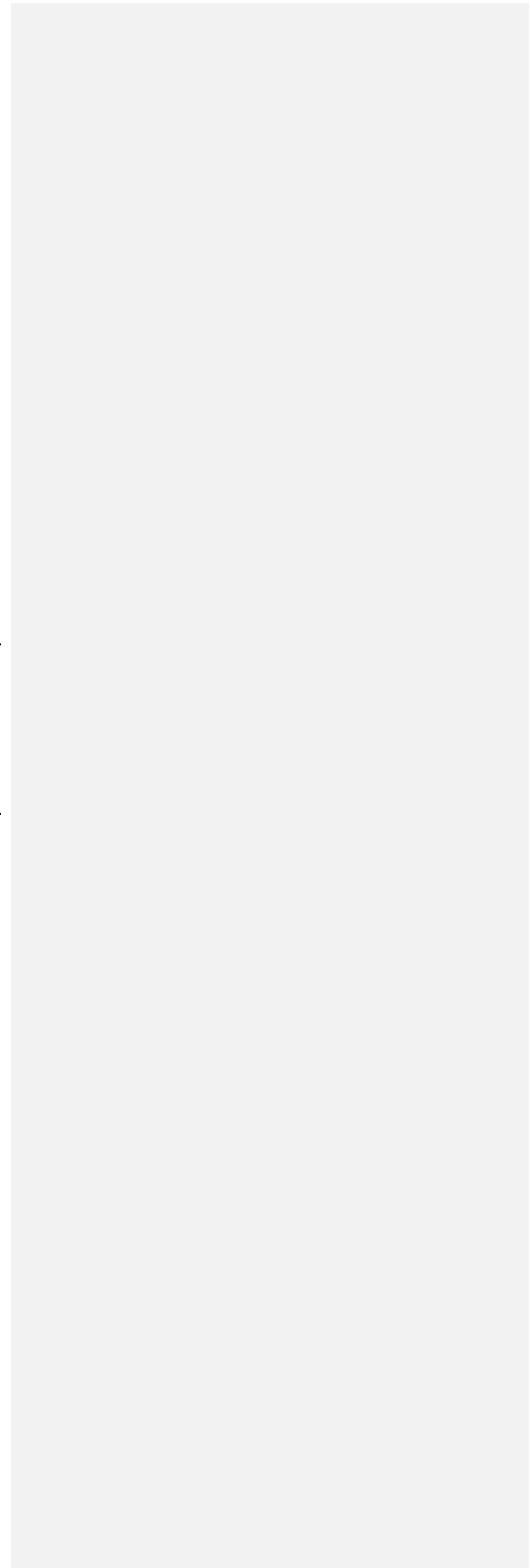




IMAGINE 128[™] I/O
Information





Section 3: IMAGINE 128^{MB} I/O Information

3.1 Signal Descriptions

IMAGINE 128^{MB} signal pins are categorized into the following five groups: **PCI/AGP Bus Interface**, **Display Buffer Interface**, **Peripheral Devices Interface**, **CRT Control**, and miscellaneous. The “#” indicates an active low signal.

PCI/AGP BUS INTERFACE SIGNALS

NAME	I/O	DESCRIPTION
AD[31:0]	I/O	Multiplexed address and data bus
C BE[3:0]	I/O	Command and Byte enables
HCLK	I	Host Bus Clock
RST#	I	System Reset
FRAME#	I/O	PCI cycle FRAME
PRDY#	I/O	Processor Ready (IRDY#, Initiator Ready)
TRDY#	I/O	Target Ready
DEVSEL#	I/O	PCI Device Select
STOP#	I/O	PCI cycle stop
INTRP#	O	Interrupt Pin
PAR	I/O	PCI Parity indicator
IDSEL	I	PCI Configuration Select
REQ#	O	Request bus mastering
GNT#	I	Grant bus mastering

DISPLAY BUFFER CONTROL SIGNALS

The local memory buffers of Imagine4 may be built using one of two types of memory:

- WINDOW RAM**
- SGRAM**

Names and/or function of some signals in this group change accordingly with selected type of memories.

Window RAM configuration:

NAME	I/O	DESCRIPTION
MCLK	I	Memory Controller Clock
RAD [8:0]	O	Display Buffer Address
PDAT [127:0]	I/O	Display Buffer Data Bus
RAS# [3:0]	O	Display Buffer Row Address Strobes
BEL# [15:0]	O	Display Buffer Low Byte Enable
BEH# [15:0]	O	Display Buffer High Byte Enable (Used only with Interleaved WRAM)
CAS#	O	Display Buffer Column Address Strobes
OE# SF	O	Output enable for Display Buffer
SF[2:0]	O	Display Buffer Special Function Signal
SOE# [3:0]	O	Display Buffer Serial Output enable

SGRAM configuration:

NAME	I/O	DESCRIPTION
MCLK	I	Memory Controller Clock
RAD [10:0]	O	Display Address RAD[9] is used as SGRAM bank select
PDAT [127:0]	I/O	Display Buffer Data Bus
CS# [3:0]	O	Display Buffer Chip Select D SC#[3:2] are used as RAD[11:10] in case of 16Mbit SGRAM
DQM# [15:0]	O	Display Buffer Byte Enable
CJ[15:0]	I	Placeholders for SGRAM only.
WE#	O	Display Buffer Write Enable
DSF	O	Display Buffer Special Function Signal
RAS#	O	Display Buffer Row Address Strobe Enable
CAS#	O	Display Buffer Column Address Strobe Enable
PWE#	O	Peripheral Write Enable
POE#	O	Peripheral Output Enable

**PERIPHERAL DEVICES CONTROL SIGNALS**

NAME	I/O	DESCRIPTION
PA [7:0]	O	Address
PD [7:0]	I/O	Data Bus
PWE#	O	Write Strobe
POE#	O	EPROM Output Enable
PCS#	O	EPROM Chip Select
PWR#	O	Peripheral Port (DAC) Write
PRD#	O	Peripheral Port (DAC) Read
PSFT	O	Load Soft Switch

CRT CONTROLLER SIGNALS

NAME	I/O	DESCRIPTION
VCLK	I	Video Timing Clock
SCLK	I/O	Serial Clock
HSYNC	O	Horizontal Sync
VSYNC	O	Vertical Sync
CBLANK	O	Composite Blank
DDC_DAT	I/O	DDC Data to/from monitor (SDA)
DDC_CLK	I/O	DDC clock (SCL)
EXV#	I	Enable External Video
LD_CLK	O	RAMDAC Load Clock
DDAT[31:0]	O	DRAM Controller/ VGA data

MISCELLANEOUS SIGNALS

NAME	I/O	DESCRIPTION
DECLK	I	Drawing Engine Clock
VCSEL	0	VGA Clock Frequency Select
TOUT	O	Factory Test

3.2 Pin Assignments

IMAGINE 128[™] is packaged in a 388 pin Plastic Ball Grid Array (PBGA).

NAME	NUMBER	I/O	DRIVE (mA)
AD [31]	C10	I/O	
AD [30]	A9	I/O	
AD [29]	D8	I/O	
AD [28]	B8	I/O	
AD [27]	A7	I/O	
AD [26]	D7	I/O	
AD [25]	B7	I/O	
AD [24]	A5	I/O	
AD [23]	C6	I/O	
AD [22]	D5	I/O	
AD [21]	B5	I/O	
AD [20]	B1	I/O	
AD [19]	C1	I/O	
AD [18]	C2	I/O	
AD [17]	D1	I/O	
AD [16]	D3	I/O	
AD [15]	G1	I/O	
AD [14]	G2	I/O	
AD [13]	G3	I/O	
AD [12]	G4	I/O	
AD [11]	H1	I/O	
AD [10]	H2	I/O	
AD [09]	H3	I/O	
AD [08]	J1	I/O	
AD [07]	J4	I/O	
AD [06]	K1	I/O	
AD [05]	K2	I/O	
AD [04]	K3	I/O	
AD [03]	K4	I/O	



NAME	NUMBER	I/O	DRIVE (mA)
AD [02]	L1	I/O	
AD [01]	L2	I/O	
AD [00]	G4	I/O	
C BE [3]	A6	I	
C BE [2]	D2	I	
C BE [1]	F3	I	
C BE [0]	J2	I	
HCLK	C11	I	
RST#	D12	I	
FRAME#	E2	I	
PRDY#	E1	I	
TRDY#	E4	O	
DEVSEL#	E3	O	
INTRP#	C8	O	
STOP#	F1	O	
PAR	F2	O	
IDSEL	B4	O	
REQ#	C9	O	
GNT#	F3	I	
MCLK	F26	I	
RAD [9]	D18	O	12
RAD [8]	K26	O	12
RAD [7]	L26	O	12
RAD [6]	M26	O	12
RAD [5]	N26	O	12
RAD [4]	P26	O	12
RAD [3]	AE26	O	12
RAD [2]	AD26	O	12
RAD [1]	AC26	O	12
RAD [0]	AB26	O	12
PDAT [127]	R25	I/O	4
PDAT [126]	R24	I/O	4
PDAT [125]	R23	I/O	4

NAME	NUMBER	I/O	DRIVE (mA)
PDAT [124]	T24	I/O	4
PDAT [123]	T25	I/O	4
PDAT [122]	T26	I/O	4
PDAT [121]	U24	I/O	4
PDAT [120]	U23	I/O	4
PDAT [119]	AD22	I/O	4
PDAT [118]	AF23	I/O	4
PDAT [117]	AF24	I/O	4
PDAT [116]	AE22	I/O	4
PDAT [115]	AE23	I/O	4
PDAT [114]	AE24	I/O	4
PDAT [113]	AD23	I/O	4
PDAT [112]	AD25	I/O	4
PDAT [111]	AF21	I/O	4
PDAT [110]	AE21	I/O	4
PDAT [109]	AD21	I/O	4
PDAT [108]	AF20	I/O	4
PDAT [107]	AE20	I/O	4
PDAT [106]	AD20	I/O	4
PDAT [105]	AC20	I/O	4
PDAT [104]	AE19	I/O	4
PDAT [103]	AE11	I/O	4
PDAT [102]	AF11	I/O	4
PDAT [101]	AE12	I/O	4
PDAT [100]	AD12	I/O	4
PDAT [99]	AC12	I/O	4
PDAT [98]	AD13	I/O	4
PDAT [97]	AE13	I/O	4
PDAT [96]	AF14	I/O	4
PDAT [95]	AD11	I/O	4
PDAT [94]	AE10	I/O	4
PDAT [93]	AD10	I/O	4
PDAT [92]	AC9	I/O	4



NAME	NUMBER	I/O	DRIVE (mA)
PDAT [91]	AD9	I/O	4
PDAT [90]	AE9	I/O	4
PDAT [89]	AF9	I/O	4
PDAT [88]	AE8	I/O	4
PDAT [87]	AC1	I/O	4
PDAT [86]	AB2	I/O	4
PDAT [85]	AB3	I/O	4
PDAT [84]	AB4	I/O	4
PDAT [83]	AC2	I/O	4
PDAT [82]	AC3	I/O	4
PDAT [81]	AD1	I/O	4
PDAT [80]	AD2	I/O	4
PDAT [79]	AA3	I/O	4
PDAT [78]	AA2	I/O	4
PDAT [77]	AA1	I/O	4
PDAT [76]	Y4	I/O	4
PDAT [75]	Y3	I/O	4
PDAT [74]	Y2	I/O	4
PDAT [73]	W4	I/O	4
PDAT [72]	W3	I/O	4
PDAT [71]	L1	I/O	4
PDAT [70]	K3	I/O	4
PDAT [69]	L3	I/O	4
PDAT [68]	M3	I/O	4
PDAT [67]	M4	I/O	4
PDAT [66]	N1	I/O	4
PDAT [65]	N2	I/O	4
PDAT [64]	N3	I/O	4
PDAT [63]	U26	I/O	4
PDAT [62]	V25	I/O	4
PDAT [61]	V24	I/O	4
PDAT [60]	V23	I/O	4

NAME	NUMBER	I/O	DRIVE (mA)
PDAT [59]	W24	I/O	4
PDAT [58]	W25	I/O	4
PDAT [57]	Y24	I/O	4
PDAT [56]	Y25	I/O	4
PDAT [55]	AC24	I/O	4
PDAT [54]	AC25	I/O	4
PDAT [53]	AB23	I/O	4
PDAT [52]	AB24	I/O	4
PDAT [51]	AB25	I/O	4
PDAT [50]	AA24	I/O	4
PDAT [49]	AA25	I/O	4
PDAT [48]	Y26	I/O	4
PDAT [47]	AD19	I/O	4
PDAT [46]	AC19	I/O	4
PDAT [45]	AF18	I/O	4
PDAT [44]	AE18	I/O	4
PDAT [43]	AD18	I/O	4
PDAT [42]	AE17	I/O	4
PDAT [41]	AD17	I/O	4
PDAT [40]	AC17	I/O	4
PDAT [39]	AE14	I/O	4
PDAT [38]	AD14	I/O	4
PDAT [37]	AF15	I/O	4
PDAT [36]	AE15	I/O	4
PDAT [35]	AD15	I/O	4
PDAT [34]	AE16	I/O	4
PDAT [33]	AD16	I/O	4
PDAT [32]	AF17	I/O	4
PDAT [31]	AD8	I/O	4
PDAT [30]	AE7	I/O	4
PDAT [29]	AD7	I/O	4
PDAT [28]	AC7	I/O	4



NAME	NUMBER	I/O	DRIVE (mA)
PDAT [27]	AD6	I/O	4
PDAT [26]	AE6	I/O	4
PDAT [25]	AF6	I/O	4
PDAT [24]	AE5	I/O	4
PDAT [23]	AF2	I/O	4
PDAT [22]	AF3	I/O	4
PDAT [21]	AE3	I/O	4
PDAT [20]	AD4	I/O	4
PDAT [19]	AE4	I/O	4
PDAT [18]	AF4	I/O	4
PDAT [17]	AC5	I/O	4
PDAT [16]	AD5	I/O	4
PDAT [15]	W2	I/O	4
PDAT [14]	W1	I/O	4
PDAT [13]	V3	I/O	4
PDAT [12]	V2	I/O	4
PDAT [11]	V1	I/O	4
PDAT [10]	U4	I/O	4
PDAT [09]	U3	I/O	4
PDAT [08]	U2	I/O	4
PDAT [07]	P3	I/O	4
PDAT [06]	P4	I/O	4
PDAT [05]	R2	I/O	4
PDAT [04]	R3	I/O	4
PDAT [03]	R4	I/O	4
PDAT [02]	T1	I/O	4
PDAT [01]	T2	I/O	4
PDAT [00]	T3	I/O	4
D_CS#[3] (SGRAM) DRAS#[3] (WRAM, EDO)	N25	O	6
D_CS#[2] (SGRAM) DRAS#[2] (WRAM, EDO)	L25	O	6
D_CS#[1] (SGRAM) DRAS#[1] (WRAM, EDO)	D26	O	6

NAME	NUMBER	I/O	DRIVE (mA)
D_CS#[0] (SGRAM) DRAS# [0] (WRAM, EDO)	J26	O	6
V_CS#[1] (SGRAM) VRAS# [1] (WRAM, EDO)	E25	O	6
V_CS#[0] (SGRAM) VRAS# [0] (WRAM, EDO)	U25	O	6
DQM[15] (SGRAM) BE#[15] (WINRAM) CAS# [15] (EDO)	R26	O	6
DQM[14] (SGRAM) BE#[14] (WINRAM) CAS# [14] (EDO)	AA26	O	6
DQM[13] (SGRAM) BE#[13] (WINRAM) CAS# [13] (EDO)	AF22	O	6
DQM[12] (SGRAM) BE#[12] (WINRAM) CAS# [12] (EDO)	AF13	O	6
DQM[11] (SGRAM) BE#[11] (WINRAM) CAS# [11] (EDO)	AF10	O	6
DQM[10] (SGRAM) BE#[10] (WINRAM) CAS# [10] (EDO)	AF5	O	6
DQM[09] (SGRAM) BE#[09] (WINRAM) CAS# [09] (EDO)	AB1	O	6
DQM[08] (SGRAM) BE#[08] (WINRAM) CAS# [08] (EDO)	P1	O	6
DQM[07] (SGRAM) BE#[07] (WINRAM) CAS# [07] (EDO)	V26	O	6
DQM[06] (SGRAM) BE#[06] (WINRAM) CAS# [06] (EDO)	W26	O	6



DQM[05] BE#[05] (WINRAM) CAS# [05]	(SGRAM) (EDO)	AF19	O	6
DQM[04] BE#[04] (WINRAM) CAS# [04]	(SGRAM) (EDO)	AF16	O	6
DQM[03] BE#[03] (WINRAM) CAS# [03]	(SGRAM) (EDO)	AF8	O	6
DQM[02] BE#[02] (WINRAM) CAS# [02]	(SGRAM) (EDO)	AF7	O	6
DQM[01] BE#[01] (WINRAM) CAS# [01]	(SGRAM) (EDO)	Y1	O	6
DQM[00] BE#[00] (WINRAM) CAS# [00]	(SGRAM) (EDO)	U1	O	6
WE [1] CAS# [1] WB_WE [1]	(SGRAM) (WINRAM) (EDO)	AF12	O	8
WE [0] CAS# [0] WB_WE [0]	(SGRAM) (WINRAM) (EDO)	P25	O	8
D_SF D_OE# DT_OE#	(SGRAM) (WINRAM) (EDO)	H26	O	8
V_SF V_OE# V_OE# (EDO)	(SGRAM) (WINRAM) (EDO)	AC22	O	8
CAS# SF[2]	(SGRAM) (WINRAM) (EDO N/A)	M23	O	12
RAS# SF[1]	(SGRAM) (WINRAM) (EDO N/A)	Y23	O	12

SF[0] SF[0]	(SGRAM N/A) (WINRAM) (EDO)	F24	O	12
SOE[3]#	(SGRAM) (WINRAM)	R1	O	2
SOE[2]#	(SGRAM) (WINRAM)	P2	O	2
POE# SOE[1]#	(SGRAM) (WINRAM)	M2	O	2
SOE[0]#	(SGRAM) (WINRAM)	M1	O	2
(?)		C16	O	2
(?)		C17	O	2
PA [7]		A10	O	2
PA [6]		B11	O	2
PA [5]		A11	O	2
PA [4]		B12	O	2
PA [3]		A12	O	2
PA [2]		B13	O	2
PA [1]		A13	O	2
PA [0]		B14	O	2



NAME	NUMBER	I/O	DRIVE (mA)
PD [07]	A18	I/O	4
PD [06]	A17	I/O	4
PD [05]	B17	I/O	4
PD [04]	A16	I/O	4
PD [03]	B16	I/O	4
PD [02]	A15	I/O	4
PD [01]	B15	I/O	4
PD [00]	A14	I/O	4
PWE#	C26	O	2
POE#	E26	O	2
VCLK	B23	I	
SCLK	G26	I/O	8
HSYNC	B24	O	4
VSYNC	A24	O	4
CBLANK	A23	O	4
DECLK	K25	I	
SENSE#	A22	I	
RST_OUT#	B21	O	2
PWR#	D20	O	2
PRD#	C21	O	2
PCS#	B22	O	2
PSFT	C15	O	2

NAME	NUMBER	I/O	DRIVE (mA)
EXV#	B10	I	
DDC DAT	A25	I/O	4
DDC CLK	B20	I/O	4
VCSEL	C20	O	4
LD CLK	A21	O	4
DDAT[31]	B18	O	4
DDAT[30]	C18	O	4
DDAT[29]	A19	O	4
DDAT[28]	A20	O	4
DDAT[27]	B19	O	4
DDAT[26]	C19	O	4
DDAT[25]	C22	O	4
DDAT[24]	D22	O	4
DDAT[23]	C23	O	4
DDAT[22]	H23	O	4
DDAT[21]	D17	O	4
DDAT[20]	C25	O	4
DDAT[19]	D24	O	4
DDAT[18]	D25	O	4
DDAT[17]	E24	O	4
DDAT[16]	E23	O	4
DDAT[15]	F25	O	4
DDAT[14]	G25	O	4
DDAT[13]	G23	O	4
DDAT[12]	G24	O	4
DDAT[11]	H25	O	4
DDAT[10]	H24	O	4
DDAT[9]	J25	O	4
DDAT[8]	J24	O	4
DDAT[7]	K24	O	4
DDAT[6]	K23	O	4
DDAT[5]	L24	O	4



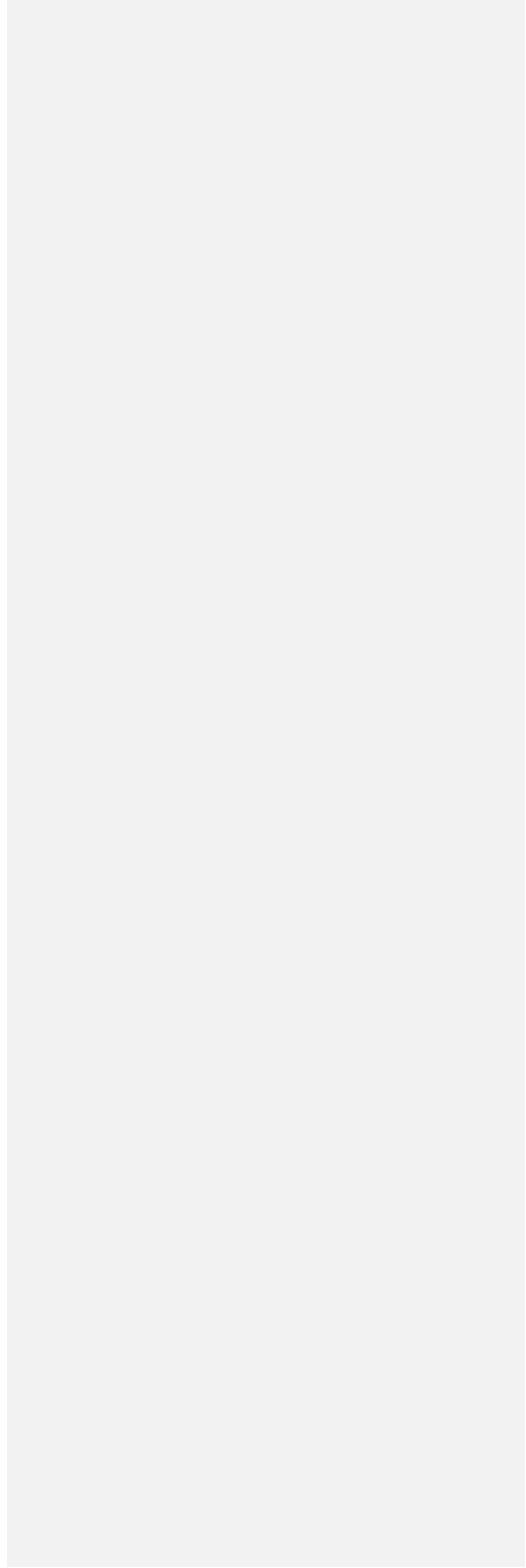
NAME	NUMBER	I/O	DRIVE (mA)
DDAT[4]	M25	O	4
DDAT[3]	M24	O	4
DDAT[2]	N23	O	4
DDAT[1]	N24	O	4
DDAT[0]	P24	O	4
TOUT	AC10	O	4

Power Pins

NAME	NUMBER
VDD (+5 volts)	A4, A8, B6, D3, F1, J1
VDD (+3.3 volts)	D6, D11, D16, D21, F4, F23, L4, L23, T4, T23, AA4, AC6, AC11, AC16, AC21, AA23
VSS	A1, A2, A26, B2, B25, B26, C3, C12, C13, C14, C24, D4, D9, D13, D14, D15, D19, D23, H4, J23, N4, P23, V4, W23, AC4, AC8, AC13, AC14, AC15, AC18, AC23, AD3, AD24, AE1, AE2, AE25, AF1, AF25, AF26

Note: D10 and all pins N/C or N/A are unconnected pins.

(Bottom View of 388)

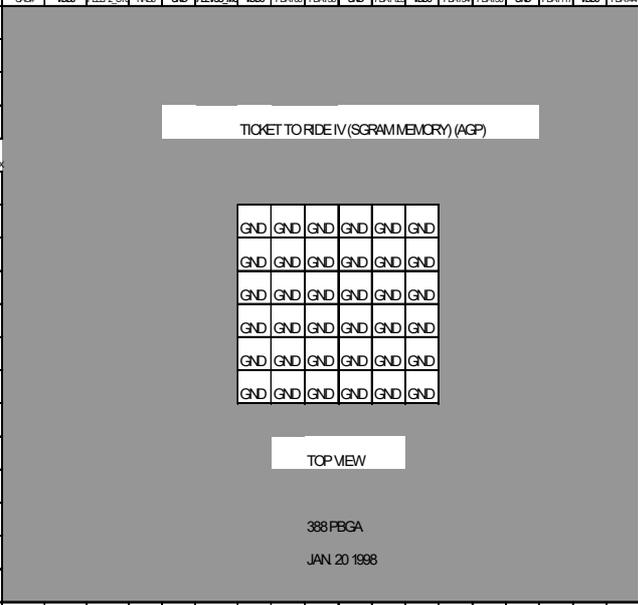




3.3 SGRAM PCI Configuration (Top View)

	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	T	U	V	W	Y	AA	AB	AC	AD	AE	AF																																															
26	GND	GND	BMGRN#	MDK_OUT	DSF	FLAGN_S#	NC	RWD0	RWD5	PLVDD_M	RWZ	DE_CLK	PDAT83	PDAT89	CJ15	PDAT128	PDAT122	CJ6	PDAT83	PDAT89	DQM4	PDAT116	PDAT115	VE#	CJ5	GND	26																																														
25	VSINC	GND	DDC	EMREQ	PLVDD_S#	PLVSS_S#	MDK_IN	RWD9	RWD4	RWD6	DDI#	PDAT82	PDAT88	DQM5	PDAT125	PDAT121	DQM6	PDAT82	PDAT88	PDAT118	PDAT113	PDAT112	PDAT47	DQM5	GND	GND	25																																														
24	HSINC	CEBLANK	GND	CLTST	RW#	RWD2	PLVBAS_S#	RWD3	RWD1	RWD10	CJ7	PDAT81	PDAT87	PDAT127	PDAT124	PDAT123	PDAT85	PDAT81	CJ14	PDAT118	PDAT114	PDAT96	PDAT45	GND	CS90	CS91	24																																														
23	RED	IRF	BLUE	GND	CS#	VDD3	PLLP2_S#	RWD6	GND	PLVSS_M	VDD3	PDAT80	PDAT86	GND	PDAT123	VDD3	PDAT84	PDAT80	GND	PDAT117	VDD3	PDAT94	GND	PDAT43	PDAT42	PDAT41	23																																														
22	DMA_GND	RGB_RET	GREEN	DMA_VDD	<div style="border: 1px solid black; padding: 10px; width: fit-content; margin: 0 auto;"> <p>TICKET TO RIDE IV (SGRAM MEMORY) (PCI)</p> </div> <div style="border: 1px solid black; padding: 10px; width: fit-content; margin: 10px auto;"> <table border="1" style="text-align: center;"> <tr><td>GND</td><td>GND</td><td>GND</td><td>GND</td><td>GND</td><td>GND</td></tr> <tr><td>GND</td><td>GND</td><td>GND</td><td>GND</td><td>GND</td><td>GND</td></tr> <tr><td>GND</td><td>GND</td><td>GND</td><td>GND</td><td>GND</td><td>GND</td></tr> <tr><td>GND</td><td>GND</td><td>GND</td><td>GND</td><td>GND</td><td>GND</td></tr> <tr><td>GND</td><td>GND</td><td>GND</td><td>GND</td><td>GND</td><td>GND</td></tr> </table> </div> <div style="border: 1px solid black; padding: 10px; width: fit-content; margin: 10px auto;"> <p>TOPVIEW</p> </div> <div style="text-align: center; margin: 10px auto;"> <p>388 PBGA JAN. 20 1998</p> </div>																	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	PDAT40	CJ3	DQM3	PDAT111	22																	
GND	GND	GND	GND	GND																		GND																																																			
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21	EDC2_CLK	PW#	RF#	VDD3																		<div style="border: 1px solid black; padding: 10px; width: fit-content; margin: 0 auto;"> <p>TICKET TO RIDE IV (SGRAM MEMORY) (PCI)</p> </div> <div style="border: 1px solid black; padding: 10px; width: fit-content; margin: 10px auto;"> <table border="1" style="text-align: center;"> <tr><td>GND</td><td>GND</td><td>GND</td><td>GND</td><td>GND</td><td>GND</td></tr> <tr><td>GND</td><td>GND</td><td>GND</td><td>GND</td><td>GND</td><td>GND</td></tr> <tr><td>GND</td><td>GND</td><td>GND</td><td>GND</td><td>GND</td><td>GND</td></tr> <tr><td>GND</td><td>GND</td><td>GND</td><td>GND</td><td>GND</td><td>GND</td></tr> <tr><td>GND</td><td>GND</td><td>GND</td><td>GND</td><td>GND</td><td>GND</td></tr> </table> </div> <div style="border: 1px solid black; padding: 10px; width: fit-content; margin: 10px auto;"> <p>TOPVIEW</p> </div> <div style="text-align: center; margin: 10px auto;"> <p>388 PBGA JAN. 20 1998</p> </div>																	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	PDAT110	PDAT109	PDAT108	21	
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20	PLVSS_P#	REFCLK	PLLP2_P#	PC#	<div style="border: 1px solid black; padding: 10px; width: fit-content; margin: 0 auto;"> <p>TICKET TO RIDE IV (SGRAM MEMORY) (PCI)</p> </div> <div style="border: 1px solid black; padding: 10px; width: fit-content; margin: 10px auto;"> <table border="1" style="text-align: center;"> <tr><td>GND</td><td>GND</td><td>GND</td><td>GND</td><td>GND</td><td>GND</td></tr> <tr><td>GND</td><td>GND</td><td>GND</td><td>GND</td><td>GND</td><td>GND</td></tr> <tr><td>GND</td><td>GND</td><td>GND</td><td>GND</td><td>GND</td><td>GND</td></tr> <tr><td>GND</td><td>GND</td><td>GND</td><td>GND</td><td>GND</td><td>GND</td></tr> <tr><td>GND</td><td>GND</td><td>GND</td><td>GND</td><td>GND</td><td>GND</td></tr> </table> </div> <div style="border: 1px solid black; padding: 10px; width: fit-content; margin: 10px auto;"> <p>TOPVIEW</p> </div> <div style="text-align: center; margin: 10px auto;"> <p>388 PBGA JAN. 20 1998</p> </div>																																		GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	PDAT107	PDAT106	PDAT105	PDAT104	20
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19	PLVDD_P#	FLAGN_P#	LD_CLK	GND																		<div style="border: 1px solid black; padding: 10px; width: fit-content; margin: 0 auto;"> <p>TICKET TO RIDE IV (SGRAM MEMORY) (PCI)</p> </div> <div style="border: 1px solid black; padding: 10px; width: fit-content; margin: 10px auto;"> <table border="1" style="text-align: center;"> <tr><td>GND</td><td>GND</td><td>GND</td><td>GND</td><td>GND</td><td>GND</td></tr> <tr><td>GND</td><td>GND</td><td>GND</td><td>GND</td><td>GND</td><td>GND</td></tr> <tr><td>GND</td><td>GND</td><td>GND</td><td>GND</td><td>GND</td><td>GND</td></tr> <tr><td>GND</td><td>GND</td><td>GND</td><td>GND</td><td>GND</td><td>GND</td></tr> <tr><td>GND</td><td>GND</td><td>GND</td><td>GND</td><td>GND</td><td>GND</td></tr> </table> </div> <div style="border: 1px solid black; padding: 10px; width: fit-content; margin: 10px auto;"> <p>TOPVIEW</p> </div> <div style="text-align: center; margin: 10px auto;"> <p>388 PBGA JAN. 20 1998</p> </div>																	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	CJ4	DQM4	PDAT99	PDAT98	19
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18	SECLK	PROC_MON	PA7	PLVBAS_P#	<div style="border: 1px solid black; padding: 10px; width: fit-content; margin: 0 auto;"> <p>TICKET TO RIDE IV (SGRAM MEMORY) (PCI)</p> </div> <div style="border: 1px solid black; padding: 10px; width: fit-content; margin: 10px auto;"> <table border="1" style="text-align: center;"> <tr><td>GND</td><td>GND</td><td>GND</td><td>GND</td><td>GND</td><td>GND</td></tr> <tr><td>GND</td><td>GND</td><td>GND</td><td>GND</td><td>GND</td><td>GND</td></tr> <tr><td>GND</td><td>GND</td><td>GND</td><td>GND</td><td>GND</td><td>GND</td></tr> <tr><td>GND</td><td>GND</td><td>GND</td><td>GND</td><td>GND</td><td>GND</td></tr> <tr><td>GND</td><td>GND</td><td>GND</td><td>GND</td><td>GND</td><td>GND</td></tr> </table> </div> <div style="border: 1px solid black; padding: 10px; width: fit-content; margin: 10px auto;"> <p>TOPVIEW</p> </div> <div style="text-align: center; margin: 10px auto;"> <p>388 PBGA JAN. 20 1998</p> </div>																																		GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	PDAT97	PDAT96	PDAT95	18
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16	PA4	PA3	PA2	VDD3	<div style="border: 1px solid black; padding: 10px; width: fit-content; margin: 0 auto;"> <p>TICKET TO RIDE IV (SGRAM MEMORY) (PCI)</p> </div> <div style="border: 1px solid black; padding: 10px; width: fit-content; margin: 10px auto;"> <table border="1" style="text-align: center;"> <tr><td>GND</td><td>GND</td><td>GND</td><td>GND</td><td>GND</td><td>GND</td></tr> <tr><td>GND</td><td>GND</td><td>GND</td><td>GND</td><td>GND</td><td>GND</td></tr> <tr><td>GND</td><td>GND</td><td>GND</td><td>GND</td><td>GND</td><td>GND</td></tr> <tr><td>GND</td><td>GND</td><td>GND</td><td>GND</td><td>GND</td><td>GND</td></tr> <tr><td>GND</td><td>GND</td><td>GND</td><td>GND</td><td>GND</td><td>GND</td></tr> </table> </div> <div style="border: 1px solid black; padding: 10px; width: fit-content; margin: 10px auto;"> <p>TOPVIEW</p> </div> <div style="text-align: center; margin: 10px auto;"> <p>388 PBGA JAN. 20 1998</p> </div>																																		GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	VDD3	DQM2	PDAT91	PDAT90	16
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14	PD5	PD4	PLVDD_A0	GND	<div style="border: 1px solid black; padding: 10px; width: fit-content; margin: 0 auto;"> <p>TICKET TO RIDE IV (SGRAM MEMORY) (PCI)</p> </div> <div style="border: 1px solid black; padding: 10px; width: fit-content; margin: 10px auto;"> <table border="1" style="text-align: center;"> <tr><td>GND</td><td>GND</td><td>GND</td><td>GND</td><td>GND</td><td>GND</td></tr> <tr><td>GND</td><td>GND</td><td>GND</td><td>GND</td><td>GND</td><td>GND</td></tr> <tr><td>GND</td><td>GND</td><td>GND</td><td>GND</td><td>GND</td><td>GND</td></tr> <tr><td>GND</td><td>GND</td><td>GND</td><td>GND</td><td>GND</td><td>GND</td></tr> <tr><td>GND</td><td>GND</td><td>GND</td><td>GND</td><td>GND</td><td>GND</td></tr> </table> </div> <div style="border: 1px solid black; padding: 10px; width: fit-content; margin: 10px auto;"> <p>TOPVIEW</p> </div> <div style="text-align: center; margin: 10px auto;"> <p>388 PBGA JAN. 20 1998</p> </div>																																		GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	PDAT89	PDAT88	CJ8	DQM8	14
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13	PD2	PD1	PD3	PLL21ST																		<div style="border: 1px solid black; padding: 10px; width: fit-content; margin: 0 auto;"> <p>TICKET TO RIDE IV (SGRAM MEMORY) (PCI)</p> </div> <div style="border: 1px solid black; padding: 10px; width: fit-content; margin: 10px auto;"> <table border="1" style="text-align: center;"> <tr><td>GND</td><td>GND</td><td>GND</td><td>GND</td><td>GND</td><td>GND</td></tr> <tr><td>GND</td><td>GND</td><td>GND</td><td>GND</td><td>GND</td><td>GND</td></tr> <tr><td>GND</td><td>GND</td><td>GND</td><td>GND</td><td>GND</td><td>GND</td></tr> <tr><td>GND</td><td>GND</td><td>GND</td><td>GND</td><td>GND</td><td>GND</td></tr> <tr><td>GND</td><td>GND</td><td>GND</td><td>GND</td><td>GND</td><td>GND</td></tr> </table> </div> <div style="border: 1px solid black; padding: 10px; width: fit-content; margin: 10px auto;"> <p>TOPVIEW</p> </div> <div style="text-align: center; margin: 10px auto;"> <p>388 PBGA JAN. 20 1998</p> </div>																	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	PDAT87	PDAT86	PDAT85	13
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9	NC	NC	NC	GND																		<div style="border: 1px solid black; padding: 10px; width: fit-content; margin: 0 auto;"> <p>TICKET TO RIDE IV (SGRAM MEMORY) (PCI)</p> </div> <div style="border: 1px solid black; padding: 10px; width: fit-content; margin: 10px auto;"> <table border="1" style="text-align: center;"> <tr><td>GND</td><td>GND</td><td>GND</td><td>GND</td><td>GND</td><td>GND</td></tr> <tr><td>GND</td><td>GND</td><td>GND</td><td>GND</td><td>GND</td><td>GND</td></tr> <tr><td>GND</td><td>GND</td><td>GND</td><td>GND</td><td>GND</td><td>GND</td></tr> <tr><td>GND</td><td>GND</td><td>GND</td><td>GND</td><td>GND</td><td>GND</td></tr> <tr><td>GND</td><td>GND</td><td>GND</td><td>GND</td><td>GND</td><td>GND</td></tr> </table> </div> <div style="border: 1px solid black; padding: 10px; width: fit-content; margin: 10px auto;"> <p>TOPVIEW</p> </div> <div style="text-align: center; margin: 10px auto;"> <p>388 PBGA JAN. 20 1998</p> </div>																	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	PDAT80	PDAT79	PDAT78	PDAT77	9
GND	GND	GND	GND	GND																																			GND																																		
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8	NC	SPARE	NC	NC	<div style="border: 1px solid black; padding: 10px; width: fit-content; margin: 0 auto;"> <p>TICKET TO RIDE IV (SGRAM MEMORY) (PCI)</p> </div> <div style="border: 1px solid black; padding: 10px; width: fit-content; margin: 10px auto;"> <table border="1" style="text-align: center;"> <tr><td>GND</td><td>GND</td><td>GND</td><td>GND</td><td>GND</td><td>GND</td></tr> <tr><td>GND</td><td>GND</td><td>GND</td><td>GND</td><td>GND</td><td>GND</td></tr> <tr><td>GND</td><td>GND</td><td>GND</td><td>GND</td><td>GND</td><td>GND</td></tr> <tr><td>GND</td><td>GND</td><td>GND</td><td>GND</td><td>GND</td><td>GND</td></tr> <tr><td>GND</td><td>GND</td><td>GND</td><td>GND</td><td>GND</td><td>GND</td></tr> </table> </div> <div style="border: 1px solid black; padding: 10px; width: fit-content; margin: 10px auto;"> <p>TOPVIEW</p> </div> <div style="text-align: center; margin: 10px auto;"> <p>388 PBGA JAN. 20 1998</p> </div>																																		GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	CJ2	DQM2	PDAT76	8
GND	GND	GND	GND	GND																																			GND																																		
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7	NC	NC	NC	NC																		<div style="border: 1px solid black; padding: 10px; width: fit-content; margin: 0 auto;"> <p>TICKET TO RIDE IV (SGRAM MEMORY) (PCI)</p> </div> <div style="border: 1px solid black; padding: 10px; width: fit-content; margin: 10px auto;"> <table border="1" style="text-align: center;"> <tr><td>GND</td><td>GND</td><td>GND</td><td>GND</td><td>GND</td><td>GND</td></tr> <tr><td>GND</td><td>GND</td><td>GND</td><td>GND</td><td>GND</td><td>GND</td></tr> <tr><td>GND</td><td>GND</td><td>GND</td><td>GND</td><td>GND</td><td>GND</td></tr> <tr><td>GND</td><td>GND</td><td>GND</td><td>GND</td><td>GND</td><td>GND</td></tr> <tr><td>GND</td><td>GND</td><td>GND</td><td>GND</td><td>GND</td><td>GND</td></tr> </table> </div> <div style="border: 1px solid black; padding: 10px; width: fit-content; margin: 10px auto;"> <p>TOPVIEW</p> </div> <div style="text-align: center; margin: 10px auto;"> <p>388 PBGA JAN. 20 1998</p> </div>																	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	PDAT76	PDAT75	PDAT74	PDAT73	7
GND	GND	GND	GND	GND																																			GND																																		
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GND	GND	GND	GND	GND	GND																																																																				
6	AD31	AD30	AD29	VDD3	<div style="border: 1px solid black; padding: 10px; width: fit-content; margin: 0 auto;"> <p>TICKET TO RIDE IV (SGRAM MEMORY) (PCI)</p> </div> <div style="border: 1px solid black; padding: 10px; width: fit-content; margin: 10px auto;"> <table border="1" style="text-align: center;"> <tr><td>GND</td><td>GND</td><td>GND</td><td>GND</td><td>GND</td><td>GND</td></tr> <tr><td>GND</td><td>GND</td><td>GND</td><td>GND</td><td>GND</td><td>GND</td></tr> <tr><td>GND</td><td>GND</td><td>GND</td><td>GND</td><td>GND</td><td>GND</td></tr> <tr><td>GND</td><td>GND</td><td>GND</td><td>GND</td><td>GND</td><td>GND</td></tr> <tr><td>GND</td><td>GND</td><td>GND</td><td>GND</td><td>GND</td><td>GND</td></tr> </table> </div> <div style="border: 1px solid black; padding: 10px; width: fit-content; margin: 10px auto;"> <p>TOPVIEW</p> </div> <div style="text-align: center; margin: 10px auto;"> <p>388 PBGA JAN. 20 1998</p> </div>																																		GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	VDD3	PDAT74	PDAT73	PDAT72	6
GND	GND	GND	GND	GND																																			GND																																		
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5	AD28	AD27	AD26	AD25																		<div style="border: 1px solid black; padding: 10px; width: fit-content; margin: 0 auto;"> <p>TICKET TO RIDE IV (SGRAM MEMORY) (PCI)</p> </div> <div style="border: 1px solid black; padding: 10px; width: fit-content; margin: 10px auto;"> <table border="1" style="text-align: center;"> <tr><td>GND</td><td>GND</td><td>GND</td><td>GND</td><td>GND</td><td>GND</td></tr> <tr><td>GND</td><td>GND</td><td>GND</td><td>GND</td><td>GND</td><td>GND</td></tr> <tr><td>GND</td><td>GND</td><td>GND</td><td>GND</td><td>GND</td><td>GND</td></tr> <tr><td>GND</td><td>GND</td><td>GND</td><td>GND</td><td>GND</td><td>GND</td></tr> <tr><td>GND</td><td>GND</td><td>GND</td><td>GND</td><td>GND</td><td>GND</td></tr> </table> </div> <div style="border: 1px solid black; padding: 10px; width: fit-content; margin: 10px auto;"> <p>TOPVIEW</p> </div> <div style="text-align: center; margin: 10px auto;"> <p>388 PBGA JAN. 20 1998</p> </div>																	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	CJ10	DQM10	PDAT71	PDAT70	5
GND	GND	GND	GND	GND																																			GND																																		
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4	AD24	AD23	C_BE#	GND	TREN#	VDD3	AD12	GND	AD7	AD3	VDD3	PDAT64	GND	PDAT71	PDAT70	VDD3	DQM10	GND	PDAT77	CJ6	VDD3																		PDAT74	GND	PDAT75	PDAT74	PDAT73	4																													
3	AD22	AD21	GND	AD16	DESEL#	C_BE#	AD13	AD9	NC	AD4	AD0	PA#	PDAT67	PDAT70	PDAT69	PDAT68	PDAT67	PDAT66	PDAT65	PDAT64	DQM9																		PDAT70	PDAT73	CJ11	GND	CS92	CS93	3																												
2	GND	GND	AD18	C_BE#	FRW#	P#	AD14	AD10	C_BE#	AD5	AD1	PC#	PDAT66	PDAT69	CJ8	PDAT68	PDAT67	PDAT66	PDAT65	PDAT64	PDAT63																		PDAT62	DQM8	PDAT61	GND	PDAT62	2																													
1	GND	AD20	AD19	AD17	RD#	STOP#	AD15	AD11	AD8	AD6	AD2	EDT#	PDAT65	PDAT68	DQM8	PDAT67	PDAT66	CJ0	PDAT74	PDAT73	PDAT69																		PDAT61	PDAT65	PDAT60	GND	GND	1																													
	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	T	U	V	W	Y	AA	AB	AC	AD	AE	AF																																															

3.4 SGRAM AGP Configuration (Top View)

	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	T	U	V	W	Y	AA	AB	AC	AD	AE	AF	
26	GND	GND	EMGRN#	MDLK_OUT	DSF	RLLAGN_SH	NC	RND	RND	PLUSS_M	RND	DE_CLK	PDAT83	PDAT83	CJ5	PDAT128	PDAT122	C6	PDAT83	DDM4	PDAT118	PDAT112	VE#	C6	GND	GND	26
25	VSNC	GND	DDC	EMREQ#	PLUSS_SH	PLUSS_SH	MDLK_N	RND	RND	RND	DDM7	PDAT82	PDAT82	DDM5	PDAT128	PDAT122	DDM6	PDAT82	PDAT82	PDAT115	PDAT115	PDAT112	DDM6	GND	GND	GND	25
24	HSYNC	BLANK	GND	LTST	PA#	RND	RLBAS_SH	RND	RND	RND	C7	PDAT81	PDAT81	PDAT127	PDAT124	PDAT123	PDAT85	PDAT85	C14	PDAT115	PDAT114	PDAT86	PDAT86	GND	CS90	CS91	24
23	RED	REF	BLLE	GND	CS#	VDD3	PLLLP2_S#	RND	GND	PLUSS_M	VDD3	PDAT80	PDAT80	GND	PDAT122	VDD3	PDAT84	PDAT84	GND	PDAT117	VDD3	PDAT84	GND	PDAT83	PDAT82	PDAT81	23
22	DMAGND	RGB_RET	GREEN	DMAGND																		PDAT80	CJ3	DDM13	PDAT111	22	
21	DDC2_CLK	PWR#	RND	VDD3																		VDD3	PDAT110	PDAT108	PDAT108	PDAT103	21
20	PLUSS_P#	REFCLK	PLLLP2_P#	PC#																		PDAT101	PDAT108	PDAT108	PDAT104	20	
19	PLUSS_P#	RLLAGN_P#	LD_CLK	GND																		C14	DDM1	PDAT89	PDAT88	19	
18	SECLK	PROC_MON	PA7	RLBAS_P#																		GND	PDAT87	PDAT86	PDAT85	18	
17	PSFT	RL_EP	PA6	PA6																		CJ2	PDAT84	PDAT83	PDAT82	17	
16	PA4	PA3	PA2	VDD3																		VDD3	DDM12	PDAT103	PDAT103	16	
15	PA1	PA0	PD7	PD8																		PDAT101	PDAT102	PDAT89	PDAT88	15	
14	PD5	PD4	RLUSS_AG	GND																		PDAT89	PDAT86	C6	DDM6	14	
13	PD2	PD1	PD3	RL2TST																		GND	PDAT81	PDAT80	PDAT28	13	
12	PD0	PLUSS_AG	HLK	INT	PDAT28	PDAT27	PDAT26	PDAT25	12																		
11	RS#	REQ#	GN#	VDD3	VDD3	PDAT20	C11	DDM11	11																		
10	SD	ST1	ST2	PIPE#	PDAT85	PDAT84	PDAT83	PDAT82	10																		
9	SB0	SB1	SB2	GND	PDAT81	PDAT80	PDAT80	PDAT88	9																		
8	SB3	SB4	SB5	SB4	GND	C2	DDM2	PDAT23	8																		
7	SB6	SB6	SB7	ADTB1	PDAT22	PDAT21	PDAT20	PDAT19	7																		
6	AD81	AD80	AD89	VDD3	VDD3	PDAT18	PDAT17	PDAT16	6																		
5	AD8	AD7	AD6	AD5	CJ0	DDM0	PDAT87	PDAT88	5																		
4	AD4	AD3	C.BE#	GND	TDM#	VDD3	AD12	GND	AD7	AD3	VDD3	PDAT64	GND	PDAT71	PDAT01	VDD3	DDM0	GND	PDAT77	C9	VDD3	PDAT14	GND	PDAT85	PDAT84	PDAT83	4
3	AD2	AD1	GND	AD16	DESEL#	C.BE#	AD13	AD9	ADSTERG	AD4	AD0	PWR#	PDAT67	PDAT70	PDAT00	PDAT04	PDAT07	PDAT73	PDAT76	DDM6	PDAT10	PDAT13	C11	GND	CS82	CS83	3
2	GND	GND	AD18	C.BE#	FRM#	PAR	AD14	AD10	C.BE#	AD5	AD1	PO#	PDAT66	PDAT69	C8	PDAT03	PDAT06	PDAT72	PDAT75	PDAT79	PDAT09	PDAT12	DDM1	PDAT81	GND	PDAT82	2
1	GND	AD20	AD19	AD17	IFD#	STOP#	AD15	AD11	AD6	AD2	DDTEST	PDAT65	PDAT68	DDM8	PDAT02	PDAT05	C0	PDAT74	PDAT78	PDAT08	PDAT11	PDAT15	PDAT80	GND	GND	1	
	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	T	U	V	W	Y	AA	AB	AC	AD	AE	AF	



3.5 WINDOW RAM PCI Configuration (Top View)

	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	T	U	V	W	Y	AA	AB	AC	AD	AE	AF		
26	GND	GND	BAGN17	SQLK	CE#_SF	FLAQN_S1	SF0	RWD0	RWD6	PLLVDD_M	RA7	DE_CLK	PDAT63	PDAT59	BEH15	PDAT128	PDAT122	BEH6	PDAT53	PDAT46	BEL14	PDAT118	PDAT113	CASH	BEH6	GND	26	
25	VSINC	GND	DDC	EMREQ	PLLVDD_S1	PLLVSS_S1	MCLK	RWD9	RWD4	RWD8	BEL7	PDAT62	PDAT58	BEL15	PDAT122	PDAT121	BEL6	PDAT52	PDAT48	PDAT118	PDAT115	PDAT112	PDAT47	BEL5	GND	GND	25	
24	HSMC	BLANK	GND	CLIST	SF1	RWD2	ULBAS_S1	RWD3	RWD1	RWD10	BEH9	PDAT61	PDAT57	PDAT122	PDAT124	PDAT121	PDAT55	PDAT51	BEH4	PDAT118	PDAT114	PDAT46	PDAT45	GND	RAS0	RAS1	24	
23	RED	REF	BLUE	GND	SF2	VDD1	PLLV2_S1	RWD6	GND	PLLVSS_M	VDD3	PDAT60	PDAT56	GND	PDAT123	VDD3	PDAT54	PDAT50	GND	PDAT117	VDD3	PDAT44	GND	PDAT43	PDAT42	PDAT41	23	
22	DACGND	RGB_FET	GREEN	DACVDD	<div style="border: 1px solid black; padding: 10px; width: fit-content; margin: 0 auto;"> <p>TICKET TO RIDE IV (WRAM MEMORY) (PCI)</p> <div style="border: 1px solid black; padding: 5px; width: 100px; margin: 10px auto; text-align: center;">TOP VIEW</div> <p>388 FBGA</p> <p>JAN. 20 1998</p> </div>																		PDAT40	BEH3	BEL3	PDAT111	22	
21	DDC2_CLK	PWR#	PDF#	VDD3																			VDD3	PDAT110	PDAT108	PDAT108	PDAT108	21
20	PLLVSS_P1	CRTCLK	PLLV2_P1	PCSH																			PDAT107	PDAT106	PDAT106	PDAT104	20	
19	PLLVDD_P1	FLAQN_P1	LD_CLK	GND																			BEH4	BEL4	PDAT39	PDAT38	19	
18	SECLK	PROC_MON	PAV	ULBAS_P1																			GND	PDAT37	PDAT36	PDAT36	18	
17	PSFT	PLL_BP	PA6	PA6																			BEH2	PDAT34	PDAT33	PDAT32	17	
16	PA4	PA5	PA2	VDD3																			VDD3	BEL2	PDAT103	PDAT102	16	
15	PA1	PA0	PDF	PCB																			PDAT101	PDAT100	PDAT99	PDAT98	15	
14	PD5	PD4	PLLVDD_A1	GND																			PDAT97	PDAT96	BEH3	BEL3	14	
13	PD2	PD1	PCB	PLL2TSF																			GND	PDAT91	PDAT90	PDAT29	13	
12	PD0	PLLVSS_A1	HCLK	INT	PDAT28	PDAT27	PDAT26	PDAT25	12																			
11	RST#	REQ#	GN#	VDD3	VDD3	PDAT24	BEH1	BEL1	11																			
10	NC	NC	NC	ICBEL	PDAT95	PDAT94	PDAT93	PDAT92	10																			
9	NC	NC	NC	GND	PDAT91	PDAT90	PDAT89	PDAT88	9																			
8	NC	SPARE	NC	NC	GND	BEH2	BEL2	PDAT23	8																			
7	NC	NC	NC	NC	PDAT22	PDAT21	PDAT20	PDAT19	7																			
6	AD31	AD30	AD29	VDD3	VDD3	PDAT18	PDAT17	PDAT16	6																			
5	AD28	AD27	AD26	AD25	BEH10	BEL10	PDAT97	PDAT96	5																			
4	AD24	AD23	C_BE3#	GND	TRDN#	VDD3	AD12	GND	AD7	AD3	VDD3	PDAT64	GND	PDAT71	PDAT71	VDD3	BEL0	GND	PDAT77	BEH9	VDD3	PDAT14	GND	PDAT95	PDAT94	PDAT93	4	
3	AD22	AD21	GND	AD16	DBSEL#	C_BE1#	AD13	AD9	NC	AD4	AD0	SCEN#	PDAT67	PDAT70	PDAT70	PDAT74	PDAT77	PDAT76	BEL9	PDAT10	PDAT10	BEH1	GND	RAS0	RAS0	3		
2	GND	GND	AD16	C_BE2#	TRNEN#	PWR	AD14	AD10	C_BE0#	AD5	AD1	SCEN#	PDAT66	PDAT68	BEH8	PDAT70	PDAT75	PDAT72	PDAT75	PDAT75	PDAT75	PDAT12	BEL1	PDAT91	GND	PDAT92	2	
1	GND	AD20	AD19	AD17	REQ#	STOR#	AD15	AD11	AD8	AD5	AD2	ICDTEST	PDAT65	PDAT66	BEL8	PDAT70	PDAT75	BEH9	PDAT74	PDAT76	PDAT76	PDAT11	PDAT15	PDAT90	GND	GND	1	
A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	T	U	V	W	Y	AA	AB	AC	AD	AE	AF			

3.6 WINDOW RAM AGP Configuration (Top View)

	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	T	U	V	W	Y	AA	AB	AC	AD	AE	AF		
26	GND	GND	BMGRT#	SOLK	CE#_SF	PLAEN_SY	SF0	RVD0	RVD6	PLLVDD_M	RVD7	DE_CLK	PDAT63	PDAT50	BEH15	PDAT128	PDAT122	BEH6	PDAT33	PDAT40	BEL14	PDAT118	PDAT113	CASH	BEH4	GND	GND	26
25	VS17C	GND	DDC	EMREQ#	PLLVDD_SY	PLLVSS_SY	MCLK	RVD8	RVD4	RVD8	BEL7	PDAT62	PDAT58	BEL15	PDAT125	PDAT121	BEL6	PDAT32	PDAT46	PDAT119	PDAT115	PDAT112	PDAT61	BEL5	GND	GND	25	
24	HSYNC	CLANK	GND	CLTST	SF1	RVD2	PLLBAS_SY	RVD3	RVD1	RVD10	BEH7	PDAT61	PDAT57	PDAT127	PDAT124	PDAT123	PDAT55	PDAT51	BEH4	PDAT118	PDAT114	PDAT66	PDAT65	GND	FRSG0	FRSG1	24	
23	RED	REF	BLE	GND	SF2	VDD3	PLLV2_SY	RVD6	GND	PLLVSS_M	VDD3	PDAT60	PDAT56	GND	PDAT123	VDD3	PDAT54	PDAT50	GND	PDAT117	VDD3	PDAT44	GND	PDAT43	PDAT42	PDAT41	23	
22	DVDDGND	RGB_FET	GREEN	DVDD000	<div style="border: 1px solid black; padding: 5px; width: fit-content; margin: 0 auto;"> TICKET TO RIDE IV (WRAM MEMORY) (AGP) </div> <div style="border: 1px solid black; padding: 5px; width: fit-content; margin: 10px auto;"> TOP MEW </div> <div style="border: 1px solid black; padding: 5px; width: fit-content; margin: 10px auto;"> 388 FBGA JAN. 20 1998 </div>																		PDAT60	BEH13	BEL13	PDAT111	22	
21	DDC2_CLK	PVRF#	RFDF	VDD3																			VDD3	PDAT107	PDAT103	PDAT103	PDAT108	21
20	PLLVSS_PM	CRTOCLK	PLLV2_PM	PC#																			PDAT107	PDAT106	PDAT105	PDAT104	20	
19	PLLVDD_PM	PLLVGN_PM	LD_CLK	GND																			BEH4	BEL4	PDAT39	PDAT38	19	
18	SECLK	PRDC_MDR	PA7	PLLBAS_PM																			GND	PDAT37	PDAT35	PDAT35	18	
17	RSFT	PLL_SP	PA6	PA6																			BEH12	PDAT34	PDAT32	PDAT32	17	
16	PA4	PA3	PA2	VDD3																			VDD3	BEL12	PDAT109	PDAT104	16	
15	PA1	PA0	PD7	PC6																			PDAT101	PDAT100	PDAT99	PDAT98	15	
14	PD5	PD4	PLVDD_AG	GND																			PDAT97	PDAT96	BEH6	BEL3	14	
13	PD2	PD1	PC6	PLL2TST																			GND	PDAT91	PDAT30	PDAT29	13	
12	PD0	PLLVSS_AG	HCLK	INT	PDAT28	PDAT27	PDAT26	PDAT25	12																			
11	RS7#	REQ#	GN7#	VDD3	VDD3	PDAT24	BEH11	BEL11	11																			
10	ST0	ST1	ST2	PIPE#	PDAT65	PDAT64	PDAT63	PDAT62	10																			
9	SB40	SB41	SB42	GND	PDAT61	PDAT60	PDAT59	PDAT58	9																			
8	SB43	SB44	SB45	SB44	GND	BEH2	BEL2	PDAT23	8																			
7	SB46	SB47	SB48	AD5TB1	PDAT22	PDAT21	PDAT20	PDAT19	7																			
6	AD31	AD30	AD29	VDD3	VDD3	PDAT18	PDAT17	PDAT16	6																			
5	AD28	AD27	AD26	AD25	BEH10	BEL10	PDAT87	PDAT88	5																			
4	AD24	AD23	C.BE#	GND	TRD#	VDD3	AD22	GND	AD7	AD5	VDD3	PDAT64	GND	PDAT77	PDAT01	VDD3	BEL0	GND	PDAT77	BEH8	VDD3	PDAT14	GND	PDAT85	PDAT84	PDAT83	4	
3	AD22	AD21	GND	AD16	DESEL#	C.BE1#	AD13	AD9	AD5TB0	AD4	AD0	SCEN#	PDAT67	PDAT70	PDAT00	PDAT04	PDAT07	PDAT75	PDAT76	BEL9	PDAT10	PDAT13	BEH1	GND	FRSG2	FRSG3	3	
2	GND	GND	AD18	C.BE2#	FRAME#	PRR	AD14	AD10	C.BE#	AD5	AD1	SCEN#	PDAT66	PDAT69	BEH8	PDAT03	PDAT06	PDAT72	PDAT75	PDAT79	PDAT09	PDAT12	BEL1	PDAT81	GND	PDAT82	2	
1	GND	AD20	AD19	AD17	RDY#	STOP#	AD15	AD11	AD6	AD6	AD2	DDTEST#	PDAT65	PDAT68	BEL8	PDAT02	PDAT05	BEH0	PDAT74	PDAT78	PDAT08	PDAT11	PDAT15	PDAT80	GND	GND	1	
	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	T	U	V	W	Y	AA	AB	AC	AD	AE	AF		



3.6 Configuration Pins

As IMAGINE 128SM is being reset during the power up sequence, the logic states of **32 configuration pins** are used to configure specific functions. The values on configuration pins are latched into XXXXSM on the rising edge of the RST# signal and may be read at any time in the ID or CONFIG registers. The notation "CP[0]" corresponds to the logic state on CONFIGURATION_PIN[0] at the rising edge of RST#. Likewise, CP[27:26] would correspond to CONFIGURATION_PIN[27:26].

The configuration pins are **not** dedicated pins. They actually correspond to other functional pins of the chip as follows:

```
CONFIGURATION_PIN[15:0] use BEh[15:0] pins
CONFIGURATION_PIN[23:16] use PD[7:0] pins
CONFIGURATION_PIN[31:24] use PA[7:0] pins
```

The PA and PD pins are internally pulled down to logic zero. A value of logic one can be achieved on CP[31:16] through the use of an external pull up resistor.

The BEh pins are internally pulled up to logic one. A value of logic zero can be achieved on CP[15:0] through the use of an external pull down resistor.

Добавлено примечание ([NNCC1]):

PINS	NAME	VALUE	DESCRIPTION
CP[15:0]	SVID		Subsystem Vendor ID This 16 bit field is the PCI Subsystem Vendor ID. It can be read at address 0x2C in PCI configuration space. This field will correspond to CP[15:0] unless CP[16] is set to zero, in which case the SVID will be set to 0x105D; the vendor ID for Number Nine Visual Technology
CP[16]	SSEL	0 1	Subsystem Vendor ID Select This bit allows the Subsystem Vendor ID fields in PCI configuration space to be set according to CP[15:0]. Subsystem Vendor ID = 0x105D; Subsystem Vendor ID selected by CP[15:0]
CP[22:17]	SID		Subsystem ID This 6 bit field corresponds to the lower 6 bits of the PCI Subsystem ID; the upper 10 bits of the SID will always be zero. It can be read at address 0x2E in PCI configuration space. This field will always correspond to CP[22:17] (regardless of the value of CP[16]).
CP[23]	HBT	0 1	Host Bus Type AGP Bus PCI Bus It can be read in ID register bit[3]

PINS	NAME	VALUE	DESCRIPTION
CP[24]	SGR	1 0	Local memory type: SGRAM WINDOW RAM It can be read in CONFIG2 REGISTER bit[1]
CP[25]	IDAC	0 1	Internal RAMDAC enable External RAMDAC enabled Internal RAMDAC enabled It can be read in CONFIG2 REGISTER bit[0] This configuration pin selects default value (after reset) of CONFIG2 REGISTER bit[0].
CP[27:26]	DDEN	00 01 10 11	Local buffer memory density/type reserved 256K bits by N memory chips 16MBit chips (512K bits by 32) - if SGRAM memory 256K bits in interleaved mode - if WINDOW RAM Reserved It can be read in ID REGISTER bits[9:8]
CP[28]	CLASS	0 1	PCI Device Sub-Class VGA Other It can be read in ID REGISTER bit[28] Setting this configuration pin to a 1 disables the VGA component (i.e., VGA decodes will never occur regardless of VGA_CTRL settings).
CP[29]	EE	0 1	EPROM Boot Enable: This pin provides the power-on default value for CONFIG1[13], which is the EPROM (RBASE_E) decode enable. EPROM Boot Decode disabled EPROM Boot Decode Enabled It can be read in ID REGISTER bit[30]



CP[31:30]	BASE0/1		<p>PCI Base 0 Address Register Size and PCI Base 1 Address Register Size</p> <p>00 4 Megabyte Memory Space Requested 01 8 Megabyte Memory Space Requested 10 16 Megabyte Memory Space Requested 11 32 Megabyte Memory Space Requested</p> <p>These two bits select memory space requested for Linear Memory Window 0 and 1. Both memory windows request same amount of memory.</p> <p>Value of CP[31:30] can be read in ID REGISTER bits[7:6] or ID REGISTER bits[12:11]</p>
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