4

PCI & AGP CONFIGURATION

Section 4: PCI CONFIGURATION

4.1 PCI & AGP Configuration Space

To be both PCI and AGP compliant, IMAGINE 128 implements the required 256 bytes of configuration space. This configuration space allows configuration of the device by the system BIOS at boot time. This is sometimes referred to as "plug and play". These registers are read from and written to via special PCI configuration cycles.

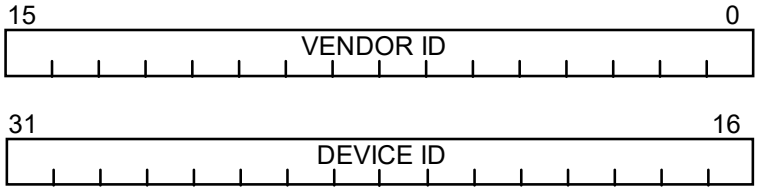
4.2 IMAGINE 128 PCI Registers

The diagram on the following page illustrates the PCI configuration registers implemented within IMAGINE 128. The values in parentheses indicate power up default values except in the case of the base registers, where IMAGINE 128 register mapping is indicated.

Greyed out fields indicate unimplemented PCI functions and will always be read back as a zero value.

4.2.1 PCI Configuration Register 0 (00h)

Type: PCI configuration read only



Bits	Name	Default	Function
[15:0]	VENDOR ID	105Dh	Company Identifier for Number Nine
[31:16]	DEVICE ID	5348h	IMAGINE 128 Identifier

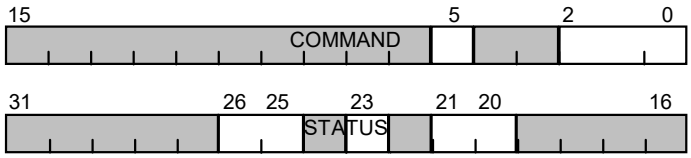
31 16	15 0	
Device ID (5348h)	Vendor ID (105Dh)	00h
Status	Command	04h
Class Code	Revision ID (00h)	08h
BIST / Header Type (00h)	Latency Tmr / Cache Line Sz	0Ch
Base Register 0 (MW0_AD)		10h
Base Register 1 (MW1_AD)		14h
Base Register 2 (XYC_AD)		18h
RESERVED		1Ch
Base Register 3 (RBASE_X)		20h
Base Register 4 (IO_CONFIG)		24h
RESERVED		28h
Subsystem ID	Subsystem Vendor ID	2Ch
Expansion ROM Base (RBASE_E)		30h
Capabilities Pointer		34h
RESERVED		38h
Max_LAT / Min_Gnt / Interrupt Pin (01h) / Interrupt Line (XXh)		3Ch
RESERVED		40h - 7Ch
AGP Capabilities ID		80h
AGP Status		84h
AGP Command		88h
RESERVED		8Ch - FCh

IMAGINE 128 CONFIGURATION REGISTERS

<Tom to provide power management capability structure>

4.2.2 PCI Configuration Register 1 (04h)

Type: PCI configuration read write

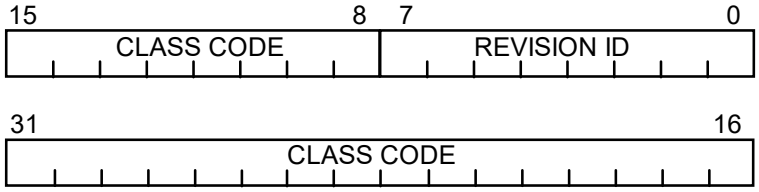


Bits	Name	Default	Function
[15:0]	COMMAND	0020h	PCI Command Register
0	I/O Space	0	Allows IMAGINE 128 to respond to I/O cycles when set to 1
1	Memory Space	0	Allows IMAGINE 128 to respond to Memory cycles when set to 1
2	Bus Master	0	Bus Master enable (read/write)
5	VGA Snooping	0	Enables Palette snooping when set to 1
[31:16]	STATUS	02B0h	PCI Status Register
[20]	Capabilities List	1	Device implements a Capabilities list (read_only)
[21]	66 MHz	1	66 MHz capable (read_only)
[23]	Fast back to back	1	Indicates that IMAGINE 128 supports fast back to back transactions (**read only**)
[26:25]	DEVSEL Timing	01	These two bits indicate that IMAGINE 128 will assert the PCI DEVSEL signal within the "MEDIUM" time frame. **(read only)**

4.2.3 PCI Configuration Register 2 (08h)

Type: PCI configuration read only

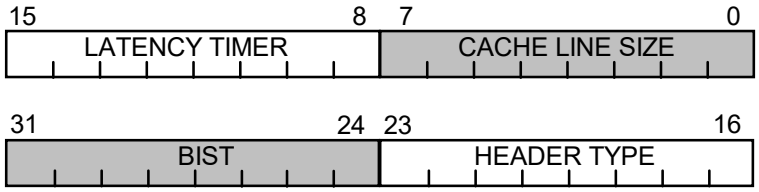
The sub-class field of the class code register is determined by configuration jumper [28]. All other fields in this register are hardwired to their default values.



Bits	Name	Default	Function
[7:0]	REVISION ID		IMAGINE 128 Revision Number
[31:8]	CLASS CODE		PCI DEVICE CLASS
[31:24]	Base Class	03h	IMAGINE 128 will always identify itself as a display controller which is base class 3.
[23:16]	Sub Class		The two sub-classes for display controllers supported by IMAGINE are:
	CP[28] = 0	00h	VGA compatible controller
	CJ[28] = 1	80h	Other Display Controller
[15:8]	Programming Interface	00h	Always defined as 0

4.2.4 PCI Configuration Register 3 (0Ch)

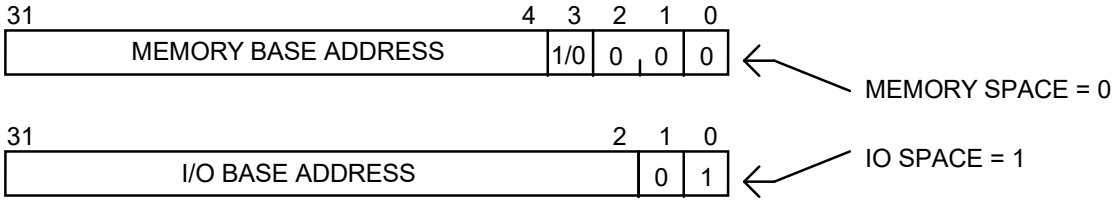
Type: PCI configuration read only



Bits	Name	Default	Function
[15:8]	LATENCY TIMER	???	PCI Bus Master Minimum Clock Count for a Burst Transaction before another master can gain bus grant.
[23:16]	HEADER TYPE	00h	Indicates that IMAGINE 128 is a single function device with the default layout of configuration space.

4.3 IMAGINE 128™ PCI Base Address Registers

To allow for maximum configurability, PCI configuration space contains five base address registers, and one EPROM base address register. A PCI compliant device such as IMAGINE 128™ uses the base registers to inform the system of its memory and I/O requirements. The system then allocates memory and I/O resources at boot time to all PCI devices. The base address registers are loaded by the system to indicate which memory or I/O locations a board has been assigned. The general format of a base address register is shown below.

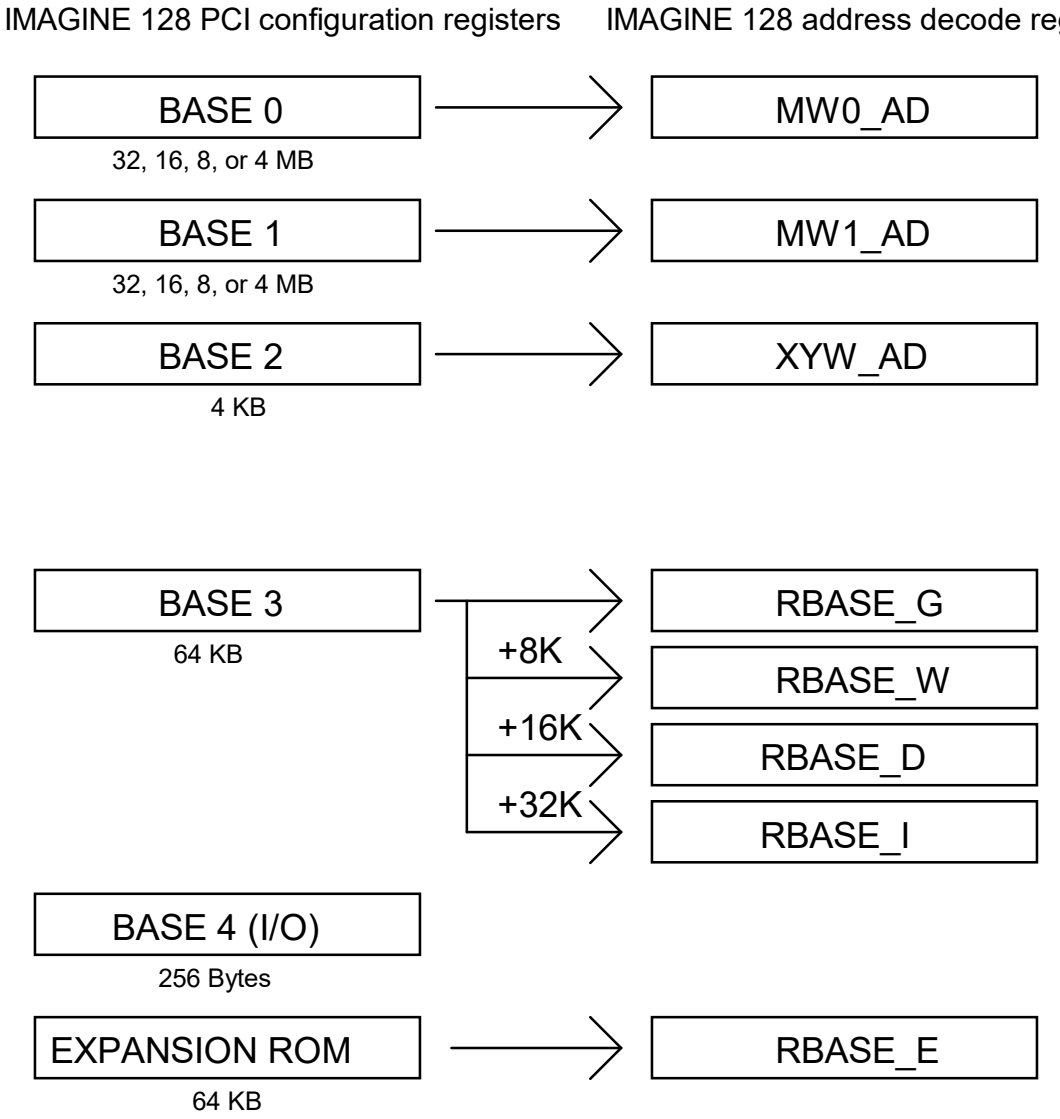


A PCI device sets bit 0 in a base register to one for I/O mapping and to zero for memory mapping. Bit 0 is read only. If the register is set to I/O, bit 1 must be read back as zero. The remaining bits (31:2) are used to specify the I/O address to which the device will respond. If the register is set to memory mapping, IMAGINE 128™ will set bits 1 and 2 both to zero indicating that the allocated memory space may be anywhere in 32 bit address space. Bit 3 indicates whether the area of memory corresponding to the base address register is pre-fetchable. Bit 3 is set to zero for all base registers except for the linear memory windows registers, where it is hardwired to 1.

The amount of memory or I/O space that IMAGINE 128™ requests from the host is determined by the number of upper order base address bits that are implemented. To request enough memory for a four megabyte memory window, for example, IMAGINE 128™ would implement base address bits (31:22) with the remaining bits (21:4) hardwired to zero. After allocating all PCI memory requests, the host would assign a four megabyte segment of memory to IMAGINE 128™ by setting bits (31:22) to the assigned memory space.

Each base register will allocate memory or I/O space for a specific IMAGINE 128™ function. IMAGINE 128™ allocates two base registers for linear memory windows, one for the DRAWING ENGINE CACHE, one for memory mapped registers, one for I/O mapped registers, and one for memory mapped EPROM. **When a PCI base address register is written, the write will be shadowed to the associated internal register.** The diagram on the following page illustrates how IMAGINE 128™'s PCI configuration registers are shadowed to IMAGINE 128™'s address decode registers. For example, base address register 0 allocates memory for linear memory window 0. When the PCI system BIOS writes to base register 0, the write will also occur to MW0_AD, the starting address of memory window 0. The first 3 PCI address registers are shadowed to MW0_AD, MW1_AD, XYW_AD(A), respectively. (*XYW_AD[B] is a reserved base address)*. Under most circumstances, there is no need to alter the values that have been written to MW0_AD, MW1_AD, XYW_AD(A), These registers are, however, accessible in IMAGINE 128™ memory space. The size of base registers 0 and 1 is determined by configuration pins (4, 8, 16, or 32 megabytes). **The size of other base registers is fixed**.

When base address register 4 is written, the value is directly shadowed to RBASE_G. RBASE_W will be written with the value in base 4 plus an offset of 8 kilobytes. RBASE_D, RBASE_C, and RBASE_I are written as shown on the following page. RBASE_G is the pointer to the starting memory location of the global register block. RBASE_W points to the memory windows registers. RBASE_D points to the drawing engine. RBASE_I points to the interrupt registers. The "RBASE" registers are I/O mapped and pointed to by the value in base address register 4.

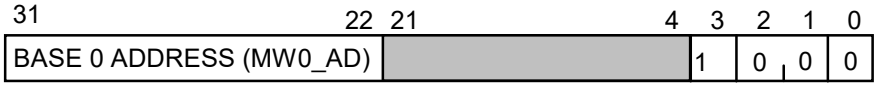


IMAGINE 128's configuration registers are shadowed to IMAGINE 128 address decode registers as indicated by the arrows

PCI Base Address Register 0 (10h)

Type: PCI configuration read write

This base address register requests 4, 8, 16, or 32 megabytes of memory space based on configuration pins[31:30]. It corresponds to the starting address of linear memory window 0. When this register is written, MW0_AD will also be written.

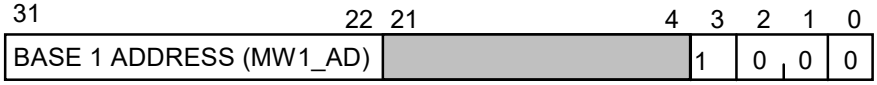


Bits	Name	Default	Function
[2:0]	Base Address Type	0x0	Indicates that base address register 0 corresponds to a memory device **(read only)**
[3]	Memory Space pre-fetchable	1	Linear Memory Window 0 is pre-fetchable **(read only)**
[31:22] [31:23] [31:24] [31:25]	Base Address 0 CP[31:30] = 00 Base Address 0 CP[31:30] = 01 Base Address 0 CP[31:30] = 10 Base Address 0 CP[31:30] = 11		Address decode for 4 megabytes Address decode for 8 megabytes Address decode for 16 megabytes Address decode for 32 megabytes

PCI Base Address Register 1 (14h)

Type: PCI configuration read write

This base address register requests 4, 8, 16, or 32 megabytes of memory space based on configuration pins[31:30]. It corresponds to the starting address of linear memory window 1. When this register is written, MW1_AD will also be written.

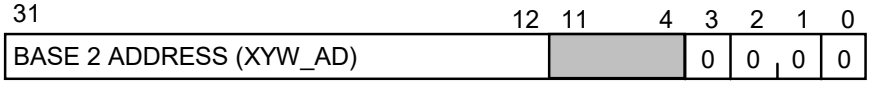


[2:0]	Base Address Type	0x0	Indicates that base address register 1 corresponds to a memory device **(read only)**
[3]	Memory Space pre-fetchable	1	Linear Memory Window 1 is pre-fetchable **(read only)**
[31:22] [31:23] [31:24] [31:25]	Base Address 1 CP[31:30] = 00 Base Address 1 CP[31:30] = 01 Base Address 1 CP[31:30] = 10 Base Address 1 CP[31:30] = 11		Address decode for 4 megabytes Address decode for 8 megabytes Address decode for 16 megabytes Address decode for 32 megabytes

4.3.3 PCI Base Address Register 2 (18h)

Type: PCI configuration read write

This base address register requests 4 KB of memory. It corresponds to the starting address of the X-Y memory window for drawing engine. When this register is written, XYW_AD will also be written.



Bits	Name	Default	Function
[3:0]	Base Address Type	0x0	Indicates that base address register 2 corresponds to a non prefetchable memory device **(read only)**
[31:12]	Base Address 2		Address decode for 4 kilobytes

4.3.4 PCI Base Address Register 3 (20h)

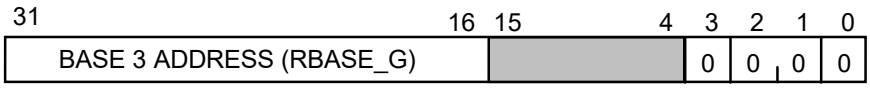
Type: PCI configuration read write

This base address register requests 64 kilobytes of memory space for the memory mapped IMAGINE 128™ registers. When this register is written, the write will also occur to RBASE_G, the base address of the Global register block. The following registers will also be loaded:

RBASE_W will be loaded with the value in RBASE_G plus 8 kilobytes

RBASE_D will be loaded with the value in RBASE_G plus 16 kilobytes

RBASE_I will be loaded with the value in RBASE_G plus 32 kilobytes

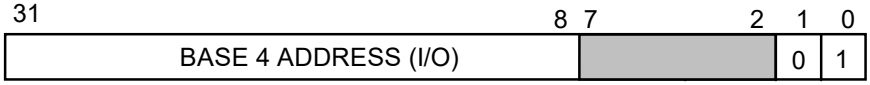


Bits	Name	Default	Function
[3:0]	Base Address Type	0x0	Indicates that base address register 3 corresponds to a non-prefetchable memory device **(read only)**
[31:16]	Base Address 3		Address decode for 64 kilobytes

4.3.5 PCI Base Address Register 4 (24h)

Type: PCI configuration read write

This base address register requests 256 bytes of I/O space for the I/O mapped IMAGINE 128™ registers. This register is not shadowed to any other registers.

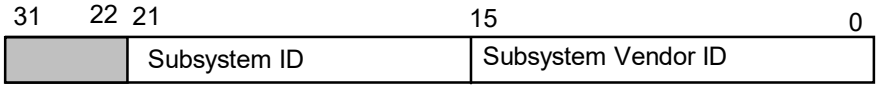


Bits	Name	Default	Function
[1:0]	Base Address Type	01	Indicates that base address register 4 corresponds to a prefetchable memory device **(read only)**

[31:8]	Base Address 4		Address decode for 256 bytes

4.3.6 SUBSYSTEM ID/SUBSYSTEM VENDOR ID (2Ch)

Type: PCI configuration read only

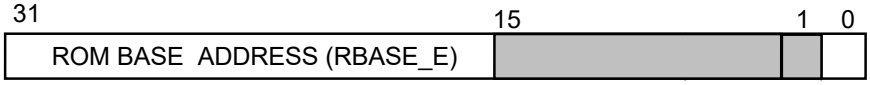


Bits	Name	Default	Function
[15:0]	Subsystem Vendor ID		Value in this register is selected by Configuration pin CP[16]. If CP[16] = 0 Subsystem Vendor ID[15:0] = 105Dh If CP[16] =1 Subsystem Vendor ID[15:0] contain settings for configuration pins CP[15:0].
[21:16]	Subsystem ID		Configuration pins CP[22:17] provide value for this 6 bit field. It may be used to get information about board configuration, other devices on the board etc. (CP[16] has no effect for this field!)

4.3.7 PCI ROM Base Address Register (30h)

Type: PCI configuration read write

The ROM base address register requests 64 kilobytes of memory space for a PROM device. When this register is written, the write will also occur to RBASE_E, the EPROM base address register. Bit 0 of this register is used by the PCI BIOS to enable or disable EPROM decode. The EPROM Enable bit in the ID register must also be set for EPROM decode to be active.

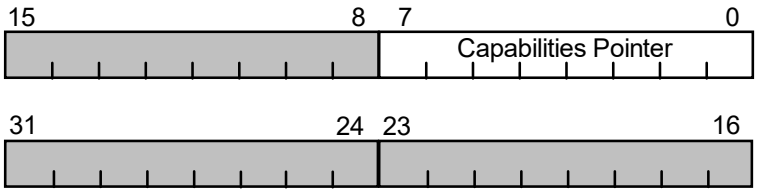


Bits	Name	Default	Function
[0]	PCI ROM Enable	0 1	Disable EPROM address decode (default) Enable EPROM address decode
[31:16]	ROM Base Address		ROM Address decode for 64 kilobytes

4.3.8 Capabilities Register (34h)

Type: PCI configuration read only

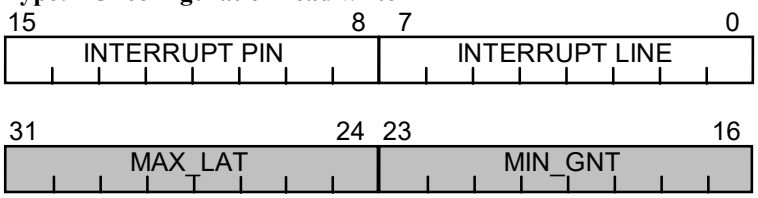
IMAGINE 128 implements a capabilities list to support its AGP features. The list is located in Configuration Space at offset 80h. The Capabilities Register contains a pointer to that list.



Bits	Name	Default	Function
[7:0]	Capabilities Pointer	80h	Pointer to a Capabilities List in Configuration Space.
[31:8]	Reserved		Reserved.

4.3.9 PCI Configuration Register 4 (3Ch)

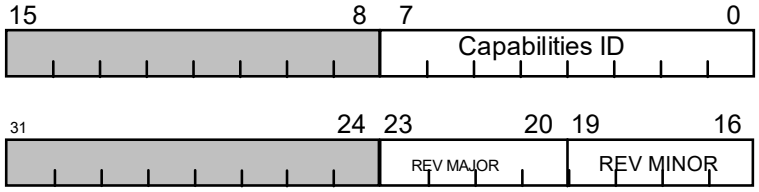
Type: PCI configuration read write



Bits	Name	Default	Function
[7:0]	INTERRUPT LINE		Indicates which input of the system interrupt controller IMAGINE 128's interrupt signal is connected to.
[15:8]	INTERRUPT PIN	01h	Indicates that IMAGINE 128's interrupt pin is connected to interrupt pin INTA#. **(read only)**

4.3.10 AGP Capabilities ID (80h)

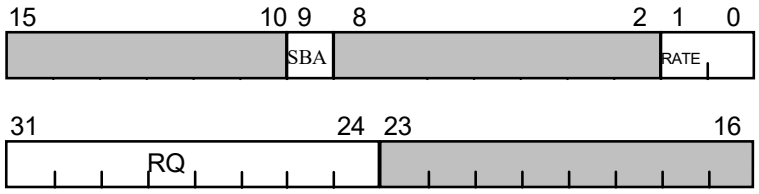
Type: AGP configuration read only



Bits	Name	Default	Function
[7:0]	Capabilities ID	02h	Identifies IMAGINE 128 as an AGP device.
[15:8]	Reserved		Reserved.
[19:16]	REV MINOR	0h	Minor AGP spec. revision that device complies to.
[23:20]	REV MAJOR	1h	Major AGP spec. revision that device complies to.
[31:24]	Reserved		Reserved

4.3.11 AGP Status (84h)

Type: AGP configuration read only



Bits	Name	Default	Function
[1:0]	Rate	11	Device supports both 1x & 2x AGP transfers.
[8:2]	Reserved		Reserved.
[9]	SBA	1	Device supports side band addressing
[23:10]	Reserved		Reserved.
[31:24]	RQ	0Fh	We can have 16 outstanding AGP requests at a time. (00h = 1; FFh = 256.)

4.3.12 AGP Command (88h)

Type: AGP configuration read write

Bits	Name	Default	Function
[1:0]	Data Rate	00	Determines AGP data transfer rate. (Set only one bit. Bit0: 1x, Bit1: 2x)
[7:2]	Reserved.		Reserved.
[8]	AGP EN	0	Enable AGP functions
[9]	SBA EN	0	Enable side band addressing
[23:10]	Reserved		Reserved.
[31:24]	RQ DEPTH	00h	Set the Request Queue depth. Note: This should not exceed 0Fh or the RQ of the corelogic.