

Hot Chips 1996

*Bringing Workstation
Graphics Performance to a
Desktop Near You*

S3 Incorporated
August 18-20, 1996



Agenda

- ViRGE/VX Marketing Slide!
- Overview of ViRGE/VX accelerator features
- 3D rendering
- Live video and MPEG YUV stream display
- C-Model and verification



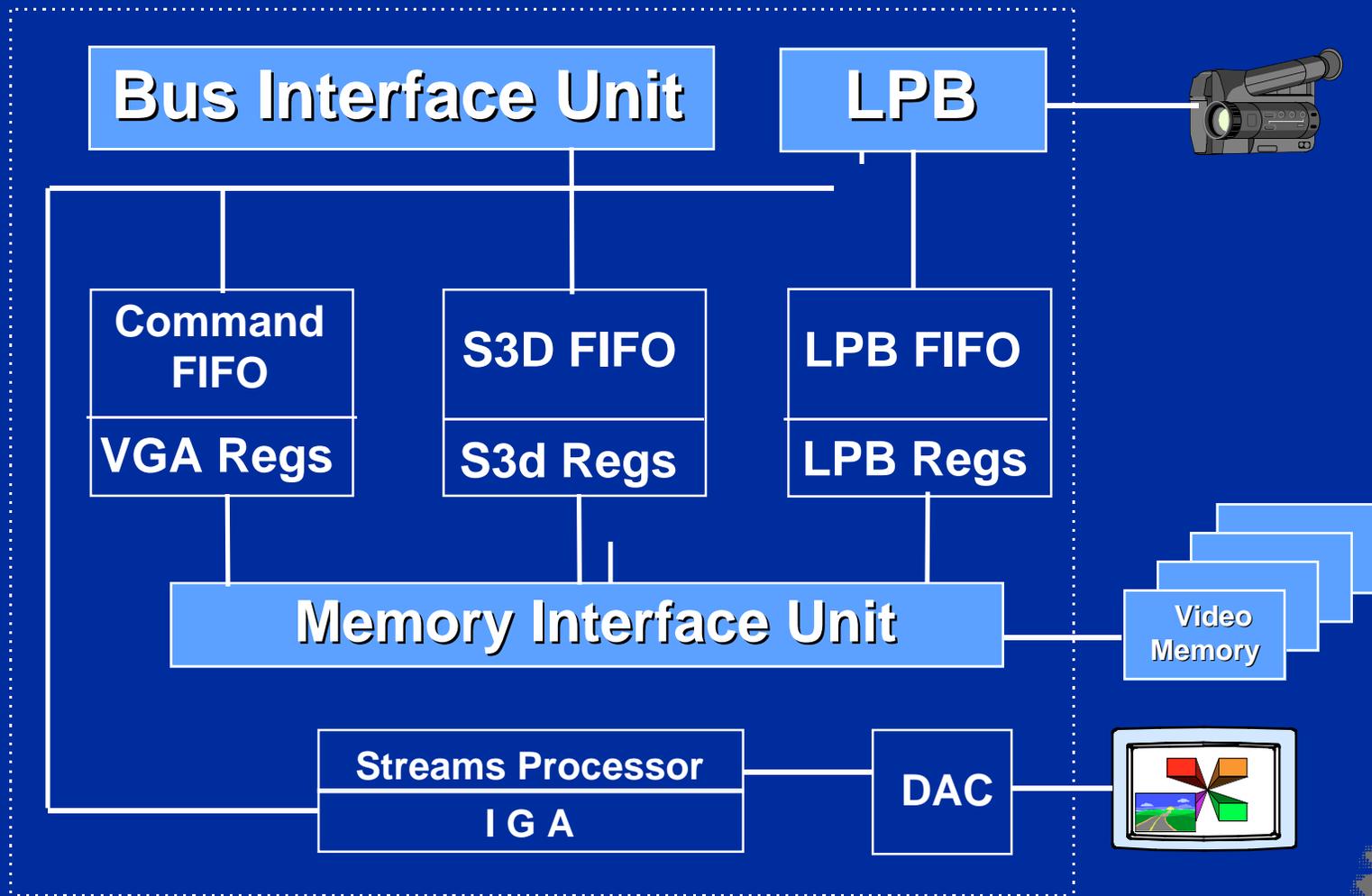
ViRGE/VX Marketing slide

The Only Marketing Slide in This Presentation!

- ViRGE / VX is the worlds only integrated NT accelerator
 - High performance 2D, Video, and 3D engine
 - Worlds only integrated 220MHz RAMDAC
 - Supports 1600x1200x16 at 85Hz!
 - 1600x1200x24 at 60Hz is achievable
- Workstation Software Support
 - OpenGL via 3D-DDI, ICD, MCD and TCD
 - NT3.51, and NT4.0



ViRGE/VX Architectural Features



Video Playback

- 2 memory display streams
 - Primary: VGA modes, 8 bit palletized; 16 and 24 bit color
 - Secondary: 8, 16, and 24 bit as well as YUV
- Secondary stream is very flexible
 - Horizontal and vertical stretching
 - Horizontal and vertical filtering
- Secondary stream can be overlaid, blended or color-keyed onto primary stream

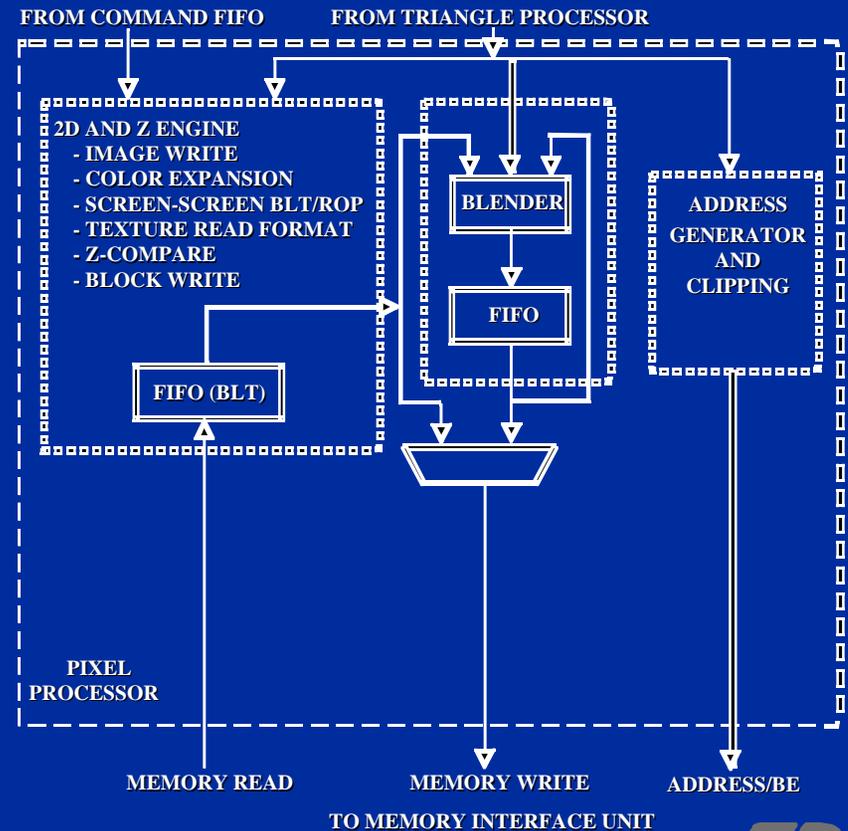
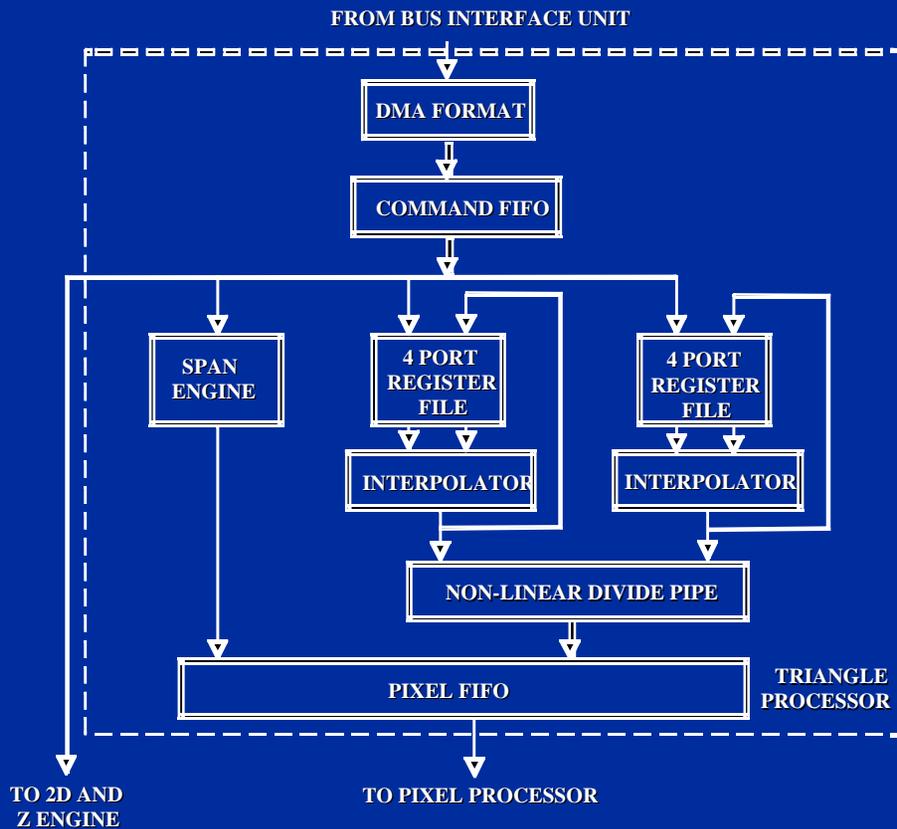


3D Rendering Features of the S3d Engine Architecture

- Triangle based rendering
- Shading features
 - Flat shading
 - Gouraud shading
- Texturing features
 - Perspective correction (w. divide)
 - Point, fast bi-linear and tri-linear filtering
 - MIP-mapping
 - Alpha blending
 - Z-buffering
 - Depth cueing
 - Compressed texture formats

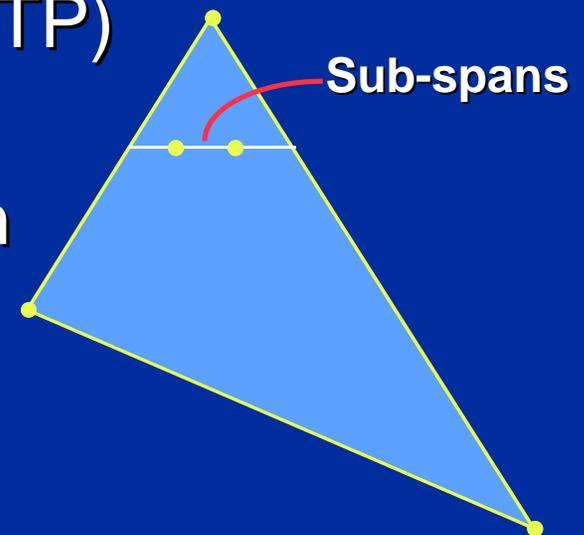


S3D 2D/3D Engine Block Diagram



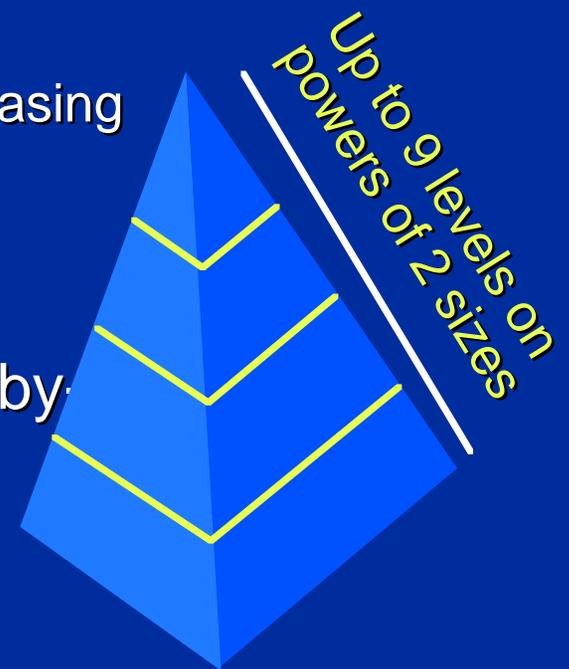
Multi-Pass Sub-Span Rendering

- Sub-spans are 16 to 64 pixels long
- Low gate count is achieved by matching the production order (in TP) with consumption order (in PP)
- Up to 4 pass rasterization on each sub-span
 - Z, if Z-buffering is enabled
 - (u, v, w), if texture mapping
 - (r, g, b), if gouraud or lit-textures
 - a, if fogging or alpha-transparency

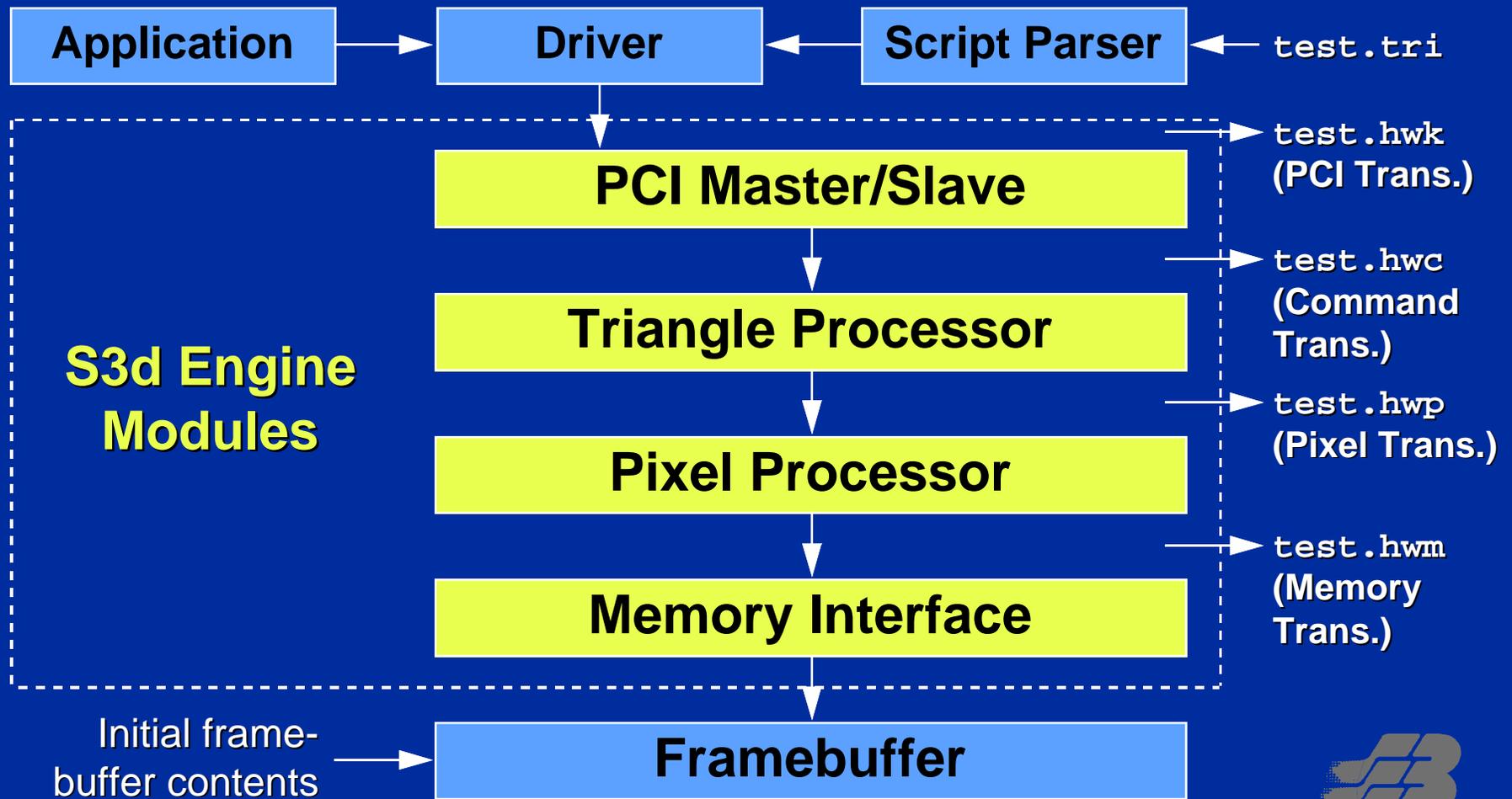


MIP-Mapping

- MIP-mapping is the basic texture map format
 - A rectangular flat map is a subset of this mode
- MIP-mapping allows:
 - improved texture fetch performance by increasing locality
 - Reduced texture download bandwidth
 - Texture anti-aliasing
- LOD calculation is computed on a pixel-by-pixel basis



C-Model Architecture



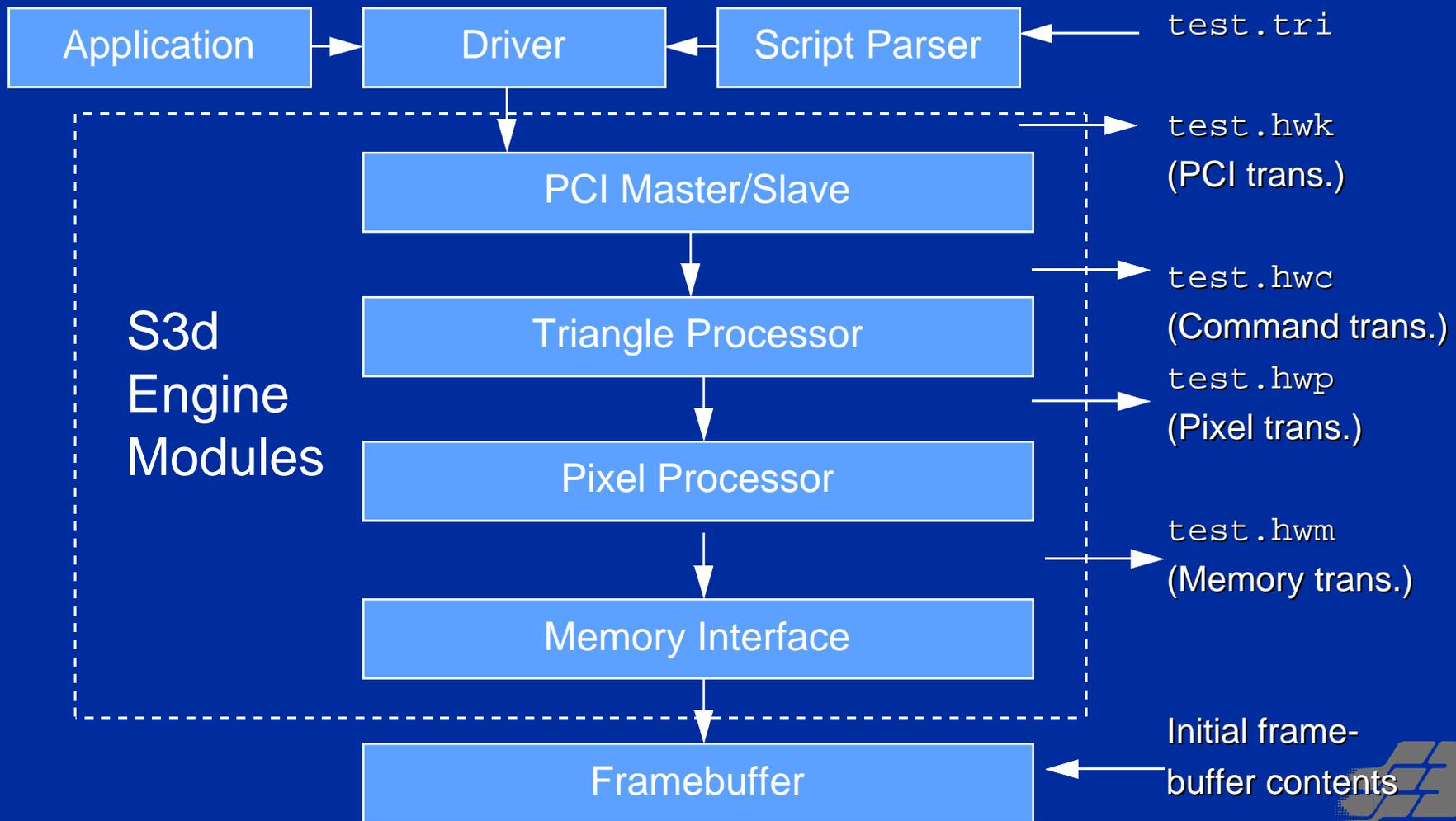
Development Project Phases

Functional Spec & Algorithm Design [Algorithmic C-Model]	Detailed Micro-arch.	Transaction accurate C-Model VHDL Entry and Verification	Full Chip Integration and Verification (pre-route)	Final Place and route Post Route Simulation	Silicon and Driver Verification
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- Algorithm and Functional Validation Accounted for Over 60% of Elapsed Time
- Ability to Lay Down Gates Is Getting Easier. Validating the Functionality is Getting Harder



C-Model Architecture



C-Model Properties

- Bit and Register Accurate
- Transaction/Order Accurate at Module Partitions
- Verified Visually Using Pictures/ Animations



C-Model Properties (cont.)

- Allows the Same Test to Be:
 - Run at module, full chip, and silicon level
 - Run on behavioral and gate level models
 - IC test vectors
- Allows Drivers and Applications to Run Using C-Model Before Silicon Is Available



Emulation

- Full Chip Emulated at 1 MHz on P5 PCI Motherboard Using Quickturn System Realizer Box
- Display Capability Using Quickturn Picasso Module
- Emulation Started When ViRGE-Core Was Stable. Allowed Net-List Conversion and Physical Setup Debugging Before Engine Logic Stable.



Emulation (cont.)

- Major Objectives Were:
 - Run VGA compliance tests
 - Debug S/W: drivers and diags
 - Run Winbench and Windows and other “Large Tests.”
 - Use to probe internal nodes during silicon debug and metal mask fixes



Summary

- ViRGE/VX provides the complete feature set for a high-end PC graphics solution
- High performance & quality 3D acceleration
- Outstanding 2D acceleration for windows
 - Enabled by an integrated 220MHz RAMDAC
- Complete VGA compatibility
- Video capture and display
- Low cost, Single-chip solution

