Video Pipeline Registers

5. VIDEO PIPELINE REGISTERS

The Video Pipeline registers in the CL-GD546X are summarized in Table 5-1. These registers are accessible only with memory-mapped I/O (that is, in the address space defined in PCI10).

Table 5-1. Video Pipeline Registers Quick Reference

Register Name	MMI/O Offset	Size (Bits)	Page
Palette State	B0h	8	5-3
External Overlay Control	B4h	8	5-5
Color Key	B8h	8	5-6
Color Key Mask	BCh	8	5-7
Graphics/Video Format	C0h	16	5-8
START_BLT_3	CAh	8	5-11
STOP_BLT_3	CBh	8	5-12
X_START_2	CCh	16	5-13
Y_START_2	CEh	16	5-14
X_END_2	D0h	16	5-15
Y_END_2	D2h	16	5-16
START_BLT_2	D4h	8	5-17
STOP_BLT_2	D5h	8	5-18
START_BLT_1	DEh	8	5-19
STOP_BLT_1	DFh	8	5-20
Cursor_X	E0h	16	5-21
Cursor_Y	E2h	16	5-22
Cursor_Preset	E4h	16	5-23
Miscellaneous_Control	E6h	16	5-24
Cursor_Address	E8h	16	5-25
Display Threshold and Tiling Control	EAh	16	5-26
Miscellaneous Test	F0h	16	5-27
Test Horizontal Counter	F2h	16	5-29
Test Vertical Counter	F4h	16	5-30

5.1 Palette State Register

Size (bits):	8
MMI/O Offset	B0h
Access Type	Read/Write

Bit	Description
7	DAC Power Down
6	External DAC
5:4	Reserved
3	Access Cursor Colors
2	Read Mode (Read only)
1:0	Palette State [1:0] (Read only)

This register contains extended controls for the palette DAC. It also contains read-only bits that return the current status of the palette logic.

Bit **Description**

7 **DAC Power Down:** When this bit is programmed to ‘1’, the palette and DACs are powered down to reduce power. The current outputs go to ‘0’. The contents of the palette are not lost, but accesses to palette cannot occur until the palette and DACs are powered up.

6 **External DAC:** This bit is reserved to enable an external RAMDAC with pixel data provided over the P[23:0] bus. This bit is not implemented on the CL-GD5464 and must be programmed to ‘0’ for compatibility.

5:4 **Reserved**

3 **Access Cursor Colors:** When this bit is programmed to ‘1’, the palette entries used for the cursor and border are accessible. The normal 256 entries are not accessible. In addition, display refresh accesses to the palette access the cursor and border colors, resulting in incorrect colors on the screen. For this reason, program this bit to ‘1’ only when the display is disabled (for example, during a set mode). The following table shows the addresses of the cursor and border colors. Addresses greater than ‘0Fh’ are reduced modulo 16.

Palette Address	Contents
00h	Cursor color 0
02h	Border color
0Fh	Cursor color 1
01h, 03h through 0Eh	Reserved for Cirrus Logic BIOS

When this bit is programmed to ‘0’, the palette entries reserved for the cursor and border are not accessible; the normal 256 entries are accessible.

2 **Read Mode (Read only):** The state of this read-only bit indicates whether the last palette access was a read (‘1’) or a write (‘0’).

5.1 Palette State Register *(cont.)*

Bit	Description
1:0	**Palette State [1:0] (Read only):** This read-only field indicates which palette field (color) was last accessed.

Palette State	Field
00	Red
01	Green
10	Blue
11	Reserved

5.2 External Overlay Control Register

Size (bits):	8
MMI/O Offset	B4h
Access Type	Read/Write

Bit	Description	Reset Value
7:6	Overlay Control [1:0]	
5:4	Color Key Mode [1:0]	
3:1	Reserved	
0	Rambus Ninth Bit Enable	0

This register contains the basic overlay controls. See Appendix C2, "Video Support".

Bit **Description**

7:6 **Overlay Control [1:0]:** This field controls overlay as shown in the following table:

Overlay Control	Overlay Selected	Switch Enabled
00b	Internal	If in window 2 or Rambus™ ninth bit enabled and '1'
01b	External	If in window 2
10b	External	If in window 2 and color key compare true
11b	Internal	If in window 2 and Rambus™ ninth bit enabled and '1'

5:4 **Color Key Mode [1:0]:** This field controls the color key comparison. This field is defined only if the overlay control field is '10b'. Otherwise program this field to '00b'. The Color Key register (offset B8h) is compared to the first byte of each pixel.

Color Key Mode	Compare is True if:
00b	Pixel = color key
01b	Pixel ≤ color key
1Xb	Pixel > color key

3:1 **Reserved**

0 **Rambus Ninth Bit Enable:** When this bit is programmed to '1', the Rambus ninth bit is included in the determination of whether to enable the internal overlay. This is effective only if the overlay control field in this register is programmed to '00b' or '11b'. This requires the use of 9-bit wide RDRAMs.

If 8-bit-wide RDRAMs are used, program this bit to '0'. When this bit is programmed to '0', Rambus ninth bit control is not enabled. Internal overlay is determined solely by whether the pixel is in window 2. This bit is cleared to '0' at reset.

5.3 Color Key Register

Size (bits):	8
MMI/O Offset	B8h
Access Type	Read/Write

Bit	Description
7:0	Color Key [7:0]

This register contains the value that is compared to the pixel for color keying. Color key comparisons are always eight bits and always compare the upper byte of the pixel.

Bit	Description
7:0	**Color Key [7:0]:** The contents of this register are compared to the upper (or only) byte of each pixel for color keying. This comparison occurs under the mask contained in the Color Key Mask register at offset BCh.

5.4 Color Key Mask Register

Size (bits):	8
MMI/O Offset	BCh
Access Type	Read/Write

Bit	Description
7:0	Color Key Mask [7:0]

This register contains the mask that is applied to the color key comparison.

Bit	Description
7:0	**Color Key Mask [7:0]:** The contents of this register are a mask that is applied to the color key comparison. If a bit in this mask is programmed to '1', the corresponding bit in the key does not participate in the comparison.

5.5 Graphics/Video Format Register

Size (bits):	16
MMI/O Offset	C0h
Access Type	Read/Write

Bit	Description
15	Reserved
14	VCLK Multiply by 2
13:12	Graphics Depth [1:0]
11:9	Graphics Format [2:0]
8	Graphics Gamma Correction Enable
7:6	Reserved
5:4	Video Depth [1:0]
3:1	Video Format [2:0]
0	Video Gamma Correction Enable

This register controls the format of pixels within the graphics and video windows. The graphics and video depths must be the same with a single exception: video depth can be 16 bpp while the graphics depth is 8 bpp. This allow mixing YUV 4:2:2 with 8-bit palettized data in a single 8-bit frame buffer. In this case, each YUV pixel is displayed for two-pixel periods.

Bit **Description**

15 **Reserved**

14 **VCLK Multiply by 2:** If this bit is programmed to '1', the clock from the synthesizer is multiplied by two in the RAMDAC, and pixels are serialized at twice the programmed frequency. This allows pixel rates to 170 MHz. Valid pixel formats (either graphics or video) are LUT8, RGB 5:6:5, AccuPak, and YUV 4:2:2. The horizontal timing remains based on the actual pixel clock divided by eight. This is also referred to as 'pixel doubling'.

If this bit is programmed to '0', the clock is not multiplied in the RAMDAC and is programmed to the actual pixel frequency. This allows the use of all pixel formats to approximately 135 MHz.

13:12 **Graphics Depth [1:0]:** This two-bit field defines the numbers of bits-per-pixel in the areas not in windows one through three. In addition, pixels that are in windows one through three can use this field according to the programming of the corresponding STOP_BLT register. The encoding is shown in the following table. The encoding is the same for the video depth field.

Graphics/Video Depth	Bits Per Pixel
00	8
01	16
10	24
11	32

5.5 Graphics/Video Format Register *(cont.)*

Bit	Description
11:9	**Graphics Format [2:0]:** This three-bit field defines the format of pixels in the areas not in windows one through three. In addition, pixels in windows one through three can use this field according to the programming of the corresponding STOP_BLT register. The encoding is shown in the following table. The encoding is exactly the same for the video format field. To obtain useful results, this field must be consistent with the corresponding depth field. Note that not all combinations are supported. Refer to Chapter 4, "Extended I/O Registers".

Graphics/Video Format	Pixel Format
000	Palettized
001	Greyscale
010	RGB (RGB 5:6:5 for graphics/video depth = ‘01b’ only)
011	RGB 5:5:5 (defined for graphics/video depth = ‘01b’ only)
100	AccuPak™
101	YUV 4:2:2
110	YUV 4:4:4
111	Reserved

5.5 Graphics/Video Format Register *(cont.)*

Bit **Description**

8 **Graphics Gamma Correction Enable:** The meaning of this bit is closely related to the value of the corresponding format field.

Gamma Correction	Format	Result
0	000: palettized	Six-bit palette entries, 256K colors
0	≠ 000: not palettized	Palette is unused
1	000: palettized and SR7[0] = 1	Eight-bit palette entries, 16M colors
1	≠ 000: not palettized	Gamma correction on three independent color fields

When this bit is programmed to '1' and the format is not '000b', the palette is taken to be three independent 256-entry lookup tables, one each for Red, Green, and Blue. For each pixel, three independent 8-bit RGB color fields are developed using color-space conversion, chroma interpolation, and bit extension as necessary. Each color field independently addresses an entry in the palette that goes to the DAC.

When this bit is programmed to '1' and the format is '000b', and SR7[0] is programmed to '1', the video is palettized. The value of each pixel accesses an entry in the palette. Each palette entry consists of three 8-bit values that are directed to the corresponding DACs. A value of 255 causes full-scale output.

When this bit is programmed to '0' and the format is '000b', the video is palettized. The value of each pixel accesses an entry in the palette. Each palette entry consists of three 6-bit values that are directed to the corresponding DACs. A value of 63 causes full-scale output.

7:6 **Reserved**

5:4 **Video Depth [1:0]:** This field defines the number of bits per pixel in video windows one through three. The encoding is exactly the same as the encoding in the graphics depth field.

3:1 **Video Format [2:0]:** This field defines the format of pixels in video windows one through three. The encoding is exactly the same as that of the graphics format field.

0 **Video Gamma Correction Enable**: This bit is used with the video format field to enable gamma correction in the video window. The meaning is exactly the same as that of the Graphics Gamma Correction Enable bit.

5.6 START_BLT_3 Register

Size (bits):	8
MMI/O Offset	CAh
Access Type	Read/Write

Bit	Description
7	ENABLE_3
6	FORMAT_3
5:0	START_BLT_3 [11:6]

This register specifies when the auto-BitBLT of window 3 is enabled. In addition, two bits control window 3.

Bit	Description
7	**ENABLE_3:** If this bit is programmed to ‘1’, window 3 is enabled. If this bit is programmed to ‘0’, window 3 is disabled. auto-BitBLT is not triggered.
6	**FORMAT_3:** If this bit is programmed to ‘1’, window 3 uses the video format, depth, and gamma fields. That is, window 3 is formatted as video. If this bit is programmed to ‘0’, window 3 uses the graphics format, depth, and gamma fields. That is, window 3 is formatted as graphics.
5:0	**START_BLT_3 [11:6]:** This six-bit field specifies when in terms of screen refresh, auto-BitBLT of window 3 is enabled. Auto-BitBLTs are described in detail in the *Laguna VisualMedia™ Accelerators Family — CL-GD546X Volume II (Software Reference Manual, Second Edition, September 1996)*, “3D-Programmer’s Guide” and Appendix C2, “Video Support”. The actual scanline number is the value in this field multiplied by 64. This field is effective only when RESIZE_C_opRDRAM[31] is ‘0’. Program this field to a value different than the value in STOP_BLT_3.

5.7 STOP_BLT_3 Register

Size (bits):	8
MMI/O Offset	CBh
Access Type	Read/Write

Bit	Description
7:6	Reserved
5:0	STOP_BLT_3 [11:6]

This register specifies when the auto-BitBLT of window 3 is disabled.

Bit	Description
7:6	**Reserved**
5:0	**STOP_BLT_3 [11:6]:** This six-bit field specifies when in terms of screen refresh, auto-BitBLT of window 3 is disabled. Auto-BitBLT is described in detail in the *Laguna VisualMedia™ Accelerators Family — CL-GD546X Volume II (Software Reference Manual, Second Edition, September 1996)*, “Programmer’s Guide” and Appendix C2, “Video Support”. The actual scanline number is the value in this field multiplied by 64. This field is effective only when RESIZE_C_opRDRAM[31] is ‘0’. This field must be programmed to a value different than the value in START_BLT_3.

5.8 X_START_2 Register

Size (bits):	16
MMI/O Offset	CCh
Access Type	Read/Write

Bit	Description
15:12	Reserved
11:0	X_START_2 [11:0]

This register specifies the left edge of window 2. Refer to Appendix C2, "Video Support".

Bit	Description
15:12	**Reserved**
11:0	**X_START_2 [11:0]:** This 12-bit field defines the left edge of window 2. This field is defined with a granularity of one pixel. The width of the window depends on the relationship between X_START_2 and X_END_2, as follows: If X_START_2 is less than X_END_2, the width of window 2 is X_END_2 minus X_START_2 pixels. If X_START_2 is greater than X_END_2, the width of the window 2 is the width of the display minus X_END_2 ≤ pixel position < X_START_2. If X_START_2 equals X_END_2, window 2 is not displayed. If X_START_2 equals 0, window 2 starts at the left edge of the screen.

5.9 Y_START_2 Register

Size (bits):	16
MMI/O Offset	CEh
Access Type	Read/Write

Bit	Description
15:12	Reserved
11:0	Y_START_2 [11:0]

This register specifies the top edge of window 2.

Bit	Description
15:12	**Reserved**
11:0	**Y_START_2 [11:0]:** This 12-bit field defines the top edge of window 2. This field is defined in terms of scanlines. The height of the window depends on the relationship between Y_START_2 and Y_END_2, as follows: If Y_START_2 is less than Y_END_2, the height of window 2 is Y_END_2 minus Y_START_2 scanlines. If Y_START_2 is greater than Y_END_2, the height of the window 2 is the height of the display minus Y_END_2 ≤ pixel position < Y_START_2. If Y_START_2 equals Y_END_2, window 2 is not displayed. If Y_START_2 equals 0, window 2 starts at the left edge of the screen.

5.10 X_END_2 Register

Size (bits):	16
MMI/O Offset	D0h
Access Type	Read/Write

Bit	Description
15:12	Reserved
11:3	X_END_2 [11:3]
2:0	Reserved

This register specifies the right edge of window 2.

Bit	Description
15:12	**Reserved**
11:3	**X_END_2 [11:3]:** This 10-bit field defines the right edge of window 2. This field is defined with a granularity of eight pixels. If X_START_2 [11:0] > X_END_2 [11:3] ⇒ width = full horizontal scanline – (X_START_2 [11:3] – X_END_2 [11:3]) If X_START_2 [11:0] ≤ X_END_2 [11:3] ⇒ width = inclusive (X_END_2 [11:3] – X_START_2 [11:3])
2:0	**Reserved**

5.11 Y_END_2 Register

Size (bits):	16
MMI/O Offset	D2h
Access Type	Read/Write

Bit	Description
15:12	Reserved
11:0	Y_END_2 [11:0]

This register specifies the bottom edge of window 2.

Bit	Description
15:12	**Reserved**
11:0	**Y_END_2 [11:0]:** This 12-bit field defines the bottom edge of window 2. This field is defined in terms of scanlines. The width of the window depends on the relationship between Y_START_2 and Y_END_2 as covered in the description of Y_START_2. The following additional notes apply to Y_END_2. The scanline at Y_END_2 is not part of window 2. If Y_END_2 is equal to or greater than the vertical display end (in scanlines), window 2 extends to the bottom edge of the display. If Y_END_2 is greater than the vertical display total (in pixels), the end of window 2 is never detected. This constitutes a programming error.

5.12 START_BLT_2 Register

Size (bits):	8
MMI/O Offset	D4h
Access Type	Read/Write

Bit	Description
7	ENABLE_2
6	FORMAT_2
5:0	START_BLT_2 [11:6]

This register specifies when the auto-BitBLT of window 2 is enabled. In addition, two bits control window 2.

Bit	Description
7	**ENABLE_2:** If this bit is programmed to '1', window 2 is enabled. If this bit is programmed to '0', window 2 is disabled. Auto-BitBLT is not triggered and V-Port data is not overlayed.
6	**FORMAT_2:** If this bit is programmed to '1', window 2 uses the video format, depth, and gamma fields. That is, window 2 is formatted as video. If this bit is programmed to '0', window 2 uses the graphics format, depth, and gamma fields. That is, window 2 is formatted as graphics.
5:0	**START_BLT_2 [11:6]:** This field specifies when, in terms of screen refresh, auto-BitBLT of window 2 is enabled. Auto-BitBLT is described in detail in *Laguna VisualMedia™ Accelerators Family — CL-GD546X Volume II (Software Reference Manual, Second Edition, September 1996)*, "3D-Programmer's Guide" and Appendix C2, "Video Support". The actual scanline number is the value in this field multiplied by 64. This field is effective only when RESIZE_B_opRDRAM[31] is '0'. Program this field to a value different than the value in STOP_BLT_2.

5.13 STOP_BLT_2 Register

Size (bits):	8
MMI/O Offset	D5h
Access Type	Read/Write

Bit	Description
7:6	Reserved
5:0	STOP_BLT_2 [11:6]

This register specifies when the auto-BitBLT of window 2 is disabled.

Bit	Description
7:6	**Reserved**
5:0	**STOP_BLT_2 [11:6]:** This six-bit field specifies when in terms of screen refresh, auto-BitBLT of window 2 is disabled. Auto-BitBLT is described in detail in *Laguna VisualMedia™ Accelerators Family — CL-GD546X Volume II (Software Reference Manual, Second Edition, September 1996)*, “3D-Programmer’s Guide” and Appendix C2, “Video Support”. The actual scanline number is the value in this field multiplied by 64. This field is effective only when RESIZE_B _opRDRAM[31] is ‘0’. Program this field to a value different than the value in START_BLT_2.

5.14 START_BLT_1 Register

Size (bits):	8
MMI/O Offset	DEh
Access Type	Read/Write

Bit	Description
7	ENABLE_1
6	FORMAT_1
5:0	START_BLT_1 [11:6]

This register specifies when the auto-BitBLT of window 1 is enabled. In addition, two bits control window 1.

Bit	Description
7	**ENABLE_1:** If this bit is programmed to '1', window 1 is enabled. If this bit is programmed to '0', window 1 is disabled. Auto-BitBLT is not triggered.
6	**FORMAT_1:** If this bit is programmed to '1', window 1 uses the video format, depth, and gamma fields. That is, window 1 is formatted as video. If this bit is programmed to '0', window 1 uses the graphics format, depth, and gamma fields. That is, window 1 is formatted as graphics.
5:0	**START_BLT_1 [11:6]:** This field specifies when, in terms of screen refresh, auto-BitBLT of window 1 is enabled. Auto-BitBLT is described in detail in *Laguna VisualMedia™ Accelerators Family — CL-GD546X Volume II (Software Reference Manual, Second Edition, September 1996)*, "3D-Programmer's Guide" and Appendix C2, "Video Support". The actual scanline number is the value in this field multiplied by 64. This field is effective only when RESIZE_A_opRDRAM[31] is '0'. Program this field to a value different than the value in STOP_BLT_1.

5.15 STOP_BLT_1 Register

Size (bits):	8
MMI/O Offset	DFh
Access Type	Read/Write

Bit	Description
7:6	Reserved
5:0	STOP_BLT_1 [11:6]

This register specifies when the auto-BitBLT of window 1 is disabled.

Bit	Description
7:6	Reserved
5:0	**STOP_BLT_1 [11:6]:** This six-bit field specifies when in terms of screen refresh, auto-BitBLT of window 1 is disabled. Auto-BitBLT is described in detail in *Laguna VisualMedia™ Accelerators Family — CL-GD546X Volume II (Software Reference Manual, Second Edition, September 1996)*, “3D-Programmer’s Guide” and Appendix C2, “Video Support”. The actual scanline number is the value in this field multiplied by 64. This field is effective only when RESIZE_A_opRDRAM[31] is ‘0’. Program this field to a value different than the value in START_BLT_1.

5.16 CURSOR_X Register

Size (bits):	16
MMI/O Offset	E0h
Access Type	Read/Write

Bit	Description
15:12	Reserved
11:0	CURSOR_X [11:0]

This register specifies the horizontal position of the hardware cursor.

Bit	Description
15:12	Reserved
11:0	**CURSOR_X [11:0]:** This 12-bit field specifies the starting point of the visible portion of the hardware cursor. This field is programmed in terms of pixels. This register is double-buffered; the new value takes effect at the end of the frame. This avoids tearing of the cursor as it is being moved.

5.17 CURSOR_Y Register

Size (bits):	16
MMI/O Offset	E2h
Access Type	Read/Write

Bit	Description
15:12	Reserved
11:0	CURSOR_Y [11:0]

This register specifies the vertical position of the hardware cursor.

Bit	Description
15:12	Reserved
11:0	**CURSOR_Y [11:0]:** This 12-bit field specifies the starting point of the visible portion of the hardware cursor. This field is programmed in terms of scanlines. This register is double-buffered; the new value takes effect at the end of the frame. This avoids tearing of the cursor as it is being moved.

5.18 Cursor_Preset Register

Size (bits):	16
MMI/O Offset	E4h
Access Type	Read/Write

Bit	Description
15	Reserved
14:8	X_PRESET [6:0]
7	Reserved
6:0	Y_PRESET [6:0]

This register specifies the pixel within the cursor image that is displayed at the Cursor_X and Cursor_Y location specified in registers E0h and E2h. This allows the appearance of the cursor moving off the left or top of the screen without the necessity of negative cursor locations.

Bit	Description
15	**Reserved**
14:8	**X_PRESET [6:0]:** This seven-bit field specifies the horizontal component of the pixel within the cursor that is displayed at the Cursor_X location. This allows the appearance of the cursor moving off the left of the screen. This field is an unsigned value.
7	**Reserved**
6:0	**Y_PRESET [6:0]:** This seven-bit field specifies the vertical component of the pixel within the cursor that is displayed at the Cursor_Y location. This allows the appearance of the cursor moving off the top of the screen. This field is an unsigned value.

5.19 Miscellaneous_Control Register

Size (bits):	16
MMI/O Offset	E6h
Access Type	Read/Write

Bit	Description	Reset Value
15:13	Reserved	
12	CSYNC Enable	
11:9	Reserved	
8	STEREO Enable	0
7:1	Reserved	
0	CURSOR Enable	0

This register contains the bits that control the hardware cursor, composite sync generation, and stereo display.

Bit 15:13 — Reserved

Bit 12 — CSYNC Enable: If this bit is programmed to '1', composite sync is driven onto the CSYNC pin. If this bit is programmed to '0', STEREO is driven onto the CSYNC pin.

Bit 11:9 — Reserved

Bit 8 — STEREO Enable: If this bit is programmed to '1', STEREO display is enabled. This bit consists of alternate display of two independent frame buffers. The following table shows the definitions of the two frames.

Frame	Beginning Address	CSYNC Pin
Left	Absolute 0	0
Right	Screen Start A (CRC, CRD)	1

This bit is '0' at reset.

Bit 7:1 — Reserved

Bit 0 — CURSOR Enable: If this bit is programmed to '1', the hardware cursor is enabled. If this bit is programmed to '0', the hardware cursor is not enabled. This bit is '0' at reset.

5.20 Cursor_Address Register

Size (bits):	16
MMI/O Offset	E8h
Access Type	Read/Write

Bit	Description
15	Reserved
14:2	Cursor Address [22:10]
1:0	Reserved

This register specifies the address in the frame buffer of the cursor image.

Bit	Description
15	**Reserved**
14:2	**Cursor Address [22:10]:** This 13-bit field gives the location of the cursor form in the frame buffer. This field is the most-significant 13 bits of a 23-bit number, allowing the cursor to be anywhere in 8 Mbytes with a granularity of 1024 bytes. The cursor image is always 64 × 64 pixels. The cursor has two planes, and these are stored interleaved as qwords (64 bits). From the cursor address, the first qword is the first scanline of plane 0, the second qword is the first scanline of plane 1, the third qword is the second scanline of plane 0, and so on to the sixty-third scanline of plane 1. This is a total of 128 qwords or 1024 bytes. Cursor images can be stored contiguously with no wasted memory. The *Laguna VisualMedia™ Accelerators Family — CL-GD546X Volume II (Software Reference Manual, Second Edition, September 1996)*, “3D-Programmer’s Guide” discusses the programming of the cursor in detail. This register is not double buffered. Normally, this register is modified at the end of a frame. This address does not undergo tiling translation before being applied to the RIF. The driver must compensate for tiling when calculating the address. Bank interleaving is handled by the hardware.
1:0	**Reserved**

5.21 Display Threshold and Tiling Control Register

Size (bits):	16
MMI/O Offset	EAh
Access Type	Read/Write

Bit	Description	Reset Value
15:14	Interleave Mode [1:0]	0
13:8	Tiles Per Line [5:0]	1
7	Tiling Enable	0
6	Wide Tile	0
5:4	FIFO Threshold [5:4]	0
3	FIFO Threshold [3:0]	1

This register controls tiling and the FIFO threshold. It is programmed by the Cirrus Logic BIOS during a video mode set and must never be programmed by any application program. This register description is included for completeness only. See the *Laguna VisualMedia™ Accelerators Family — CL-GD546X Volume II (Software Reference Manual, Second Edition, September 1996)*, "3D-Programmer's Guide" for additional information.

Bit **Description**

15:14 **Interleave Mode [1:0]:** This two-bit field controls the Interleave mode according to the following table:

Interleave Mode [1:0]	Description
00	1-way interleave
01	2-way interleave
10	4-way interleave
11	Reserved

13:8 **Tiles Per Line [5:0]:** This six-bit field specifies the number of tiles per scanline.

7 **Tiling Enable:** If this bit is programmed to '1', tiling is enabled. If this bit is programmed to '0', tiling is disabled.

6 **Wide Tile:** If this bit is programmed to '1', the CRTC fetches wide tiles. If this bit is programmed to '0', the CRTC does not fetch wide tiles.

5:0 **FIFO Threshold [5:0]:** This six-bit field specifies the level (number of 64-bit words of valid data remaining) in the display FIFO where the display module should request a Rambus cycle to refill the FIFO. For each video mode/refresh rate combination and Rambus clock, there is a value that optimizes the use of the FIFO and Rambus.

5.22 Miscellaneous Test Register

Size (bits):	16
MMI/O Offset	F0h
Access Type	Read/Write

Bit	Description	Reset Value
15	Select RCLK	0
14	TR6 [1]	0
13	TR6 [0]	0
12	PC1 Bypass	0
11	Error Diffusion Bypass	0
10	DAC Linearity Test	
9	Test YUV Bypass	0
8	Test Bypass	0
7	Source of PCI Bypass	0
6	Disable 3D-Texture Write	0
5	Enable 3D-Texture Write	
4	Reserved	
3	Test Extended I/O Block	0
2	Test VGA Block	0
1	Test CRTC Block	0
0	Test RAM	0

This register contains the bits that invoke various test modes, and should never be written by any application program. This description is included for completeness only.

Bit	Description
15	**Select RCLK:** If this bit is programmed to ‘1’, the internal pixel clock is sourced directly from the RCLK pin. If this bit is ‘0’, the CL-GD546X operates normally.
14	**TR6 [1]:** If this bit is programmed to ‘1’, the VCLK VCO output for the numerator counter is replaced with OSCi. If this bit is ‘0’, the CL-GD546X operates normally.
13	**TR6 [0]:** If this bit is programmed to ‘1’, the numerator counter output is selected. If this bit is ‘0’, the CL-GD546X operates normally.
12	**PC1 Bypass:** If this bit is programmed to ‘1’, PC1 is from VCLK0. If this bit is ‘0’, the CL-GD546X operates normally.
11	**Error Diffusion Bypass:** If this bit is programmed to ‘1’, error diffusion for AccuPak is disabled. If this bit is ‘0’, the CL-GD546X operates normally.
10	**DAC Linearity Test:** The data on the V-Port pins directly drives the RAMDAC.
9	**Test YUV Bypass:** If this bit is programmed to ‘1’, the YUV interpolation block is bypassed. If this bit is ‘0’, the CL-GD546X operates normally.
8	**Test Bypass:** If this bit is programmed to ‘1’, the logic does not wait for the end of a frame to update double-buffered registers. If this bit is ‘0’, the CL-GD546X operates normally.

5.22 Miscellaneous Test Register *(cont.)*

Bit	Description
7	**Source of PC1 Bypass:** If this bit is '1', the source for PC1 bypass is VCK0. If this bit is '0', the source for PC1 bypass is DCLK.
6	**Disable 3D-Texture Write:** If this bit is '1', the 3D-texture write is disabled. If this bit is '0', the 3D-texture write is enabled.
5	**Enable 3D-Texture Write:** If this bit is '1', the 3D-texture write is enabled. If this bit is '0', the 3D-texture write is disabled.
4	**Reserved**
3	**Test Extended I/O Block:** If this bit is '1', the extended I/O block is tested. If this bit is '0', the CL-GD546X operates normally.
2	**Test VGA Block:** If this bit is '1', the VGA core block is tested. If this bit is '0', the CL-GD546X operates normally.
1	**Test CRTC Block:** If this bit is '1', the CRTC block is tested. If this bit is '0', the CL-GD546X operates normally.
0	**Test RAM:** If this bit is '1', the palette RAM is tested. If this bit is '0', the CL-GD546X operates normally.

5.23 Test Horizontal Counter Register

Size (bits):	16
MMI/O Offset	F2h
Access Type	Read/Write

Bit	Description
15	Test HT Load
14:9	Reserved
8:0	HT [8:0]

This register tests the CRTC horizontal counter. This register must never be written by any application program. This description is included for completeness only.

Bit	Description
15	**Test HT Load:** If this bit is programmed to ‘1’, the horizontal counter is loaded with the HT [8:0] field.
14:9	**Reserved**
8:0	**HT [8:0]:** This value is loaded into the horizontal counter for testing.

5.24 Test Vertical Counter Register

Size (bits):	16
MMI/O Offset	F4h
Access Type	Read/Write

Bit	Description
15	Test VT Load
14:11	Reserved
10:0	VT [10:0]

This register tests the CRTC vertical counter. This register must never be written by any application program. This description is included for completeness only.

Bit	Description
15	**Test VT Load:** If this bit is programmed to '1', the vertical counter is loaded with the VT [10:0] field.
14:11	**Reserved**
10:0	**VT [10:0]:** This value is loaded into the vertical counter for testing.

