Appendix B5

Pin Scan

PIN SCAN

1. INTRODUCTION

Pin-Scan testing is a technique for verifying that an IC has been properly soldered to the circuit board. Any IC signal pin not connected to the board, or shorted to any neighboring pin or trace, is detectable using this technique. The advantage of Pin-Scan testing is that the test patterns to verify full board connectivity are much simpler than would otherwise be possible. The pins are connected sequentially around the IC in a single chain, so that the value on each output pin depends on the values applied to other pins, rather than the internal state of the VGA processor. In addition, the Pin-Scan logic is strictly combinatorial, so no clock pulses are required.

The first pin in the chain is an input pin; the last pin is an output pin. Each input signal is XOR'ed with the scan data from its lower-numbered neighboring input or output pin. The result of this XOR is passed to its higher-numbered neighbor. Each output pin is driven with the value passed from its lower-numbered neighbor; that value is inverted and passed to its higher-numbered neighbor.

NOTE: There is no necessary relationship between the direction of a pin in Pin-Scan mode and the normal direction of a pin.

2. TEST METHOD

In Pin-Scan mode the test program begins by driving all the input pins to '1', and verifying that the output pins match the values shown in Table B5-1. On subsequent cycles, the program drives each input pin, individually to '0' and verifies that all the 'down-stream' outputs match the values shown. In each case, the output is inverted from the value for the all-zeroes case.

If the value applied to an input pin is changed and the 'down-stream' output pins do not change, that input is shorted or not soldered. If any single output is wrong, it is either shorted or not soldered.

2.1 Entering Pin-Scan Mode: CL-GD5462

The CL-GD5464 is placed into Pin-Scan mode by making RST# low for at least 20 ns while pin 125 is low, then making RST# high.

2.2 Exiting Pin-Scan Mode: CL-GD5462

The CL-GD5464 is removed from Pin-Scan mode by making RST# low with pin 125 high.

2.3 Entering Pin-Scan Mode: CL-GD5464

The CL-GD5464 is placed into Pin-Scan mode by making RST# low for at least 20 ns while pin 107 is low, then making RST# high.

2.4 Exiting Pin-Scan Mode: CL-GD5464

The CL-GD5464 is removed from Pin-Scan mode by making RST# low with pin 107 high.

3. PIN SCAN ORDER

In Table B5-1, the pin names are for the PCI bus. The table indicates the pins that are outputs, and indicates the level to be expected for the two cases of ‘all inputs = 1’ and ‘one upstream input = 0’.

Table B5-1. Pin Scan Order

Pin Name	Pin Number	In/Out	All Inputs = 1	1 Input = 0
GNT#	206	In		
CLK	207	In		
RST#	1	In		
REQ#	2	In		
AD31	3	In		
AD30	4	In		
AD29	5	In		
AD28	6	In		
AD27	7	In		
AD26	8	In		
AD25	9	In		
AD24	10	In		
CBE3#	11	In		
IDSEL	13	In		
AD23	15	In		
AD22	16	In		
AD21	17	In		
AD20	18	In		
AD19	19	In		
AD18	20	In		
AD17	21	In		
AD16	22	In		
CBE2#	23	In		
FRAME#	24	In		
IRDY#	26	In		
TRDY#	27	In		
DEVSEL#	28	In		

Table B5-1. Pin Scan Order *(cont.)*

Pin Name	Pin Number	In/Out	All Inputs = 1	1 Input = 0
STOP#	29	In		
PAR	30	In		
CBE1#	31	In		
AD15	32	In		
AD14	34	In		
AD13	35	In		
AD12	36	In		
AD11	37	In		
AD10	39	In		
AD9	40	In		
AD8	41	In		
CBE0#	42	In		
AD7	43	In		
AD6	44	In		
AD5	45	In		
AD4	47	In		
AD3	49	In		
AD2	50	In		
AD1	51	In		
AD0	52	In		
RCLK	54	In		
ROMCS#	62	Out	0	1
PRDY	87	In		
PCS#	88	In		
RD0	89	In		
RD1	90	In		
RD2	91	In		
RD3	92	In		
RD4	93	In		
RD5	95	In		
RD6	96	In		

Table B5-1. Pin Scan Order *(cont.)*

Pin Name	Pin Number	In/Out	All Inputs = 1	1 Input = 0
RD7	97	In		
RA0	99	In		
RA1	100	In		
RA2	101	In		
RA3	102	In		
RA4	103	In		
RA5	104	In		
RA6	106	In		
RA7	107	In		
RA8	108	In		
RA9	109	In		
RA10	110	In		
RA11	111	In		
RA12	112	In		
RA13	113	In		
RA14	115	In		
RA15	117	In		
RESERVED	118	In		
RESERVED	119	In		
RESERVED	120	In		
RESERVED	121	In		
P23	122	In		
P22	123	In		
P21	124	In		
P20	125	In		
P19	127	In		
P18	128	In		
P17	129	In		
P16	130	In		
P15	132	In		
P14	133	In		
P13	134	In		

Table B5-1. Pin Scan Order *(cont.)*

Pin Name	Pin Number	In/Out	All Inputs = 1	1 Input = 0
P12	135	In		
P11	137	In		
P10	138	In		
P9	139	In		
P8	140	In		
VCLK	141	Out	0	0
EDCLK#	142	In		
ESYNC#	143	In		
EVIDEO#	144	In		
BLANK#	145	In		
DCLK	147	In		
P7	148	In		
P6	149	In		
P5	150	In		
P4	152	In		
P3	153	In		
P2	154	In		
P1	155	In		
P0	156	In		
SDA	158	In		
SCL	159	In		
SREQ#	160	In		
HSYNC	161	In		
VSYNC	162	In		
SOUT	179	Out	1	1
CSYNC#	204	Out	0	0
INTA#	205	Out	1	1

Pins not listed in Table B5-1 are not accessible in the pin scan because they are either analog or Rambus Channel pins. Also, the power pins are not accessible to pin scan.

