Enhanced V-Port™ *Registers*

6.   ENHANCED V-PORT™ REGISTERS

The Enhanced V-Port registers in the CL-GD546X are summarized in Table 6-1. These registers are accessible only with memory-mapped I/O (that is, in the address space defined in PCI10).

Table 6-1.   Enhanced V-Port™ Registers Quick Reference

Register Name	MMI/O Offset	Size (Bits)	Page
Buffer 0 X Address	100h	16	6-3
Buffer 1 X Address	102h	16	6-4
Buffer 0 Y Address	104h	16	6-5
Buffer 1 Y Address	106h	16	6-6
Capture X Start	108h	16	6-7
Capture X Stop	10Ah	16	6-8
Capture Y Start	10Ch	16	6-9
Capture Y Stop	10Eh	16	6-10
V-Port Mode	110h	32	6-14
Video Y Start	114h	16	6-19
Test Output	118h	16	6-20

6.1   Buffer 0 X Address Register

Size (bits):	16
MMI/O Offset	100h
Access Type	Read/Write

Bit	Description
15:13	Reserved
12:8	X Start (Odd) [12:8]
7:0	Reserved

This register specifies the starting X address of the off-screen buffer used for V-Port reads or writes.

Bit	Description
15:13	**Reserved**
12:8	**X Start (Odd) [12:8]:** This five-bit field specifies the X address, in bytes, of the off-screen buffer used for V-Port reads or writes. If double buffering is enabled (see V-Port Control at 10Ch[3] on page 6-14), this address is used for every other frame, beginning with the first. The granularity is 256 bytes.
7:0	**Reserved**

6.2   Buffer 1 X Address Register

Size (bits):	16
MMI/O Offset	102h
Access Type	Read/Write

Bit	Description
15:13	Reserved
12:8	X Start (Even) [12:8]
7:0	Reserved

This register specifies the starting X address of the off-screen buffer used for V-Port reads or writes.

Bit	Description
15:13	**Reserved**
12:8	**X Start (Even) [12:8]:** This five-bit field specifies the X address, in bytes, of the off-screen buffer used for V-Port reads or writes. If double buffering is disabled (see V-Port Control at 10Ch[3] on page 6-14), this address is not used. If double buffering is enabled, this address is used for every other frame, beginning with the second. The granularity is 256 bytes.
7:0	**Reserved**

6.3   Buffer 0 Y Address Register

Size (bits):   16
MMI/O Offset   104h
Access Type   Read/Write

Bit	Description
15:14	Reserved
13:0	Y Start (Odd) [13:0]

This register specifies the starting Y address of the off-screen buffer used for V-Port reads or writes.

Bit	Description
15:14	**Reserved**
13:0	**Y Start (Odd) [13:0]:** This 14-bit field specifies the Y address, in scanlines, of the off-screen buffer used for V-Port reads or writes. After each scanline, the display pitch is added to the starting address of that scanline to calculate the beginning address in the next scanline. At the end of each frame, the X,Y address is reloaded from the start registers.
	If double buffering is enabled (see V-Port Control at 10Ch[3] on page 6-14), this address is used for every other frame, beginning with the first.
	If double buffering is disabled (see V-Port Control at 10Ch[3] on page 6-14), this address is not used. If double buffering is enabled, this address is used for every other frame, beginning with the second.

6.4   Buffer 1 Y Address Register

Size (bits):	16
MMI/O Offset	106h
Access Type	Read/Write

Bit	Description
15:14	Reserved
13:0	Y Start (Even) [13:0]

This register specifies the starting Y address of the off-screen buffer used for V-Port reads or writes.

Bit	Description
15:14	**Reserved**
13:0	**Y Start (Even) [13:0]:** This 14-bit field specifies the Y address, in scanlines, of the off-screen buffer used for V-Port reads or writes. After each scanline, the display pitch is added to the starting address of that scanline to calculate the beginning address in the next scanline. At the end of each frame, the X,Y address is reloaded from the start registers.

6.5   Capture X Start Register

Size (bits):	16
MMI/O Offset	108h
Access Type	Read/Write

Bit	**Description**
15:10	Reserved
9:0	Capture X Start [9:0]

This register defines the left edge of a capture window for incoming video, measured in PCLK cycles. Only video inside this window is captured by the V-Port. This register is required for decoders that do not have an output to indicate the active video interval to prevent capturing data during blanking intervals, and to select closed caption or teletext data, if that is all that should be captured.

Bit	**Description**
15:10	**Reserved**
9:0	**Capture X Start:** This 10-bit field defines the left edge of a capture window for incoming video. This field must be set to start capture at an RGB or UYVY boundary; the minimum Capture X Start granularity for different DCLK modes and bus widths is as shown in the following table:

DCLK Mode	Bus Width	Video Format	Granularity (Clock Cycle)	Notes
11	1	X	X	Double-clocked 16-bit bus not supported
11	0	YUV 4:4:2	2	Double-clocked 8-bit mode
11	0	RGB 5:6:5	1	Double-clocked 8-bit mode
10	1	YUV 4:4:2	2	Rising-edge clocked 16-bit mode
10	1	RGB 5:6:5	1	Rising-edge clocked 16-bit mode
10	0	YUV 4:4:2	4	Rising-edge clocked 8-bit mode
10	0	RGB 5:6:5	2	Rising-edge clocked 8-bit mode
01	1	YUV 4:4:2	2	Falling-edge clocked 16-bit mode
01	1	RGB 5:6:5	1	Falling-edge clocked 16-bit mode
01	0	YUV 4:4:2	4	Falling-edge clocked 8-bit mode
01	0	RGB 5:6:5	2	Falling-edge clocked 8-bit mode
00	X	X	X	Feature Connector mode; no capture

For decoders without a 'video active' signal, Capture X Start can need lower granularity, than shown in the table above, to start capturing data on an RGB or UYVY boundary; the difference of Capture X Start minus Capture X Stop, should have the granularity shown in the table above.

6.6   Capture X Stop Register

Size (bits):	16
MMI/O Offset	10Ah
Access Type	Read/Write

Bit	Description
15:10	Reserved
9:0	Capture X Stop [9:0]

This register defines the right edge of a capture window for incoming video. Only video inside this window is captured by the V-Port and written to off-screen memory. This register is also required for decoders that do not have an output to indicate the active-video interval to prevent capturing data during blanking intervals, and to select closed caption or teletext data, if that is all that should be captured. Capture granularity is limited to two-pixel boundaries.

Bit	Description
15:10	**Reserved**
9:0	**Capture X Stop:** This 10-bit field defines the right edge of a capture window for incoming video. This field must be set to stop capture at an RGB or UYVY boundary; the minimum Capture X Stop granularity for different DCLK modes and bus widths is as shown in the following table:

DCLK Mode	Bus Width	Video Format	Granularity (clock cycle)	Notes
11	1	X	X	Double-clocked 16-bit bus not supported
11	0	YUV 4:4:2	2	Double-clocked 8-bit mode
11	0	RGB 5:6:5	1	Double-clocked 8-bit mode
10	1	YUV 4:4:2	2	Rising-edge clocked 16-bit mode
10	1	RGB 5:6:5	1	Rising-edge clocked 16-bit mode
10	0	YUV 4:4:2	4	Rising-edge clocked 8-bit mode
10	0	RGB 5:6:5	2	Rising-edge clocked 8-bit mode
01	1	YUV 4:4:2	2	Falling-edge clocked 16-bit mode
01	1	RGB 5:6:5	1	Falling-edge clocked 16-bit mode
01	0	YUV 4:4:2	4	Falling-edge clocked 8-bit mode
01	0	RGB 5:6:5	2	Falling-edge clocked 8-bit mode
00	X	X	X	Feature Connector mode; no capture

For decoders without a 'video active' signal, Capture X Stop can need lower granularity, than shown in the table above, to stop capturing data on an RGB or UYVY boundary; the difference of Capture X Start minus Capture X Stop, should have the granularity shown in the table above.

6.7 Capture Y Start Register

Size (bits):   16

MMI/O Offset   10Ch

Access Type   Read/Write

Bit	Description
15:9	Reserved
8:0	Capture Y Start [8:0]

This register defines the top edge of a capture window for incoming video. Only video inside this window is captured by the V-Port and written to off-screen memory. This register is also required for decoders that do not have an output to indicate the active-video interval to prevent capturing data during blanking intervals, and to select closed caption or teletext data, if that is all that should be captured.

Bit	Description
15:9	**Reserved**
8:0	**Capture Y Start [8:0]:** These nine bits define the top edge of a capture window for incoming video.

6.8   Capture Y Stop Register

Size (bits):	16
MMI/O Offset	10Eh
Access Type	Read/Write

Bit	Description
15:9	Reserved
8:0	Capture Y Stop [8:0]

This register defines the bottom edge of a capture window for incoming video. Only video inside this window is captured by the V-Port and written to off-screen memory. This register is also required for decoders that do not have an output to indicate the active-video interval to prevent capturing data during blanking intervals, and to select closed caption or teletext data, if that is all that should be captured.

Bit	Description
15:9	**Reserved**
8:0	**Capture Y Stop [8:0]:** These nine bits define the right edge of a capture window for incoming video.

6.9 V-Port™ Control Register (CL-GD5462 Only)

Size (bits):	16
MMI/O Offset	10Ch
Access Type	Read/Write

Bit	Description	Reset Value
15:12	Test Output [3:0]	0
11	Odd Field Detect (Read only)	1
10	Buffer (Read only)	1
9	External VSYNC Interrupt	0
8	Skip Frame	0
7	DCLK Mode [1]	1
6	DCLK Mode [0]	0
5	Readback External Interrupt (Read only)	0
4	Bus Width	1
3	Double Buffer Enable	0
2:0	V-Port Mode [2:0]	0

Bits in this register control the enhanced V-Port. The enhanced V-Port is covered in detail in Appendix C2, "Video Support" . This register description summarizes the controls.

Bit	Description
15:12	**Test Output [3:0]:** This field allows output of 24-bit digital RGB or other test data. This is intended for factory testing only. This field should always be programmed to '0000b' by any application program. The following table is for reference only:

Pin Names	RA[15:8]	RA[7:0]	RD[7:0]	P[23:16]	NOTES
0000	RA[15:8] ROM address	RA[7:0] ROM address	RD[7:0] ROM data	P[23:16]	Normal mode
1000	R[7:0] or Test[23:16]	RA[7:0]	RD[7:0]	P[23:16]	–
1100	R[7:0] or Test[23:16]	G[7:0] or Test[15:8]	RD[7:0]	P[23:16]	–
1110	R[7:0] or Test[23:16]	G[7:0] or Test[15:8]	B[7:0] or Test[7:0]	P[23:16]	–
1111	R[7:0] or Test[23:16]	G[7:0] or Test[15:8]	B[7:0] or Test[7:0]	Test[31:24]	8- and 16-bit V-Port™ mode only

Bit	Description
11	**Odd Field Detect:** This read-only bit reflects which interlaced field was last detected. If this bit is set to '1', it is odd field (VSYNC in middle of scanline); if this bit is set to '0' it is even field (VSYNC at beginning of scanline). If this bit is read in response to an external VSYNC interrupt, this bit reflects the state of the previous field now in off-screen memory, not the new field currently being captured. If odd field detect is '0', it is always for decoders that output non-interlaced video (for example, MPEG decoders).

6.9   V-Port™ Control Register (CL-GD5462 Only) *(cont.)*

Bit	Description
10	**Buffer:** When double buffering is enabled, this bit indicates in which buffer the previously captured video field is stored. If this bit is set to '0', it is Buffer 0; if this bit is set to '1', it is Buffer 1. Buffer is equal to '0' is used when double buffering is not enabled. This bit is a read-only bit.
9	**External VSYNC Interrupt:** When this bit is programmed to '1', this bit enables a CL-GD546X interrupt to be generated on the trailing edge of an external VSYNC (the CL-GD546X EDCLK# pin), rather than its own VSYNC; VSYNC interrupts must still be enabled by the CR11 register, bit 5.
8	**Skip Frame:** This field specifies how frequently video frames are requested by the V-Port. VSYNC refers to the external VSYNC (the CL-GD546X EDCLK# pin). This allows skipping video frames (fields for interlaced video) to reduce the Rambus bandwidth used for video.

Skip Frame	Video Frame Rate
0	VSYNC rate
1	VSYNC / 2 rate

Bit	Description
7:6	**DCLK Mode [1:0]:** This field controls which DCLK clock edges capture data.

DCLK Mode	Data Clocked On
00	Every second falling clock edge
01	Every falling clock edge
10	Every rising clock edge
11	Both edges

Bit	Description
5	**Readback External Interrupt:** This bit is a read-only bit.
4	**Bus Width:** This field specifies the V-Port bus width.

Bus Width	Width (bits)	P Bus Bits Used
1	8	P[7:0]
0	16	P[15:0]

6.9   V-Port™ Control Register (CL-GD5462 Only) *(cont.)*

Bit	Description
3	**Double Buffer Enable:** If this bit is programmed to '1', capture data is double buffered by using both sets of addresses. If this bit is programmed to '0', only the addresses in the X,Y_START_ODD registers are used.
2:0	**V-Port Mode [2:0]:** This field controls the basic V-Port mode of operation. This field is modified by the other bits in this register.

V-Port™ Mode	Basic Mode
000	Feature Connector
001	Reserved
010	Video Capture
011	Reserved
100	Reserved
110	Reserved
111	Reserved

6.10   V-Port™ Mode Register (CL-GD5464 Only)

Size (bits):	32
MMI/O Offset	110h
Access Type	Read/Write

Bit	Description	Reset
31:30	Reserved	X
29:28	Skip Request Threshold [1:0]	0
27:25	Reserved	X
24	Teletext Capture Enable	0
23:21	Reserved	X
20	Odd Scanlines on Top	0
19	Enable External IRQ	0
18	Clear External IRQ	0
17	External IRQ (Read only)	X
16	External VSYNC (Read only)	X
15	VACT Enable	0
14	VACT Active High	0
13	X Decimate Enable	0
12	Reverse Field Polarity	0
11	Odd Field (Read only)	X
10	Buffer (Read only)	X
9	Reserved	X
8	Double Buffer Enable	0
7:6	DCLK Mode [1:0]	0
5	PRESENT# (Read only) / ENABLE (Write only)	see bit description
4	16-bit Bus Width	0
3:2	Capture Mode [1:0]	1
1	External HSYNC Polarity	1
0	External VSYNC Polarity	1

This register controls operation of the V-Port.

Bit	Description
31:30	**Reserved**
29:28	**Skip Request Threshold [1:0]:** These bits set a V-Port FIFO level above which a pending memory request is aborted, and the memory pointer advanced to skip over those dropped pixels. In the case where memory latency is too large and a FIFO overrun is imminent (as determined by the setting of this bit), the V-Port drops on request (64 bytes) and advances its memory pointer 64 bytes. This allows it to catch up with incoming data and keep the memory pointer correct for the rest of the scanline.
27:25	**Reserved**

6.10 V-Port™ Mode Register (CL-GD5464 Only) *(cont.)*

Bit	Description
24	**Teletext Capture Enable:** If this bit is '1', the teletext capture is enabled. On scanlines between Y Capture Start and Y Video Start minus 1 teletext capture is enabled (only Y data is captured and X decimation is disabled); on scanlines from Y Video Start to Y Capture Stop data is captured normally (YUV data is captured and X decimation is controlled by the X Decimation Enable, bit 13). If this bit is '0', the teletext capture is disabled. Teletext capture is not supported for AccuPak data.
23:21	**Reserved**
20	**Odd Scanlines on Top:** This bit is tentatively defined to determine which field is stored on top for interlaced capture. If this bit is '1', scanlines from odd fields are stored above the same scanline from even fields. If this bit is '0' (default), scanlines from even fields are stored above the same scanline from odd fields.
19	**Enable External IRQ:** If this bit is '1', the IRQ pin is activated when the external decoder VSYNC is active, and is deactivated when a '1' is written to External IRQ Clear (bit 18); in this mode, internal VSYNC interrupts do not activate the IRQ pin. If this bit is '0', the IRQ is activated when the CL-GD546X internal VSYNC is active (if enabled by CR11[5] is '0'), and is deactivated when CR11[4] is '0'; in this mode, external VSYNC interrupts do not activate the IRQ pin, but can still be polled on External IRQ (bit 17).
18	**Clear External IRQ:** A write of '1' to this bit forces the IRQ pin inactive; a write of '0' to this bit allows the IRQ pin to be reactivated (if external interrupts are enabled by Enable External IRQ, bit 19).
17	**External IRQ (Read only):** This read-only bit returns the state of the external IRQ register. This bit is '1' when the external decoder VSYNC is active, and is '0' when a '1' is written to Clear External IRQ (bit 18).
16	**External VSYNC (Read only):** This read-only bit returns the state of the external decoder VSYNC pin. Unlike External IRQ (bit 17) it is not latched. This bit is provided for DirectDraw support.
15	**VACT Enable:** If this bit is '1', the video decoder provides a 'video active' signal to qualify when there is valid video data on P[15:0]; video is captured on pixel clocks where VACT is '1'. If this bit is '0', it is assumed the decoder does not provide a 'video active' signal; video capture is controlled by the X,Y Capture Start and X,Y Capture End registers only. All scanlines (starting from the falling edge of VSYNC) are counted for comparison to the Y Capture Start, Y Capture Stop, and Y Video Start registers, and pixels are counted from the falling edge of HSYNC.
14	**VACT Active High:** If this bit is '1', the external VACT signal (if enabled by bit 15) is high to indicate valid video data on P[15:0] or P[7:0].

6.10 V-Port™ Mode Register (CL-GD5464 Only) *(cont.)*

Bit	Description
13	**X Decimate Enable:** If this bit is '1', video data is decimated (except for scanlines less than Y Video Start when the Teletext Capture Enable (bit 24) is '1').

The following table shows how YUV 4:2:2 and RGB 5:6:5 data is decimated; a '✔' shows which input bytes are captured, and the row below shows the resulting decimated data packed in UYVY or RGB groups. The X decimation is not supported for AccuPak mode.

YUV 4:2:2

Byte	0	1	2	3	4	5	6	7	8	9	10	11
Input	U0✔	Y0✔	V0✔	Y1	U2	Y2✔	V2	Y3	U4✔	Y4✔	V4✔	Y5
Captured	U0	Y0	V0	Y2	U4	Y4	V4	Y6	U8	Y8	V8	Y10

RGB 5:6:5

Byte	0	1	2	3	4	5	6	7	8	9	10	11
Input	pixel 0✔		pixel 1		pixel 2✔		pixel 3		pixel 4✔		pixel 5	
Captured	pixel 0		pixel 2		pixel 4		pixel 6		pixel 8		pixel 10	

Bit	Description
12	**Reverse Field Polarity:** If this bit is '1', the sense of the Even and Odd fields is reversed. If this bit is '0', the sense of the Even and Odd fields is normal; even fields are defined as VSYNC falling during HSYNC active, and odd fields are defined as VSYNC falling between two HSYNC pulses.
11	**Odd Field (Read only):** This read-only bit reflects which interlaced field was last detected; '1' is Odd field (VSYNC falling edge between two HSYNC pulses), and '0' is Even field (VSYNC falling edge during HSYNC active).

If this bit is read in response to an external VSYNC interrupt, this bit reflects the state of the previous field already in off-screen memory, not the new field currently being captured. This is necessary because external VSYNC interrupts are generated on the rising edge of VSYNC while the Odd Field is detected on the falling edge of VSYNC; because the interrupt latency can be less than or greater than the VSYNC pulse width, otherwise it is difficult to determine if an Odd Field for the previous field or the current field is being read.

Odd Field is always '1' for decoders that output non-interlaced video (for example, MPEG decoders).

Bit	Description
10	**Buffer (Read only):** When double buffering is enabled (bit 8), this read-only bit indicates buffer in which the previously captured video field is stored; '0' is buffer 0, '1' is buffer 1. Buffer is always '0' when double buffering is not enabled. This is independent of odd field detection (bit 11).
9	**Reserved**

6.10   V-Port™ Mode Register (CL-GD5464 Only) *(cont.)*

Bit	Description
8	**Double Buffer Enable:** If this bit is '1', double buffering of video data in off-screen memory is enabled, at the locations specified by the Buffer 0 X Address, Buffer 0 Y Address, Buffer 1 X Address, and Buffer 1 Y Address registers. The first video field (frame) is stored in buffer 0, and the buffers alternate until the next hardware or software reset. Buffers 0 and 1 do not correspond to even or odd video fields, field information is in Odd Field (bit 11).
	Double buffering can be used with interlaced or non-interlaced video.
	If the video is interlaced and both field capture (Capture mode is 11) is selected, consecutive fields are stored alternately in buffer 0 and buffer 1; odd fields can be stored in buffer 0 or buffer 1, check both Odd Field (bit 11) and Buffer (bit 10) bits to see which field is where.
	If the video is interlaced and even field (Capture mode is 10) or odd field (Capture mode is 01) capture is selected, the even (odd) fields of consecutive frames are stored alternately in buffer 0 and buffer 1.
	If the video is interlaced and interlaced capture (Capture mode is 00) is selected or if the video is non-interlaced, consecutive frames are stored alternately in buffer 0 and buffer 1.
	If this bit is '0,' double buffering is disabled; data is stored in buffer 0 only.
7:6	**DCLK Mode [1:0]:** These two bits control on which clock edges V-Port data is sampled, and also select between the V-Port and Feature Connector mode for the V-Port pins.

DCLK Mode [1]	DCLK Mode [0]	Sample Video Data
1	1	On both DCLK edges (start with rising; sample BLANK#, EDCLK#, and EVIDEO# on rising edge only)
1	0	On rising DCLK edges
0	1	On falling DCLK edges
0	0	Never (Feature Connector mode)

Bit	Description
5	**PRESENT # (Read only) /ENABLE (Write only):** When this bit is a read, it reflects the state of PRESENT# pin (pin 141); when this bit is '0', it indicates a video decoder is connected to the V-Port.
	When written in V-Port mode (DCLK mode ≠ 00), this bit sets the state of the ENABLE pin (pin 143). This pin enables the video outputs of an external video decoder. Because decoders can have an active-high or active-low enable, the ENABLE pin tristates on reset and remains tristated until a non-zero value is written to the DCLK Mode bits (above); an external pull-up resistor should pull ENABLE to the correct inactive state at reset.
4	**16-bit Bus Width:** If this bit is '1', it indicates a 16-bit-wide bus; if this bit is '0' it indicates a 8-bit-wide bus. This is only the width of the V-Port bus, not the pixel depth of the video data. The earlier 24-bit option is dropped.

6.10   V-Port™ Mode Register (CL-GD5464 Only) *(cont.)*

Bit	Description

3:2   **Capture Mode [1:0]:** These two bits must be '10' to capture non-interlaced video. Capture logic detects whether each field is odd or even; even fields are defined as having HSYNC active at the trailing edge of VSYNC and odd fields are defined as having HSYNC inactive at the trailing edge of VSYNC.

If programmed for interlaced capture, capture starts with an odd field; the odd field is stored starting at buffer 0 (or '1') Y Address + 1. Even fields are stored starting at buffer 0 (or '1') Y Address. If programmed for interlaced capture and never has an odd field, the V-Port does not capture any data.

Capture Mode [1]	Capture Mode [0]	Capture Data For
1	1	Both fields
1	0	Even fields only
0	1	Odd fields only
0	0	Interlaced capture (odd field first)

1   **External HSYNC Polarity:** If this bit is '1', it is active high; if this bit is '0' it is active low.

0   **External VSYNC Polarity:** If this bit is '1', it is active high; if this bit is '0' it is active low.

6.11   Video Y Start Register (CL-GD5464 Only)

Size (bits):	16
MMI/O Offset	114h
Access Type	Read/Write

Bit	Description	Reset
15:9	Reserved	X
8:0	Video Y Start [8:0]	X

For scanlines less than Video Y Start, only Y data is captured and X decimation (V-Port Mode bit 13) is disabled; for scanlines greater than or equal then Video Y Start, Y, U, and V data is captured and the X decimation is controlled by V-Port Mode bit 13. If Video Y Start is '0', teletext capture is disabled. This register is only defined for YUV capture data.

This register aids in capture of teletext, closed caption, or VBI data that is transmitted only over the Y carrier; so decoding software does not have to discard U and V data. Also, by disabling X decimation, the decoding software has more data samples available for data bit detection and echo cancellation.

The X decimation is provided to reduce the pitch of the off-screen buffer by half in cases where it is would otherwise be greater than the frame buffer pitch. This is not required because capturing only Y data reduces the data by one-half, the same result as the X decimation.

Bit	Description
15:9	**Reserved**
8:0	**Video Y Start [8:0]**

6.12 Test Output Register (CL-GD5464 Only)

Size (bits):   16
MMI/O Offset   118h
Access Type   Read/Write

Bit	Description	Reset
15:12	Test Output, Byte [3:0]	0
11:0	Reserved	X

This register controls operation of the V-Port.

Bit	Description
15:12	**Test Output, Byte [3:0]:** This allows outputting either 24-bit digital RGB data or 32-bit test data from the video pipeline. In either case, the data is output from the end of the video pipeline, just prior to the DACs. These bits allow individual control of each byte of the test bus, so that digital RGB information can be output at the same time as V-Port data is being input on other bytes; this is necessary for V-Port operational testing on a digital tester or for simulation.

Values	A[15:8]	P[23:16]	P[15:8]	P[7:0]	Notes
0000	ROM Address	P[23:16]	P[15:8]	P[7:0]	Normal mode
1000	R[7:0] or Test[23:16]	P[23:16]	P[15:8]	P[7:0]	24-bit V-Port™ mode
1100	R[7:0] or Test[23:16]	G[7:0] or Test[15:8]	P[15:8]	P[7:0]	16-bit V-Port™ mode
1110	R[7:0] or Test[23:16]	G[7:0] or Test[15:8]	B[7:0] or Test[7:0]	P[7:0]	8-bit V-Port™ mode
1111	R[7:0] or Test[23:16]	G[7:0] or Test[15:8]	B[7:0] or Test[7:0]	Test[31:24]	Test mode (no input)

Bit	Description
11:0	**Reserved**