Miscellaneous Registers

10. MISCELLANEOUS REGISTERS

The Miscellaneous registers in the CL-GD546X are summarized in Table 10-1. These registers are accessible only with memory-mapped I/O (located in the defined address space in PCI10).

Table 10-1. Miscellaneous Registers Quick Reference

Register Name	MMI/O Offset	Size (Bits)	Page
BCLK Multiplier	8Ch	8	10-3
GPIO Timing	1FCh	16	10-4
GPIO Data	180h–1FFh	16	10-6
GPIO Configuration	1FEh	16	10-7
Serial Bus (I2C)	280h	16	10-9

10.1   BCLK Multiplier Register

Size (bits):	8
MMI/O Offset	8Ch
Access Type	Read/Write

Bit	Description
7	Use RCLK
6:5	Reserved
4:0	BCLK Multiplier [4:0]

This register specifies the frequency of BCLK (the Rambus clock).

Bit	Description
7	**Use RCLK:** If this bit is programmed to '1', the RCLK is connected directly to the clock input of the numerator counter in the BCLK PLL. This mode is intended for factory testing only.
6:5	**Reserved**
4:0	**BCLK Multiplier [4:0]:** This field directly programs the Rambus clock (BCLK) frequency.

$$BCLK \ = \ RCLK \bullet BCLK \ Multiplier \qquad\qquad \textbf{Equation 10-1}$$

The RCLK is the 14.31818-MHz reference clock and the BCLK multiplier can be programmed to any value from 7 to 22. This provides a range of 100.2 MHz to 315.0 MHz. The normal value is 18d (12h) giving a BCLK frequency of 257.7 MHz.
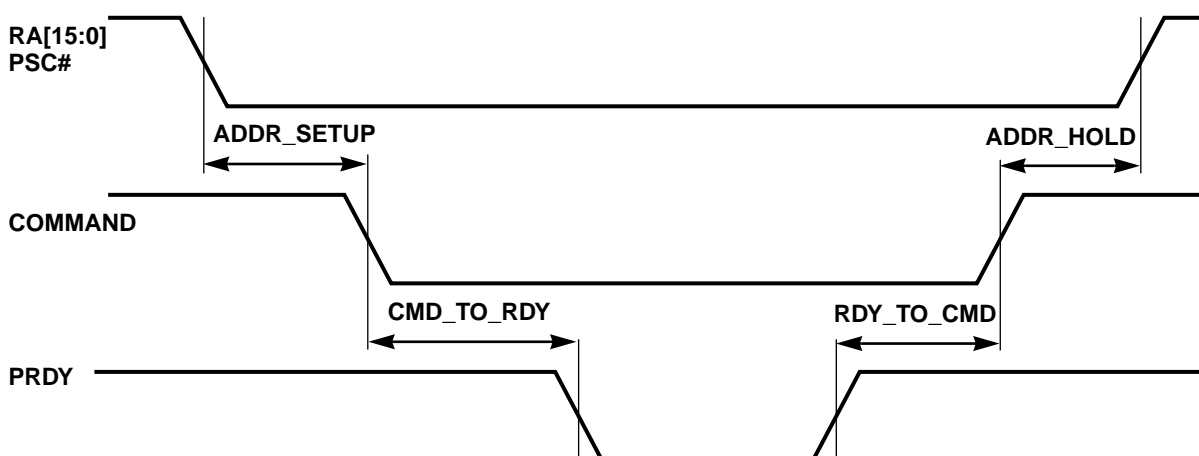
10.2 GPIO Timing Register

Size (bits):	16
MMI/O Offset	1FCh
Access Type	Read/Write

Bit	Description	Reset State
15	ADDR_HOLD [3]	0
14	ADDR_HOLD [2]	0
13	ADDR_HOLD [1]	1
12	ADDR_HOLD [0]	0
11	RDY_TO_CMD [3]	0
10	RDY_TO_CMD [2]	1
9	RDY_TO_CMD [1]	0
8	RDY_TO_CMD [0]	1
7	CMD_TO_RDY [3]	0
6	CMD_TO_RDY [2]	1
5	CMD_TO_RDY [1]	0
4	CMD_TO_RDY [0]	1
3	ADDR_SETUP [3]	0
2	ADDR_SETUP [2]	1
1	ADDR_SETUP [1]	1
0	ADDR_SETUP [0]	1

The four fields in this register specify the timing of the general-purpose I/O port. The following timing diagram is useful for understanding the fields in this register. The GPIO is discussed in detail in Appendix B7, "General-Purpose I/O Port".

NOTE: This register is only word addressable.

10.2 GPIO Timing Register *(cont.)*

Bit	Description
15:12	**ADDR_HOLD [3:0]:** This four-bit field specifies the number of memory clock cycles after the command is released and before the address and PSC# are released. The actual number of clocks is equal to the value programmed, except for zero, which defaults to one clock cycle.
11:8	**RDY_TO_CMD [3:0]:** Until the command is released, this four-bit field specifies the number of memory clock cycles after PRDY is sampled high. Before the command is released, the data from the peripheral during read cycles is sampled one clock cycle. The actual number of clocks is one more than the value programmed.
7:4	**CMD_TO_RDY [3:0]:** Until the GPIO interface starts sampling the PRDY input, this four-bit field specifies the number of memory clock cycles after the command is driven active. If it needs to extend the cycle, this is the period that the peripheral has to drive PRDY low. The actual number of clocks is one more than the value programmed.
3:0	**ADDR_SETUP [3:0]:** Until a command (for example, IOW# and IOR#) is driven active, this four-bit field specifies the number of memory clock cycles from RA[15:0] and PCS# that are valid. The actual number of clocks is one more than the value programmed.

10.3 GPIO Data Register

Size (bits):	16
MMI/O Offset	180h–1FFh
Access Type	Read/Write

Bit   **Description**

15:0   GPIO_DATA [15:0]

This group of addresses accesses the general-purpose I/O port. Writes to this group of addresses cause GPIO writes; reads from this group of addresses cause GPIO reads. Depending on the peripheral, the port is set up for the least-significant three, four, or six bits of the address that appear on the GPIO address bits. The actual address is the MMI/O address offset minus 180h. GPIO is described in Appendix B7, "General-Purpose I/O Port". Note that 8-bit cycles to peripherals that allow 16-bit cycles are not allowed.

Bit	Description
15:0	**GPIO_DATA [15:0]:** This 16-bit field accesses the GPIO port.

10.4 GPIO Configuration Register

Size (bits):	16
MMI/O Offset	1FEh
Access Type	Read only

Bit	Description
15:3	Reserved
2:0	GPIO Configuration [2:0]

This read-only register returns the GPIO Configuration bits latched from RA[6:4] at reset. The software can read this register to determine the type of local peripheral. Refer to Appendix B7, "General-Purpose I/O Port" for details of GPIO operation.

Bit	Description
15:3	**Reserved**

10.4   GPIO Configuration Register *(cont.)*

Bit	Description
2:0	**GPIO Configuration [2:0]:** This three-bit field returns the GPIO Configuration bits and is summarized in the following table.

V-Port™ Mode	GPIO 2:0 Configuration	
	CL-GD5462 RA[5:4]	**CL-GD5464 RA[6:4]**
C-CUBE CL480 (VMI mode 'A')	00	000
Reserved	01	001, 101–111
16-bit Intel® configuration	10	010
GPIO disabled	11	011
8-bit Intel® configuration (VMI mode 'B')	n/a	100

10.5 Serial Bus (I^{2}C) Register

Size (bits):	16
MMI/O Offset	280h
Access Type	Read/Write

Bit	Description
15	Serial Clock In
14:9	Reserved
8	Serial Data In
7	Serial Clock Out
6:1	Reserved
0	Serial Data Out

This register is used with the SCL and SDA pins to implement a I^{2}C (serial data) bus. Each of the two pins can be driven by and sensed on bits in this register.

Bit	Description
15	**Serial Clock In:** This read-only bit returns the state of the SCL pin. The SCL pin is low when the Serial Clock Out bit is programmed to '0', or when the responding device drives it low.
14:9	**Reserved**
8	**Serial Data In:** This read-only bit returns the state of the SDA pin. The SDA pin is low when the Serial Data Out bit is programmed to '0', or when the responding device drives it low.
7	**Serial Clock Out:** When this bit is '0', the SCL pin is driven low by the CL-GD546X.
6:1	**Reserved**
0	**Serial Data Out:** When this bit is '0', the SDA pin is driven low by the CL-GD546X.