VGA Core Registers

3. VGA CORE REGISTERS

The VGA Core registers in the CL-GD546X are summarized in Table 3-1. These are the registers that were defined in the IBM VGA. Some of these registers are accessible as memory-mapped I/O locations; the offset is indicated in the MMI/O offset column.

Table 3-1. VGA Core Registers Quick Reference

Register Name	PCI I/O Port	Index	MMI/O Offset	Page
MISC: Miscellaneous Output	3C2h (write)	–	80h	3-5
MISC: Miscellaneous Output	3CCh (read)	–	80h	3-5
FC: Feature Control	3?Ah (write)[a]	–	–	3-7
FC: Feature Control	3CAh (read)	–	–	3-7
FEAT: Input Status Register 0	3C2h	–	–	3-8
STAT: Input Status Register 1	3?Ah	–	–	3-9
Pixel Mask	3C6h	–	A0h	3-10
Palette Address (Read mode)	3C7h (write)	–	A4h	3-11
DAC State	3C7h (read)	–	A4h	3-12
Palette Address (Write mode)	3C8h (write)	–	A8h	3-13
Pixel Data	3C9h	–	ACh	3-14
SRX: Sequencer Index	3C4h	–	–	3-15
SR0: Sequencer Reset	3C5h	00h	–	3-16
SR1: Sequencer Clocking Mode	3C5h	01h	–	3-17
SR2: Sequencer Plane Mask	3C5h	02h	–	3-18
SR3: Sequencer Character Map Select	3C5h	03h	–	3-19
SR4: Sequencer Memory Mode	3C5h	04h	–	3-21
CRX: CRTC Index	3?4h	–	–	3-22
CR0: CRTC Horizontal Total	3?5h	00h	00h	3-25
CR1: CRTC Horizontal Display End	3?5h	01h	04h	3-26
CR2: CRTC Horizontal Blanking Start	3?5h	02h	08h	3-27
CR3: CRTC Horizontal Blanking End	3?5h	03h	0Ch	3-28
CR4: CRTC Horizontal Sync Start	3?5h	04h	10h	3-29
CR5: CRTC Horizontal Sync End	3?5h	05h	14h	3-30
CR6: CRTC Vertical Total	3?5h	06h	18h	3-31
CR7: CRTC Overflow	3?5h	07h	1Ch	3-32

Table 3-1. VGA Core Registers Quick Reference *(cont.)*

Register Name	PCI I/O Port	Index	MMI/O Offset	Page
CR8: CRTC Screen A Preset	3?5h	08h	20h	3-33
CR9: CRTC Character Cell Height	3?5h	09h	24h	3-34
CRA: CRTC Text Cursor Start	3?5h	0Ah	28h	3-35
CRB: CRTC Text Cursor End	3?5h	0Bh	2Ch	3-36
CRC: CRTC Screen Start Address High	3?5h	0Ch	30h	3-37
CRD: CRTC Screen Start Address Low	3?5h	0Dh	34h	3-38
CRE: CRTC Text Cursor Location High	3?5h	0Eh	38h	3-39
CRF: CRTC Text Cursor Location Low	3?5h	0Fh	3Ch	3-40
CR10: CRTC Vertical Sync Start	3?5h	10h	40h	3-41
CR11: CRTC Vertical Sync End	3?5h	11h	44h	3-42
CR12: CRTC Vertical Display End	3?5h	12h	48h	3-43
CR13: CRTC Offset	3?5h	13h	4Ch	3-44
CR14: CRTC Underline Row Scanline	3?5h	14h	50h	3-45
CR15: CRTC Vertical Blank Start	3?5h	15h	54h	3-46
CR16: CRTC Vertical Blank End	3?5h	16h	58h	3-47
CR17: CRTC Mode Control	3?5h	17h	5Ch	3-48
CR18: CRTC Line Compare	3?5h	18h	60h	3-50
CR22: Graphics Data Latches Readback	3?5h	22h	–	3-51
CR24: Attribute Controller Toggle Readback	3?5h	24h	–	3-52
CR26: Attribute Controller Index Readback	3?5h	26h	–	3-53
GRX: Graphics Controller Index	3CEh	–	–	3-54
GR0: Graphic Controller Set/Reset	3CFh	00h	–	3-55
GR1: Graphics Controller Set/Reset Enable	3CFh	01h	–	3-56
GR2: Graphics Controller Color Compare	3CFh	02h	–	3-57
GR3: Graphics Controller Data Rotate	3CFh	03h	–	3-58
GR4: Graphics Controller Read Map Select	3CFh	04h	–	3-59
GR5: Graphics Controller Mode	3CFh	05h	–	3-60
GR6: Graphics Controller Miscellaneous	3CFh	06h	–	3-62
GR7: Graphics Controller Color Don’t Care	3CFh	07h	–	3-63
GR8: Graphics Controller Bit Mask	3CFh	08h	–	3-64
ARX: Attribute Controller Index	3C0h/3C1h	–	7Ch	3-65

Table 3-1. VGA Core Registers Quick Reference *(cont.)*

Register Name	PCI I/O Port	Index	MMI/O Offset	Page
AR0–ARF: Attribute Controller Palette	3C0h/3C1h	00h–0Fh	–	3-66
AR10: Attribute Controller Mode	3C0h/3C1h	10h	–	3-67
AR11: Overscan (Border) Color	3C0h/3C1h	11h	–	3-69
AR12: Color Plane Enable	3C0h/3C1h	12h	–	3-70
AR13: Pixel Panning	3C0h/3C1h	13h	–	3-71
AR14: Color Select	3C0h/3C1h	14h	–	3-72

[a] '?' in the above register addresses is 'B' in Monochrome mode and 'D' in Color mode.

3.1 MISC: Miscellaneous Output Register

I/O Port Address: PCI	3C2h (write), 3CCh (read)
Index	–
Size (bits):	8
MMI/O Offset	80h
Access Type	Read/Write

Bit	Description
7	Vertical Sync Polarity
6	Horizontal Sync Polarity
5	Page Select
4	Reserved
3:2	Clock Select [1:0]
1	Enable Display Memory
0	CRTC I/O Address

This is one of the standard VGA registers. This register is accessible at MMI/O offset 80h as well as the standard I/O addresses.

Bit	Description
7	**Vertical Sync Polarity:** If this bit is '0', the vertical sync is a normally low signal, going high to indicate the beginning of sync time. If this bit is '1', the vertical sync is a normally high signal, going low to indicate the beginning of sync time.
6	**Horizontal Sync Polarity:** If this bit is '0', the horizontal sync is a normally low signal, going high to indicate the beginning of sync time. If this bit is '1', the horizontal sync is a normally high signal, going low to indicate the beginning of sync time. For some monitors, the polarity of vertical and horizontal sync indicate the number of scanlines per frame as summarized below:

MISC[7]	MISC[6]	Vertical Size
0 (+)	0 (+)	Reserved
0 (+)	1 (–)	400
1 (–)	0 (+)	350
1 (–)	1 (–)	480

3.1 MISC: Miscellaneous Output Register *(cont.)*

Bit **Description**

5 **Page Select:** This bit affects the meaning of the least-significant bit of the display memory address when in Even/Odd modes (SR4[2] = 1). If this bit is '0', only odd memory locations are selected. If this bit is '1', only even memory locations are selected.

NOTE: This bit is effective in modes 6, D, E, 11, and 12. This bit is ignored if the Chain Odd Maps to Even (GR6[1]), or Chain4 (SR4[3]) bits are enabled.

4 **Reserved**

3:2 **Clock Select [1:0]:** This 2-bit field is used to select among the four VCLK frequencies, as shown in the following table:

EDCLK#	Clock Select [1:0]	VCLK Source	Default Frequency
1	00	VCLK0	25.180 MHz
1	01	VCLK1	28.325 MHz
1	10	VCLK2	41.165 MHz
1	11	VCLK3	36.082 MHz
0	XX	DCLK pin (DAC and CRTC counters)	–

NOTE: Refer to the "2D PROGRAMMER'S GUIDE" chapter, for programming VCLK frequencies other than those in the table above.

1 **Enable Display Memory:** If this bit is '0', the CL-GD546X does not respond to any access to display memory. If this bit is '1', the CL-GD546X responds normally to accesses to display memory.

0 **CRTC I/O Address:** This bit selects I/O addresses for either Monochrome or Color mode. The affected addresses are summarized in the table below:

MISC[0]	ISR/FC	CRTC Index	CRTC Data	Mode
0	3BA	3B4	3B5	Monochrome
1	3DA	3D4	3D5	Color

3.2 FC: Feature Control Register

I/O Port Address: PCI	3?Ah (write), 3CAh (read)
Index	–
Size (bits):	8
MMI/O Offset	–
Access Type	Read/Write

Bit	Description	Reset State
7:4	Reserved	
3	VSYNC Control	0
2:0	Reserved	

This is one of the original IBM PC registers.

Bit	Description
7:4	**Reserved**
3	**VSYNC Control:** If this bit is '1', VSYNC is logically OR'ed with Display Enable (an internal signal) prior to going to the VSYNC pin. If this bit is '0', VSYNC is unchanged.
2:0	**Reserved**

NOTE: '?' in the above register addresses is 'B' in Monochrome mode and 'D' in Color mode.

3.3 FEAT: Input Status Register 0

I/O Port Address: PCI	3C2h
Index	–
Size (bits):	8
MMI/O Offset	–
Access Type	Read only

Bit	Description
7	Interrupt Pending
6:5	Reserved
4	DAC Sensing
3:0	Reserved

This is one of the registers in the IBM VGA. Only a couple of bits retain any meaning. This register is read only.

Bit	Description
7	**Interrupt Pending:** If this bit is '1', an interrupt request is pending. If this bit is '0', no interrupt is pending. See the description of CR11 on page 3-42 for more information regarding the CL-GD546X interrupt system.
6:5	**Reserved**
4	**DAC Sensing:** This read-only bit is used by the Cirrus Logic BIOS to determine whether a monitor is connected and if so, whether it is color or monochrome.
3:0	**Reserved**

3.4 STAT: Input Status Register 1

I/O Port Address: PCI	3?Ah
Index	–
Size (bits):	8
MMI/O Offset	–
Access Type	Read only

Bit	Description
7:6	Reserved
5:4	Diagnostic [1:0]
3	Vertical Retrace
2:1	Reserved
0	Display Enable

This read-only register contains some VGA Status bits.

Bit	Description
7:6	**Reserved**
5:4	**Diagnostic [1:0]:** These bits follow two of eight outputs of the Attribute Controller. The selection is made according to AR12[5:4] (Color Plane Enable register) as indicated in the following table:

AR12[5]	AR12[4]	STAT[5]	STAT[4]
0	0	P[2]	P[0]
0	1	P[5]	P[4]
1	0	P[3]	P[1]
1	1	P[7]	P[6]

3	**Vertical Retrace:** ‘1’ indicates that vertical retrace is in progress.
2:1	**Reserved**
0	**Display Enable:** If this bit is read as ‘0’, video is being serialized and displayed. If this bit is read as ‘1’, vertical or horizontal blanking is active.

NOTE: ‘?’ in the above register addresses is ‘B’ in Monochrome mode and ‘D’ in Color mode.

3.5 Pixel Mask Register

I/O Port Address: PCI	3C6h
Index	–
Size (bits):	8
MMI/O Offset	A0h
Access Type	Read/Write

Bit	Description
7:0	Pixel Mask [7:0]

The bits in this register form the pixel mask for the palette DAC. This is typically programmed to all ‘1’s by the Cirrus Logic BIOS. This register is accessible at MMI/O offset A0h as well as the standard VGA I/O address.

Bit	Description
7:0	**Pixel Mask [7:0]:** This field is the pixel mask for the palette DAC. If a bit in this field is ‘0’, the corresponding bit in the pixel data is ignored in looking up an entry in the LUT.

3.6 Palette Address Register (Read Mode, Write Only)

I/O Port Address: PCI	3C7h
Index	–
Size (bits):	8
MMI/O Offset	A4h
Access Type	Write only

Bit	Description
7:0	Palette Address (Read mode) [7:0]

The bits in this write-only register specify the address (Read mode) for the palette. This is used to specify the entry to be read in the LUT. This register is accessible at MMI/O offset A4h.

Bit	Description
7:0	**Palette Address (Read mode) [7:0]:** This field is the address (Read mode) for the LUT. This address is incremented after every third read of the Pixel Data register.

3.7 DAC State Register (Read Only)

I/O Port Address: PCI	3C7h
Index	–
Size (bits):	8
MMI/O Offset	A4h
Access Type	Read only

Bit	Description
7:2	Reserved
1:0	DAC State [1:0]

The bits in this read-only register indicate whether a read or a write occurred last to the LUT. This register is accessible at MMI/O offset A4h.

Bit	Description
7:2	**Reserved**
1:0	**DAC State [1:0]:** This field indicates whether the Palette Address (Read) register or the Palette Address (Write) register was accessed last. These two bits are always the same. If they are ‘0,0’, a write operation is in progress. If they are ‘1,1’, a read operation is in progress. The same information is available from the *Palette State Register* on page 5-3 at MMI/O offset B0h.

3.8 Palette Address Register (Write Mode, Write Only)

I/O Port Address: PCI	3C8h
Index	–
Size (bits):	8
MMI/O Offset	A8h
Access Type	Write only

Bit	Description
7:0	Palette Address (Write mode) [7:0]

The bits in this register form the address (Write mode) for the palette DAC. This is used to specify the entry to be written in the LUT. This register is accessible at MMI/O offset A8h.

Bit	Description
7:0	**Palette Address (Write mode) [7:0]:** This field is the Palette Address (Write mode) for the LUT. This address is incremented after every third write to the Pixel Data register.

3.9 Pixel Data Register

I/O Port Address: PCI	3C9h
Index	–
Size (bits):	8
MMI/O Offset	ACh
Access Type	Read/Write

Bit	Description
7	Pixel Data [7]
6	Pixel Data [6]
5	Pixel Data [5]
4	Pixel Data [4]
3	Pixel Data [3]
2	Pixel Data [2]
1	Pixel Data [1]
0	Pixel Data [0]

This is the Pixel Data register for the palette DAC. This read/write register is accessible at MMI/O offset ACh.

Bit	Description
7:0	**Pixel Data [7:0]:** This 8-bit field is the pixel data for the palette DAC. Prior to writing to this register, 3C8h is written with the first or only palette address. Then three values, corresponding to red, green, and blue are written to this address. Following the third write, the values are actually transferred to the LUT and the palette address is incremented in case the values for the next address are to be written. Prior to reading from this register, 3C7h is written with the first or only palette address. Then three values, corresponding to red, green, and blue can be read from this address. Following the third read, the palette address is incremented in case the values for the next address are to be read.

3.10 SRX: Sequencer Index Register

I/O Port Address: PCI	3C4h
Index	–
Size (bits):	8
MMI/O Offset	–
Access Type	Read/Write

Bit	Description
7:5	Reserved
4:0	Sequencer Index [4:0]

This register is used to specify the register in the sequencer block to be accessed by the next I/O read or write to address 3C5h. Indices greater than five point to the registers are defined in Chapter 4, “Extended I/O Registers”.

Bit	Description
7:5	**Reserved**
4:0	**Sequencer Index [4:0]:** This field selects the register to be accessed with the next I/O read or I/O write to 3C5h.

3.11 SR0: Sequencer Reset Register

I/O Port Address: PCI	3C5h
Index	00h
Size (bits):	8
MMI/O Offset	–
Access Type	Read/Write

Bit	Description	Reset State
7:2	Reserved	
1	Synchronous Reset	1
0	Asynchronous Reset	1

This register is used to reset the sequencer. These bits are for compatibility only and never need to be used in the CL-GD546X.

Bit	Description
7:2	**Reserved**
1	**Synchronous Reset:** If this bit is '0', the sequencer is cleared and halted. This disables screen refresh and display memory refresh. If this bit is '1', the sequencer operates normally if SR0[0] is '1'.
0	**Asynchronous Reset:** If this bit is '0', the sequencer is cleared and halted. In addition, SR3 is cleared. If this bit is '1', the sequencer operates normally if SR0[1] is '1'.

3.12 SR1: Sequencer Clocking Mode Register

I/O Port Address: PCI	3C5h
Index	01h
Size (bits):	8
MMI/O Offset	–
Access Type	Read/Write

Bit	Description
7:6	Reserved
5	Full Bandwidth
4	Shift and Load 32
3	Dot Clock ÷ 2
2	Shift and Load 16
1	Reserved
0	8/9 Dot Clock

This register is used to control some miscellaneous functions in the sequencer.

Bit	Description
7:6	**Reserved**
5	**Full Bandwidth:** If this bit is '1', screen refresh stops. This allows the CPU to use nearly 100 percent of the display memory bandwidth. HSYNC and VSYNC continue normally and display memory refresh continues. BLANK# is active and stays active. If this bit is '0', the CL-GD546X operates normally.
4	**Shift and Load 32:** This bit, in conjunction with bit 2 of this register, controls the Display Data Shifters in the graphics controller as shown below:
3	**Dot Clock ÷ 2:** If this bit is '1', the VCLK is divided by two to generate DCLK. This is used for low-resolution video modes such as 0, 1, 4, 5, and D. If this bit is '0', the master clock is not divided by two.
2	**Shift and Load 16:** See the description of bit 4 of this register.
1	**Reserved**
0	**8/9 Dot Clock:** If this bit is '1', DCLK is divided by eight to generate the character clock. If this bit is '0', DCLK is divided by nine to generate the character clock. This is used for 720 × 350 and 720 × 400 resolution AN (alphanumeric) modes.

SR1[4]	SR1[2]	Data Shifters Loaded
0	0	Every character clock
0	1	Every second character clock
1	x	Every fourth character clock

3.13 SR2: Sequencer Plane Mask Register

I/O Port Address: PCI	3C5h
Index	02h
Size (bits):	8
MMI/O Offset	–
Access Type	Read/Write

Bit	Description
7:4	Reserved
3:0	Map Enable [3:0]

This register is used to enable or disable writing to the four planes of display memory.

Bit	Description
7:4	**Reserved**
3:0	**Map Enable [3:0]:** These four bits are used to individually control whether bit planes 3:0 are written with Write modes 0 through 3.

3.14 SR3: Sequencer Character Map Select Register

I/O Port Address: PCI	3C5h
Index	03h
Size (bits):	8
MMI/O Offset	–
Access Type	Read/Write

Bit	Description
7:6	Reserved
5	Secondary Map Select [0]
4	Primary Map Select [0]
3:2	Secondary Map Select [2:1]
1:0	Primary Map Select [2:1]

This register is used to specify the primary and secondary character sets (fonts). This is used only for text modes.

Bit	Description
7:6	**Reserved**
5, 3:2	**Secondary Map Select [2:0]:** These three bits select the Secondary Character Map according to the following table:

SR3[5]	SR3[3]	SR3[2]	Map	Offset
0	0	0	0	0K
0	0	1	1	16K
0	1	0	2	32K
0	1	1	3	48K
1	0	0	4	8K
1	0	1	5	24K
1	1	0	6	40K
1	1	1	7	56K

3.14 SR3: Sequencer Character Map Select Register *(cont.)*

Bit	Description
4, 1:0	**Primary Map Select [2:0]:** These three bits select the Primary Character Map according to the following table:

SR3[4]	SR3[1]	SR3[0]	Map	Offset
0	0	0	0	0K
0	0	1	1	16K
0	1	0	2	32K
0	1	1	3	48K
1	0	0	4	8K
1	0	1	5	24K
1	1	0	6	40K
1	1	1	7	56K

NOTES:

1) In text modes, the ASCII text character is stored in Plane 0, the attribute is stored in Plane 1, and the font is stored in Plane 2.

2) Bit 3 of the Attribute byte normally controls the intensity of the foreground color. This bit can be redefined to be a switch between character sets, allowing 512 displayable characters. This switch is enabled whenever there is a difference between the values of the Primary Map Select and Secondary Map Select, and SR4[1] is '1'.

3) The format of the Plane 2 Font Address bits 15:0 is:

   F0 F1 F2 C7 C6 C5 C4 C3 C2 C1 C0 R4 R3 R2 R1 R0,

   where F[2:0] is the Character Map Select, C[7:0] is the ASCII character, and R[4:0] is the character row (scanline in the character cell).

3.15 SR4: Sequencer Memory Mode Register

I/O Port Address: PCI	3C5h
Index	04h
Size (bits):	8
MMI/O Offset	–
Access Type	Read/Write

Bit	Description
7:4	Reserved
3	Chain4
2	Odd/Even
1	Extended Memory
0	Reserved

This register is used to control some miscellaneous functions in the sequencer.

Bit	Description
7:4	**Reserved**
3	**Chain4:** If this bit is ‘1’, A0 provides Plane Select bit 0, and A1 provides Plane Select bit 1. This has an effect similar to Odd/Even mode, except that both A1 and A0 are used. This bit takes priority over SR4[2] (Odd/Even) and GR5[4]. There is not a separate bit in the graphics controller to select Chain4 as is the case with the Odd/Even bit. The Graphics Controller Read Map register (GR4) is ignored when this bit is ‘1’.
2	**Odd/Even:** If this bit is ‘0’, the sequencer is put into Odd/Even mode. Even CPU addresses access Planes 0 and 2; odd CPU addresses access Planes 1 and 3. This bit must be ‘0’ for text modes. The value of this bit must track GR5[4] (Odd/Even). The values are always opposite.
1	**Extended Memory:** If this bit is ‘0’, the effective memory size is 64K, regardless of the memory actually installed. EGA modes require this to be the case. If this bit is ‘1’, the effective memory size is equal to the actual memory installed.
0	**Reserved**

3.16 CRX: CRTC Index Register

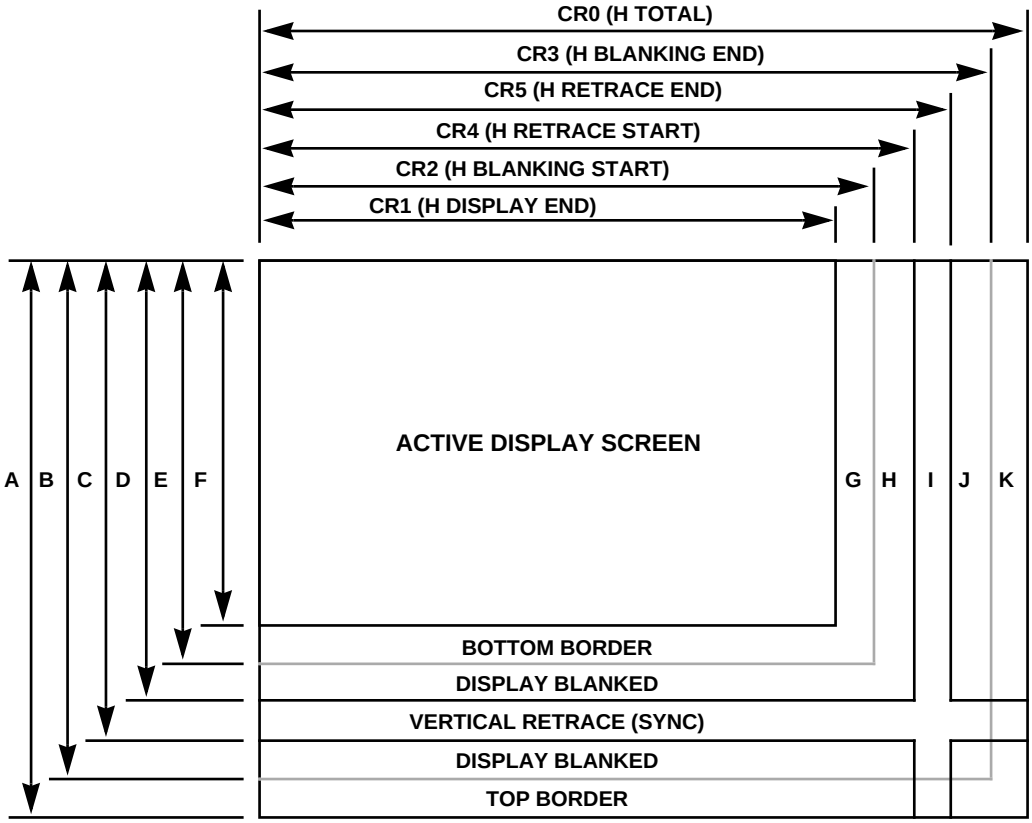
I/O Port Address: PCI	3?4h
Index	–
Size (bits):	8
MMI/O Offset	–
Access Type	Read/Write

Bit	Description
7:6	Reserved
5:0	CRTC Index [5:0]

This register is used to specify the register in the CRTC block to be accessed by the next I/O read or I/O write to address 3?5h. The registers with indices greater than 18h (except CR22, CR24, and CR26) are described in Chapter 4, "Extended I/O Registers".

Bit	Description
7:6	**Reserved**
5:0	**CRTC Index [5:0]:** This value points to the register to be accessed in the next I/O read or I/O write to address 3?5h. **NOTE:** Registers above 18h were never documented by IBM.

NOTE: '?' in the above register addresses is 'B' in Monochrome mode and 'D' in Color mode.



A - CR6 (V TOTAL)
B - CR16 (V BLANKING END)
C - CR11 (V RETRACE END)
D - CR10 (V RETRACE START)
E - CR15 (V BLANKING START)
F - CR12 (V DISPLAY END)
G - RIGHT BORDER
H - DISPLAY BLANKED
I - HORIZONTAL RETRACE (SYNC)
J - DISPLAY BLANKED
K - LEFT BORDER

Figure 3-1. CRTC Timing Registers

The Extension and Overflow bits are organized by parameter and bit position in Table 3-2.

Table 3-2. Summary of CRTC Timing Registers

Parameter	10	9	8	7	6	5	4:0
H Total			CR1E[7]	CR0[7]	CR0[6]	CR0[5]	CR0[4:0]
H Display End			CR1E[6]	CR1[7]	CR1[6]	CR1[5]	CR1[4:0]
H Blank Start			CR1E[5]	CR2[7]	CR2[6]	CR2[5]	CR2[4:0]
H Blank End				CR1A[5]	CR1A[4]	CR5[7]	CR3[4:0]
H Sync Start			CR1E[4]	CR4[7]	CR4[6]	CR4[5]	CR4[4:0]
H Sync End							CR5[4:0]
V Total	CR1E[3]	CR7[5]	CR7[0]	CR6[7]	CR6[6]	CR6[5]	CR6[4:0]
V Display End	CR1E[2]	CR7[6]	CR7[1]	CR12[7]	CR12[6]	CR12[5]	CR12[4:0]
V Blank Start	CR1E[1]	CR9[5]	CR7[3]	CR15[7]	CR15[6]	CR15[5]	CR15[4:0]
V Blank End		CR1A[7]	CR1A[6]	CR16[7]	CR16[6]	CR16[5]	CR16[4:0]
V Sync Start	CR1E[0]	CR7[7]	CR7[2]	CR10[7]	CR10[6]	CR10[5]	CR10[4:0]
V Sync End							CR11[3:0]
Line Compare		CR9[6]	CR7[4]	CR18[7]	CR18[6]	CR18[5]	CR18[4:0]
Offset		CR1D[0]	CR1B[4]	CR13[7]	CR13[6]	CR13[5]	CR13[4:0]

The Extension and Overflow bits for the Screen Start A value are shown in Table 3-3.

Table 3-3. Screen Start A Extensions

20:19	18:17	16	15:8	7:0
CR1D[4:3]	CR1B[3:2]	CR1B[0]	CRC[7:0]	CRD[7:0]

In 8-, 16-, 24-, and 32-bits-per-pixel Extended modes, the display start address is programmed as follows:

	7	6	5	4	3	2	1	0	
CR0D	X	X	X	X	X	X	X	–	Tiling disabled
CR0D	X	X	X	0	0	0	0	0	128-byte wide tiles enabled
CR0D	X	X	0	0	0	0	0	0	256-byte wide tiles enabled

Where ‘0’ is 0b, ‘–’ is not used, and ‘X’ is 0b|1b.

3.17 CR0: CRTC Horizontal Total Register

I/O Port Address: PCI	3?5h
Index	00h
Size (bits):	8
MMI/O Offset	00h
Access Type	Read/Write

Bit	Description
7:0	Horizontal Total [7:0]

This register is used to specify the total number of character clocks per horizontal period.

Bit	Description
7:0	**Horizontal Total [7:0]:** This register specifies the total number of character clocks per horizontal period. This is extended to nine bits with CR1E[7]. The character clock (derived from the VCLK according to the character width) is counted in the character counter. The value of the character counter is compared with the value in this register to provide the basic horizontal timing. All horizontal and vertical timing is eventually derived from this register. The value in the register is 'Total number of character times minus five'. Figure 3-1 indicates the way the horizontal and vertical timing is defined. The horizontal timing is calculated in terms of character clock periods and the vertical timing is calculated in terms of horizontal periods. Table 3-2 indicates how the various CRTC Timing registers are extended.

NOTE: '?' in the above register addresses is 'B' in Monochrome mode and 'D' in Color mode.

3.18 CR1: CRTC Horizontal Display End Register

I/O Port Address: PCI	3?5h
Index	01h
Size (bits):	8
MMI/O Offset	04h
Access Type	Read/Write

Bit	Description
7:0	Horizontal Display End [7:0]

This register is used to specify the number of character clocks during horizontal display time.

Bit	Description
7:0	**Horizontal Display End [7:0]:** This register specifies the number of character clocks during horizontal display time. This is extended to nine bits with CR1E[6]. For text modes, this is the number of characters; for graphics modes, this is the number of pixels in each scanline divided by the number of pixels in each character clock. The number is usually eight, but can be 16 for modes that use clock doubling. The value in the field is the number of character clocks minus one. Refer to Figure 3-1 and Table 3-2 for a summary of CRTC Timing registers.

NOTE: '?' in the above register addresses is 'B' in Monochrome mode and 'D' in Color mode.

3.19 CR2: CRTC Horizontal Blanking Start Register

I/O Port Address: PCI	3?5h
Index	02h
Size (bits):	8
MMI/O Offset	08h
Access Type	Read/Write

Bit	Description
7:0	Horizontal Blanking Start [7:0]

This register is used to specify the character count where horizontal blanking starts.

Bit	Description
7:0	**Horizontal Blanking Start [7:0]:** The contents of this register specify the character count where horizontal blanking starts. This field is extended with CR1E[5]. The value programmed into CR2 and its extension must always be larger than the value programmed into CR1 and its extension. Refer to Figure 3-1 and Table 3-2 for a summary of CRTC Timing registers.

NOTE: '?' in the above register addresses is 'B' in Monochrome mode and 'D' in Color mode.

3.20 CR3: CRTC Horizontal Blanking End Register

I/O Port Address: PCI	3?5h
Index	03h
Size (bits):	8
MMI/O Offset	0Ch
Access Type	Read/Write

Bit	Description
7	Compatible Read
6:5	Display Enable Skew [1:0]
4:0	Horizontal Blanking End [4:0]

This register is used to determine the width of the horizontal blanking period. In addition, this register controls display enable skew and access to CR10 and CR11.

Bit

7 **Compatible Read:** If this bit is '0', registers CR10 and CR11 are write-only registers. If this bit is '1', registers CR10 and CR11 are read/write registers.

6:5 **Display Enable Skew [1:0]:** This 2-bit field is used to specify the number of character clocks that display enable is to be delayed from horizontal total. This is necessary to compensate for the accesses of the character code and Attribute byte, the accesses of the font, etc. The following table indicates the coding of CR3[6:5].

CR3[6]	CR3[5]	Skew	Note
0	0	0	
0	1	1	Typical setting
1	0	2	
1	1	3	

NOTE: If the skew is too low, the left-most character is repeated. If the skew is too high, one or more characters disappear at the left of each character row.

4:0 **Horizontal Blanking End [4:0]:** This field determines the width of the horizontal blanking period. This field is extended with CR5[7] and CR1A[5:4] (if enabled). The least-significant five through eight bits of the character counter are compared with the contents of this field. When a match occurs, the horizontal blanking period is ended. Note that the horizontal blanking period is limited to 63 or 255 character-clock times. The value to be programmed into this register can be calculated by adding the desired blanking period to the value programmed into CR2 (horizontal blanking start). The blanking period must never be extend past the horizontal total.

If CR1B[5] or CR1B[7] is '1', this field is extended with Extension register CR1A[5:4].

Refer to Figure 3-1 and Table 3-2 for a summary of CRTC Timing registers.

NOTE: '?' in the above register addresses is 'B' in Monochrome mode and 'D' in Color mode.

3.21 CR4: CRTC Horizontal Sync Start Register

I/O Port Address: PCI	3?5h
Index	04h
Size (bits):	8
MMI/O Offset	10h
Access Type	Read/Write

Bit	Description
7:0	Horizontal Sync Start [7:0]

This register specifies where Horizontal Sync becomes active.

Bit	Description
7:0	**Horizontal Sync Start [7:0]:** This field specifies the character count where HSYNC becomes active. This is extended with CR1A[4]. Adjusting the value in this field moves the display horizontally on the screen. The Horizontal Sync Start *must* be equal to or greater than Horizontal Display End. The time from Horizontal Sync Start to Horizontal Total *must* be equal to or greater than four character times. Refer to Figure 3-1 and Table 3-2 for a summary of CRTC Timing registers.

NOTE: '?' in the above register addresses is 'B' in Monochrome mode and 'D' in Color mode.

3.22 CR5: CRTC Horizontal Sync End Register

I/O Port Address: PCI	3?5h
Index	05h
Size (bits):	8
MMI/O Offset	14h
Access Type	Read/Write

Bit	Description
7	Horizontal Blanking End [5]
6:5	Horizontal Sync Delay [1:0]
4:0	Horizontal Sync End [4:0]

This register specifies the position where the horizontal sync pulse ends, effectively specifying the width of the pulse. In addition, this register contains an overflow bit and a skew field.

Bit

7

Horizontal Blanking End [5]: This bit extends the horizontal blanking end value by one bit. Refer to Chapter 4, "Extended I/O Registers", register CR3 for an explanation of the horizontal blanking end value.

6:5

Horizontal Sync Delay [1:0]: This 2-bit field is used to delay the external horizontal sync pulse from the position implied in CR4. This is necessary in some modes to allow internal timing signals triggered from horizontal sync start to begin prior to display enable. The following table summarizes the HSYNC delay:

CR[6]	CR5[5]	Skew in Character Clocks
0	0	0
0	1	1
1	0	2
1	1	3

4:0

Horizontal Sync End [4:0]: This field determines the width of the horizontal sync pulse. The least-significant five bits of the character counter are compared with the contents of this field. When a match occurs, the horizontal sync pulse ends. Note the horizontal sync pulse is limited to 31 character-clock times. The value to be programmed into this register can be calculated by adding the desired sync width with the value programmed into CR4. The sync pulse must never be extend past the horizontal total. In addition, HSYNC must always end during the horizontal blanking period.

Refer to Figure 3-1 and Table 3-2 for a summary of CRTC Timing registers.

NOTE: '?' in the above register addresses is 'B' in Monochrome mode and 'D' in Color mode.

3.23 CR6: CRTC Vertical Total Register

I/O Port Address: PCI	3?5h
Index	06h
Size (bits):	8
MMI/O Offset	18h
Access Type	Read/Write

Bit	Description
7:0	Vertical Total [7:0]

This register specifies the total number of scanlines per frame.

Bit	Description
7:0	**Vertical Total [7:0]:** This field is the least-significant eight bits of a 10-bit field that defines the total number of scanlines per frame. This field is extended with CR7[0], CR7[5], and CR1E[3]. The value programmed into the Vertical Total field is the total number of scanlines minus two. Refer to Figure 3-1 and Table 3-2 for a summary of CRTC Timing registers.

NOTE: '?' in the above register addresses is 'B' in Monochrome mode and 'D' in Color mode.

3.24 CR7: CRTC Overflow Register

I/O Port Address: PCI	3?5h
Index	07h
Size (bits):	8
MMI/O Offset	1Ch
Access Type	Read/Write

Bit	Description
7	Vertical Retrace Start [9]
6	Vertical Display End [9]
5	Vertical Total [9]
4	Line Compare [8]
3	Vertical Blanking Start [8]
2	Vertical Retrace Start [8]
1	Vertical Display End [8]
0	Vertical Total [8]

This register contains bits that extend various vertical count fields. Refer to Figure 3-1 and Table 3-2 for a summary of CRTC Timing registers. There are Cirrus Logic Extension bits in this register.

Bit	Description
7	**Vertical Retrace Start [9]:** This bit extends the Vertical Retrace Start (CR10) field to 10 bits.
6	**Vertical Display End [9]:** This bit extends the Vertical Display End (CR12) field to 10 bits.
5	**Vertical Total [9]:** This bit extends the Vertical Total (CR6) field to 10 bits.
4	**Line Compare [8]:** This bit extends the Line Compare (CR18) field to nine bits.
3	**Vertical Blanking Start [8]:** This bit extends the Vertical Blanking Start (CR15) field to nine bits.
2	**Vertical Retrace Start [8]:** This bit extends the Vertical Retrace Start (CR10) field to nine bits.
1	**Vertical Display End [8]:** This bit extends the Vertical Display End (CR12) field to nine bits.
0	**Vertical Total [8]:** This bit extends the Vertical Total (CR6) field to nine bits.

NOTE: '?' in the above register addresses is 'B' in Monochrome mode and 'D' in Color mode.

3.25 CR8: CRTC Screen A Preset Row-Scan Register

I/O Port Address: PCI	3?5h
Index	08h
Size (bits):	8
MMI/O Offset	20h
Access Type	Read/Write

Bit	Description
7	Reserved
6:5	Byte Pan [1:0]
4:0	Screen A Preset Row Scan [4:0]

This register specifies the row scanline where Screen A begins, allowing scrolling on a scanline basis (soft scroll). In addition, this register specifies the byte pan (coarse panning).

Bit **Description**

7 **Reserved**

6:5 **Byte Pan [1:0]:** This two-bit field controls coarse panning. It can specify a pan of up to 24 pixels with a resolution of eight pixels. AR13 provides for panning on a pixel basis. The values programmed into CR8[6:5] are interpreted as indicated in the following table:

CR8[6]	CR8[5]	Bytes	Pixels
0	0	0	0
0	1	1	8
1	0	2	16
1	1	3	24

4:0 **Screen A Preset Row Scan [4:0]:** This field specifies the scanline where the first character row begins. This provides scrolling on a scanline basis (soft scrolling). The contents of this field should be changed only during vertical retrace time.

NOTE: '?' in the above register addresses is 'B' in Monochrome mode and 'D' in Color mode.

3.26 CR9: CRTC Character Cell Height Register

I/O Port Address: PCI	3?5h
Index	09h
Size (bits):	8
MMI/O Offset	24h
Access Type	Read/Write

Bit	Description
7	CRTC Scan Double
6	Line Compare [9]
5	Vertical Blank Start [9]
4:0	Character Cell Height [4:0]

This register specifies the number of scanlines in the character cell. In addition, it contains two vertical overflow bits and one control bit.

Bit	Description
7	**CRTC Scan Double:** If this bit is '1', every scanline is displayed twice in succession. The scanline counter-based parameters (character height, cursor start and end, and underline location) double. This bit is typically used to display 200-line modes at 400 scanlines. This function is not available in Interlaced Video modes.
6	**Line Compare [9]:** This bit extends the line compare field (CR18) to 10 bits.
5	**Vertical Blank Start [9]:** This bit extends the vertical blank start field (CR15) to 10 bits.
4:0	**Character Cell Height [4:0]:** This field specifies the vertical size of the character cell in terms of scanlines. The value programmed into this field is the actual size minus one. Refer to Figure 3-1 and Table 3-2 for a summary of CRTC Timing registers.

NOTE: '?' in the above register addresses is 'B' in Monochrome mode and 'D' in Color mode.

3.27 CRA: CRTC Text Cursor Start Register

I/O Port Address: PCI	3?5h
Index	0Ah
Size (bits):	8
MMI/O Offset	28h
Access Type	Read/Write

Bit	Description
7:6	Reserved
5	Disable Text Cursor
4:0	Text Cursor Start [4:0]

This register specifies the scanline where the text cursor is to begin. In addition, this register contains a bit that disables the text cursor.

Bit	Description
7:6	**Reserved**
5	**Disable Text Cursor:** If this bit is '1', the text cursor is disabled (that is, it is removed). If this bit is '0', the text cursor functions normally.
4:0	**Text Cursor Start [4:0]:** This field specifies the scanline within the character cell where the text cursor starts. If the Text Cursor Start value is greater than the Text Cursor End value, there is no text cursor displayed. If the Text Cursor Start value is equal to the Text Cursor End value, the text cursor occupies a single scanline.

NOTE: '?' in the above register addresses is 'B' in Monochrome mode and 'D' in Color mode.

3.28 CRB: CRTC Text Cursor End Register

I/O Port Address: PCI	3?5h
Index	0Bh
Size (bits):	8
MMI/O Offset	2Ch
Access Type	Read/Write

Bit	Description
7	Reserved
6:5	Text Cursor Skew [1:0]
4:0	Text Cursor End [4:0]

This register specifies the scanline within the character cell where the text cursor is to end. It also contains a field that allows the text cursor to be skewed from the location specified in registers CRE and CRF.

Bit	Description
7	**Reserved**
6:5	**Text Cursor Skew [1:0]:** This two-bit field specifies a delay, in character clocks, from the text cursor location specified in CRE and CRF to the actual cursor.
4:0	**Text Cursor End [4:0]:** This field specifies the scanline within the character where the text cursor ends. A value greater than the character cell height yields an effective ending value equal to the cell height.

NOTE: '?' in the above register addresses is 'B' in Monochrome mode and 'D' in Color mode.

3.29 CRC: CRTC Screen Start Address High Register

I/O Port Address: PCI	3?5h
Index	0Ch
Size (bits):	8
MMI/O Offset	30h
Access Type	Read/Write

Bit	Description
7:0	Screen Start A Address [15:8]

This register and register CRD, with Cirrus Logic extension bits, specify the location in display memory where the data to be displayed on the screen begins.

Bit	Description
7:0	**Screen Start A Address [15:8]:** This field specifies the location in display memory where the screen begins. This register contains bits 15:8 of this value. Bits 7:0 are in register CRD, bits 18:16 are in CR1B, and bits 20:19 are in CR1D[7]. Refer to Figure 3-1 and Table 3-2 for a summary of CRTC Timing registers.

NOTE: '?' in the above register addresses is 'B' in Monochrome mode and 'D' in Color mode.

3.30 CRD: CRTC Screen Start Address Low Register

I/O Port Address: PCI	3?5h
Index	0Dh
Size (bits):	8
MMI/O Offset	34h
Access Type	Read/Write

Bit	Description
7:0	Screen Start A Address [7:0]

This register and register CRC specify the location in display memory where the data to be displayed on the screen begins.

Bit	Description
7:0	**Screen Start A Address [7:0]:** This field specifies the location in display memory where the screen begins. This register contains bits 7:0 of this value, bits 15:8 are in register CRD. Extension bits 18:16 are in register CR1B, and bits 20:19 are in CR1D. Refer to Figure 3-1 and Table 3-2 for a summary of the CRTC Timing registers.

NOTE: '?' in the above register addresses is 'B' in Monochrome mode and 'D' in Color mode.

3.31 CRE: CRTC Text Cursor Location High Register

I/O Port Address: PCI	3?5h
Index	0Eh
Size (bits):	8
MMI/O Offset	38h
Access Type	Read/Write

Bit	Description
7:0	Text Cursor Location [15:8]

This register and register CRF specify the location in display memory where the text cursor is to be displayed.

Bit	Description
7:0	**Text Cursor Location [15:8]:** The text cursor location is a 16-bit field that specifies the location in display memory where the text cursor is to be displayed. This register contains bits 15:8 of this field, and register CRF contains bits 7:0. **NOTE:** The value contained in this field is an address in display memory, not an offset from the beginning of the screen. If the value of Screen A Start is changed without a compensating change in the Text Cursor Location field, the text cursor moves on the screen. Refer to Figure 3-1 and Table 3-2 for a summary of CRTC Timing registers.

NOTE: '?' in the above register addresses is 'B' in Monochrome mode and 'D' in Color mode.

3.32 CRF: CRTC Text Cursor Location Low Register

I/O Port Address: PCI	3?5h
Index	0Fh
Size (bits):	8
MMI/O Offset	3Ch
Access Type	Read/Write

Bit	Description
7:0	Text Cursor Location [7:0]

This register and register CRE specify the location in display memory where the text cursor is to be displayed.

Bit	Description
7:0	**Text Cursor Location [7:0]:** This 16-bit field specifies the location in display memory where the text cursor is to be displayed. This register contains bits 7:0 of this field, and register CRE contains bits 15:8. Refer to Figure 3-1 and Table 3-2 for a summary of CRTC Timing registers.

NOTE: '?' in the above register addresses is 'B' in Monochrome mode and 'D' in Color mode.

3.33 CR10: CRTC Vertical Sync Start Register

I/O Port Address: PCI	3?5h
Index	10h
Size (bits):	8
MMI/O Offset	40h
Access Type	Read/Write

Bit	Description
7:0	Vertical Sync Start [7:0]

The Vertical Sync Start field specifies the scanline where the vertical sync pulse becomes active. This register contains the least-significant eight bits of that field.

Bit	Description
7:0	**Vertical Sync Start [7:0]:** This field specifies the scanline where the vertical sync pulse becomes active. This register contains bits 7:0 of that field. This register is extended by bits in registers CR7 and CR1E. Refer to Figure 3-1 and Table 3-2 for a summary of CRTC Timing registers.

NOTE: '?' in the above register addresses is 'B' in Monochrome mode and 'D' in Color mode.

3.34 CR11: CRTC Vertical Sync End Register

I/O Port Address: PCI	3?5h
Index	11h
Size (bits):	8
MMI/O Offset	44h
Access Type	Read/Write

Bit	Description
7	Write Protect CR7–CR0
6	Reserved
5	Disable Vertical Interrupt
4	Clear Vertical Interrupt
3:0	Vertical Sync End [3:0]

This register specifies the scanline where the vertical sync pulse becomes inactive, thereby effectively specifying the vertical sync pulse width. In addition, this register contains controls for the interrupt and two miscellaneous control bits.

Bit	Description
7	**Write Protect CR7–CR0:** If this bit is '1', registers CR0 through CR7 cannot be written. Writes addressed to those registers are simply ignored. CR7[4] (Line Compare Extension) can always be written. If this bit is '0', registers CR0 through CR7 can be written normally.
6	**Reserved:** This bit formerly controlled the DRAM refresh, selecting between three or five cycles per scanline. The DRAM refresh logic has been replaced with new logic for Rambus that uses other controls. Refer to Chapter 7, "Rambus® Registers" for additional information.
5	**Disable Vertical Interrupt:** If this bit is '1', the vertical interrupt is disabled. The Interrupt pin is never active. If this bit is '0', the vertical interrupt is enabled and functions normally. If this bit is '1', FEAT[7] is cleared to zero, but not the Interrupt pin.
4	**Clear Vertical Interrupt:** If this bit is '0', the Interrupt Pending bit (FEAT[7]) is cleared to '0', and the Interrupt pin is forced inactive. Programming this bit to '1' allows the next occurrence of the interrupt. This can be done immediately after programming this bit to '0'.
3:0	**Vertical Sync End [3:0]:** This field determines the width of the vertical sync pulse. The least-significant four bits of the scanline counter are compared with the contents of this field. When a match occurs, the vertical sync pulse ends. Note that the vertical sync pulse is limited to 15 scanlines. The value to be programmed into this register can be calculated by subtracting the desired sync width from the value programmed into the Vertical Sync Start field. The sync pulse must never extend past the Vertical Total. Refer to Figure 3-1 and Table 3-2 for a summary of CRTC Timing registers.

NOTE: '?' in the above register addresses is 'B' in Monochrome mode and 'D' in Color mode.

3.35 CR12: CRTC Vertical Display End Register

I/O Port Address: PCI	3?5h
Index	12h
Size (bits):	8
MMI/O Offset	48h
Access Type	Read/Write

Bit	Description
7:0	Vertical Display End [7:0]

The Vertical Display End field is used to specify the scanline where the display is to end.

Bit	Description
7:0	**Vertical Display End [7:0]:** This field is used to specify the scanline where the display is to end. This register contains the least-significant eight bits of this field. Additional bits are in CR7 and CR1E. Refer to Figure 3-1 and Table 3-2 for a summary of CRTC Timing registers.

NOTE: '?' in the above register addresses is 'B' in Monochrome mode and 'D' in Color mode.

3.36 CR13: CRTC Offset Register

I/O Port Address: PCI	3?5h
Index	13h
Size (bits):	8
MMI/O Offset	4Ch
Access Type	Read/Write

Bit	Description
7:0	Offset [7:0]

This register specifies the distance in display memory between the beginnings of adjacent character rows or scanlines. This is sometimes referred to as display 'pitch'.

Bit	Description
7:0	**Offset [7:0]:** This register specifies the distance in display memory between the beginnings of adjacent character rows or scanlines. This field is extended to nine bits with CR1B[4] and to 10 bits with CR1D[0]. At the beginning of each scanline (except the first), the address that data should be fetched from is calculated by adding the contents of this register to the beginning address of the previous scanline or character row. The offset is left-shifted one or two-bit positions depending on CR17[6].

NOTE: '?' in the above register addresses is 'B' in Monochrome mode and 'D' in Color mode.

3.37 CR14: CRTC Underline Row Scanline Register

I/O Port Address: PCI	3?5h
Index	14h
Size (bits):	8
MMI/O Offset	50h
Access Type	Read/Write

Bit	Description
7	Reserved
6	DoubleWord Mode
5	Count by Four
4:0	Underline Scanline [4:0]

This register is used to specify the scanline where the underline appears. This is for VGA text modes only.

Bit	Description
7	**Reserved**
6	**DoubleWord Mode:** When this bit is '1', doubleword addresses are forced. The CRTC memory address counter is rotated left two-bit positions so that Display Memory Address bits 1 and 0 are sourced from CRTC Address Counter bits 13 and 12, respectively. When this bit is '0', CR17[6] controls whether the device uses byte or word addresses.
5	**Count by Four:** This bit must be '1' when DoubleWord mode is enabled to clock the memory address counter with the character clock divided by four. This bit must be '0' when DoubleWord mode is not enabled.
4:0	**Underline Scanline [4:0]:** This field specifies the scanline within the character cell where the underline occurs.

NOTE: '?' in the above register addresses is 'B' in Monochrome mode and 'D' in Color mode.

3.38 CR15: CRTC Vertical Blank Start Register

I/O Port Address: PCI	3?5h
Index	15h
Size (bits):	8
MMI/O Offset	54h
Access Type	Read/Write

Bit	Description
7:0	Vertical Blank Start [7:0]

This register specifies the scanline where blank becomes active.

Bit	Description
7:0	**Vertical Blank Start [7:0]:** This field specifies the scanline where Vertical Blank is to begin. The least-significant eight bits of that field are in this register. Overflow bits are in CR7 and CR9. This field is expanded with CR1E[1]. Refer to Figure 3-1 and Table 3-2 for a summary of CRTC Timing registers.

NOTE: '?' in the above register addresses is 'B' in Monochrome mode and 'D' in Color mode.

3.39 CR16: CRTC Vertical Blank End Register

I/O Port Address: PCI	3?5h
Index	16h
Size (bits):	8
MMI/O Offset	58h
Access Type	Read/Write

Bit	Description
7:0	Vertical Blank End [7:0]

The Vertical Blank End field specifies the scanline where Vertical Blank ends.

Bit	Description
7:0	**Vertical Blank End [7:0]:** This field specifies the scanline where Vertical Blank is to end. This register contains the least-significant eight bits of that field. If CR1B[5] is '1', this field is extended with CR1A[7:6]. The contents of the Vertical Blank End field are compared to the scanline counter to determine when to terminate Vertical Blank. This limits the duration of Vertical Blank to 255 scanlines if CR1B[5] is '0', or 1023 scanlines if CR1B[5] is '1'. Refer to Figure 3-1 and Table 3-2 for a summary of CRTC Timing registers.

NOTE: '?' in the above register addresses is 'B' in Monochrome mode and 'D' in Color mode.

3.40 CR17: CRTC Mode Control Register

I/O Port Address: PCI	3?5h
Index	17h
Size (bits):	8
MMI/O Offset	5Ch
Access Type	Read/Write

Bit	Description
7	Timing Enable
6	Byte/Word Mode
5	Address Wrap
4	Reserved
3	Count by Two
2	Multiply Vertical Registers by Two
1	Select Row-scan Counter
0	Compatibility Mode (CGA) Support

This register contains a number of miscellaneous control bits.

Bit	Description
7	**Timing Enable:** If this bit is '1', the CRTC timing logic is enabled and functions normally. If this bit is '0', the CRTC timing logic is disabled.
6	**Byte/Word Mode:** If this bit is '1', the contents of the CRTC address counter are sent to the display memory without being rotated. If this bit is '0', the contents of the CRTC address counter are rotated left one-bit position before being sent to the display memory.
5	**Address Wrap:** If CR17[6] is '1', this bit is ignored. If CR17[6] is '0' and this bit is '1', then the left rotation described above involves 16 bits of the CRTC address counter. If CR17[6] is '0' and this bit is '0', then the left rotation described above involves 14 bits of the CRTC address counter.
4	**Reserved**
3	**Count by Two:** If this bit is '1', then the CL-GD546X clocks the memory address counter with the character clock divided by two. If this bit is '0', then the CL-GD546X clocks the memory address counter with character clock.
2	**Multiply Vertical Registers by Two:** If this bit is '1', the scanline counter is clocked with horizontal sync divided by two. This allows the number of scanlines to be doubled to 2048. Observe that all the periods are even multiples of two scanlines. If this bit is '0', the scanline counter is clocked with horizontal sync.

3.40 CR17: CRTC Mode Control Register *(cont.)*

Bit	Description
1	**Select Row-Scan Counter:** If this bit is '0', row-scan counter [1] is substituted for CRTC address counter [14]. This provides for Hercules™ compatibility. **NOTE:** The Cirrus Logic BIOS does *not* support Hercules compatibility. If this bit is '1', the substitution described above does not occur.
0	**Compatibility Mode (CGA) Support:** If this bit is '0', row-scan counter [0] is substituted for CRTC address counter [14]. This provides for CGA compatibility. If this bit is '1', the substitution described above does not occur.

NOTE: '?' in the above register addresses is 'B' in Monochrome mode and 'D' in Color mode.

3.41 CR18: CRTC Line Compare Register

I/O Port Address: PCI	3?5h
Index	18h
Size (bits):	8
MMI/O Offset	60h
Access Type	Read/Write

Bit	Description
7:0	Line Compare [7:0]

The Line Compare field is used to specify where Screen A terminates and Screen B begins.

Bit	Description
7:0	**Line Compare [7:0]:** This field is used to specify where Screen A terminates and Screen B begins. This register contains the eight least-significant bits of this field. This is extended with one bit each in CR7 and CR9. The Line Compare field can be used to implement a vertically split screen. The top portion of the screen is called Screen A and can begin anywhere in display memory. Screen A can be panned and scrolled on a pixel basis. The bottom portion of the screen is called Screen B. Screen B always begins at location '0' in display memory and cannot be panned or scrolled. Refer to Figure 3-1 and Table 3-2 for a summary of CRTC Timing registers.

NOTE: '?' in the above register addresses is 'B' in Monochrome mode and 'D' in Color mode.

3.42 CR22: Graphics Data Latches Readback Register

I/O Port Address: PCI	3?5h
Index	22h
Size (bits):	8
MMI/O Offset	–
Access Type	Read only

Bit	Description
7:0	Graphics Data Latch n Readback [7:0]

This register address is used to read the four graphics controller data latches.

Bit	Description
7:0	**Graphics Data Latch n Readback [7:0]:** This read-only register can be used to read back one of the four graphics controller data latches. The latch is selected with GR4[1:0]. These latches are loaded whenever display memory is read by the CPU.

NOTE: '?' in the above register addresses is 'B' in Monochrome mode and 'D' in Color mode.

3.43 CR24: Attribute Controller Toggle Readback Register

I/O Port Address: PCI	3?5h
Index	24h
Size (bits):	8
MMI/O Offset	–
Access Type	Read only

Bit	Description
7	Attribute Controller Toggle
6:0	Reserved

This read-only register provides access to the Attribute Controller Toggle.

Bit	Description
7	**Attribute Controller Toggle:** If this bit is '1', the attribute controller reads or writes a data value on the next access. If this bit is '0', the attribute controller reads or writes an index value on the next access.
6:0	**Reserved**

NOTE: '?' in the above register addresses is 'B' in Monochrome mode and 'D' in Color mode.

3.44 CR26: Attribute Controller Index Readback Register

I/O Port Address: PCI	3?5h
Index	26h
Size (bits):	8
MMI/O Offset	–
Access Type	Read only

Bit	Description
7	Reserved
6	Reserved
5	Video Enable
4:0	Attribute Controller Index [4:0]

This read-only register provides access to the current Attribute Controller Index.

Bit	Description
7:6	**Reserved**
5	**Video Enable:** This bit follows the Video Enable bit in the Attribute Controller Index register (it is a read-only copy of ARX[5]).
4:0	**Attribute Controller Index [4:0]:** This field follows the index in the Attribute Controller Index register (it is a read-only copy of ARX[4:0]).

NOTE: '?' in the above register addresses is 'B' in Monochrome mode and 'D' in Color mode.

3.45 GRX: Graphics Controller Index Register

I/O Port Address: PCI	3CEh
Index	–
Size (bits):	8
MMI/O Offset	–
Access Type	Read/Write

Bit	Description
7:6	Reserved
5:0	Graphics Controller Index [5:0]

This register is used to specify the register in the VGA Graphics Controller group, or the Extension register that is accessed by the next I/O read or I/O write to address 3CFh. Registers with an index value greater than eight are described in Chapter 4, “Extended I/O Registers”.

Bit	Description
7:6	**Reserved**
5:0	**Graphics Controller Index [5:0]:** This field specifies the register in the VGA graphics controller, or in the Extension register that is accessed by the next I/O read or I/O write to address 3CFh.

3.46 GR0: Graphics Controller Set/Reset Register

I/O Port Address: PCI	3CFh
Index	00h
Size (bits):	8
MMI/O Offset	–
Access Type	Read/Write

Bit	Description
7:4	Reserved
3:0	Set/Reset Plane [3:0]

This register specifies the values to be written into the respective display memory planes when the processor executes a Write mode 0 or Write mode 3 operation.

Bit	Description
7:4	**Reserved**
3:0	**Set/Reset Plane [3:0]:** These bits control the values written into the respective display memory planes for Write mode 0 and 3. Refer to the description of GR5 on page 3-60 for an overview of the Write modes.

3.47 GR1: Graphics Controller Set/Reset Enable Register

I/O Port Address: PCI	3CFh
Index	01h
Size (bits):	8
MMI/O Offset	–
Access Type	Read/Write

Bit	Description
7:4	Reserved
3:0	Enable Set/Reset Plane [3:0]

This register is used with GR0 to determine the values to be written into the respective display memory planes when Write mode 0 is selected.

Bit	Description
7:4	**Reserved**
3:0	**Enable Set/Reset Plane [3:0]:** These bits are used with GR0 to determine the values written into the display memory planes when Write mode 0 is selected. If a bit in this field is ‘1’, the corresponding value in GR0 is written into the corresponding display memory plane. If a bit in this field is ‘0’, the corresponding value from the CPU data bus is written into the corresponding display memory plane. Refer to the description of GR5 on page 3-60 for an overview of the Write modes.

3.48 GR2: Graphics Controller Color Compare Register

I/O Port Address: PCI	3CFh
Index	02h
Size (bits):	8
MMI/O Offset	–
Access Type	Read/Write

Bit	Description
7:4	Reserved
3:0	Color Compare Plane [3:0]

This register specifies the Color Compare Value for Read mode 1.

Bit	Description
7:4	**Reserved**
3:0	**Color Compare Plane [3:0]:** These four bits are compared with each of eight bits from the corresponding display memory planes under the mask in GR7 when a Read mode 1 occurs. Refer to the description of GR5 on page 3-60 for an overview of the Read modes.

3.49 GR3: Graphics Controller Data Rotate Register

I/O Port Address: PCI	3CFh
Index	03h
Size (bits):	8
MMI/O Offset	–
Access Type	Read/Write

Bit	Description
7:5	Reserved
4:3	Function Select [1:0]
2:0	Rotate Count [2:0]

This register contains two fields that are used with Write modes 0 and 3.

Bit 7:5 — Reserved

Bit 4:3 — Function Select [1:0]: This field controls the operation that occurs between the data in the latches and the data from the CPU or Set/Reset logic. The result of this operation is written into display memory. This field is used for Write mode 0 only. The operations are summarized in the following table:

GR3[4]	GR3[3]	Operation
0	0	None (the data in the latches are ignored)
0	1	Logical AND
1	0	Logical OR
1	1	Logical XOR

Bit 2:0 — Rotate Count [2:0]: This field allows data from the CPU bus to be rotated as many as seven-bit positions prior to being altered by the Set/Reset logic. Refer to the description of GR5 on page 3-60 for an overview of the Write modes.

3.50 GR4: Graphics Controller Read Map Select Register

I/O Port Address: PCI	3CFh
Index	04h
Size (bits):	8
MMI/O Offset	–
Access Type	Read/Write

Bit	Description
7:2	Reserved
1:0	Plane Select [1:0]

This register is used to specify the display memory plane for Read mode 0.

Bit	Description
7:2	**Reserved**
1:0	**Plane Select [1:0]:** This field specifies the display memory plane for Read mode 0. The values are shown in the following table:

GR4[1]	GR4[0]	Plane Selected
0	0	0
0	1	1
1	0	2
1	1	3

3.51 GR5: Graphics Controller Mode Register

I/O Port Address: PCI	3CFh
Index	05h
Size (bits):	8
MMI/O Offset	–
Access Type	Read/Write

Bit	Description
7	Reserved
6	256-Color Mode
5	Shift Register Mode
4	Odd/Even
3	Read Mode
2	Reserved
1:0	Write Mode [1:0]

This register specifies the Read and Write modes. In addition, it controls the configuration of the Data Shift registers.

Bit	Description
7	**Reserved**
6	**256-Color Mode:** If this bit is ‘1’, the Video Shift registers are configured for 256-Color Video modes. GR5[5] is ignored. If this bit is ‘0’, the Video Shift registers are configured for 16-, 4-, or 2-color modes.
5	**Shift Register Mode:** If this bit is ‘1’, the Video Shift registers are configured for CGA compatibility. This is used for Video modes 4 and 5. If this bit is ‘0’, the Video Shift registers are configured for EGA compatibility.
4	**Odd/Even:** If this bit is ‘1’, the graphics controller is configured for Odd/Even Addressing mode. This bit should always be the opposite value as SR4[2].
3	**Read Mode:** This bit specifies whether the device is in Read mode 0 or 1. **Read Mode 0:** If this bit is ‘0’, the CPU reads data directly from display memory. Each read returns eight adjacent bits of the display memory plane specified in GR4[1:0]. The color-match logic is not used in Read mode 0. Note that an I/O read of CR22 forces a Read mode 0 for that operation. **Read Mode 1:** If this bit is ‘1’, the CPU reads the results of the color compare logic. Read mode 1 allows eight adjacent pixels (in 16-color modes) to be compared to a specified color value in a single operation. Each of the eight bits returned to the processor indicates the result of a compare between the four bits of the Color Compare (GR2[3:0]) and the bits from the four display memory planes. If the four bits of the Color Compare match the four bits from the display memory planes, ‘1’ is returned for the corresponding bit position. If any bits in the Color Don’t Care (GR7[3:0]) are zeroes, the corresponding plane comparison is forced to match.
2	**Reserved**

3.51 GR5: Graphics Controller Mode Register *(cont.)*

Bit	Description
1:0	**Write Mode [1:0]:** These two bits specify the Write mode. **Write Mode 0:** Each of the four display memory planes is written with the CPU data rotated by the number of counts in GR3[2:0]. If a bit in GR1[3:0] is '1', the corresponding plane is written with the contents of the corresponding bit in GR0[3:0]. If SR7[0] is '1', CPU data is written regardless of the contents of GR1[3:0]. The contents of the data latches can be combined with the data from the SR logic under control of GR3[4:3]. Bit planes are enabled with SR2[3:0]. Bit positions are enabled with GR8. **Write Mode 1:** Each of the four display memory planes is written with the data in the data latches. The data latches must have been previously loaded from display memory with a previous read. GR8 is ignored in Write mode 1. **Write Mode 2:** Display memory planes 3:0 are written with the values of Data bits 3:0, respectively. The four bits are replicated eight times each to write up to eight adjacent pixels. Bit planes are enabled with SR2[3:0]. Bit positions are enabled with GR8. The Data Rotator, SR logic, and Function Select fields are ignored in Write mode 2. **Write Mode 3:** The data for each display memory plane comes from the corresponding bit of GR0[3:0]. The Bit Position Enable field is formed with the logical AND of GR8 and the rotated CPU data. The Set/Reset and Function Select fields are ignored in Write mode 3.

3.52 GR6: Graphics Controller Miscellaneous Register

I/O Port Address: PCI	3CFh
Index	06h
Size (bits):	8
MMI/O Offset	–
Access Type	Read/Write

Bit	Description
7:4	Reserved
3:2	Memory Map [1:0]
1	Chain Odd Maps to Even
0	Graphics Mode

This register contains miscellaneous control bits.

Bit 7:4 — Reserved

Bit 3:2 — Memory Map [1:0]: This field specifies the beginning address and size of the display memory in the host address space. This is summarized in the following table:

GR6[3]	GR6[2]	Memory Map	Beginning Address	Length	Mode(s)
0	0	0	A000:0	128K	Extended
0	1	1	A000:0	64K	EGA/VGA
1	0	2	B000:0	32K	Hercules™
1	1	3	B800:0	32K	CGA

Bit 1 — Chain Odd Maps to Even: When this bit is '1', CPU Address bit 0 is replaced with a most-significant address bit. This causes even host addresses to access planes 0 and 2, and odd host addresses to access planes 1 and 3. This mode is useful for MDA emulation.

Bit 0 — Graphics Mode: If this bit is '1', the CL-GD546X functions in VGA Graphics (APA) modes. If it is '0', the device functions in VGA Text (AN) modes.

3.53 GR7: Graphics Controller Color Don't Care Register

I/O Port Address: PCI	3CFh
Index	07h
Size (bits):	8
MMI/O Offset	–
Access Type	Read/Write

Bit	Description
7:4	Reserved
3:0	Color Don't Care Plane [3:0]

This register is used with GR2 for Read mode 1 accesses.

Bit	Description
7:4	**Reserved**
3:0	**Color Don't Care Plane [3:0]:** These four bits are used to control whether the four planes are involved in color compares. If a bit is '1', the corresponding plane is involved; if a bit is '0', the corresponding plane is not involved. Refer to the description of GR5 on page 3-60 for an overview of the Read modes.

3.54 GR8: Graphics Controller Bit Mask Register

I/O Port Address: PCI	3CFh
Index	08h
Size (bits):	8
MMI/O Offset	–
Access Type	Read/Write

Bit	Description
7:0	Write Enable [7:0]

This register controls writes to display memory on a bit basis in Write modes 0, 2, and 3.

Bit	Description
7:0	**Write Enable [7:0]:** Each bit in this register controls whether the corresponding bit in display memory is written in Write modes 0, 2, and 3. If a bit is ‘1’, the corresponding bit in display memory is written. If a bit is ‘0’, the corresponding bit in display memory is not written. This write protection is orthogonal to that provided by SR2.

3.55 ARX: Attribute Controller Index Register

I/O Port Address: PCI	3C0h/3C1h
Index	–
Size (bits):	8
MMI/O Offset	7Ch
Access Type	Read/Write

Bit	Description
7:6	Reserved
5	Video Enable
4:0	Attribute Controller Index [4:0]

This register specifies the register in the Attribute Controller block that is accessed with the next I/O read or I/O write to 3C1h or 3C0h, respectively. Observe that the same port addresses are used for the index and data for the Attribute Controller block, unlike the other blocks for which the Index and Data registers are at different addresses. Alternate writes toggle between index and data. It is possible to read the toggle at CR24 and the index value at CR26. This register is also accessible at MMI/O offset 7Ch.

Bit	Description
7:6	**Reserved**
5	**Video Enable:** When this bit is ‘0’, the screen displays the color indicated by the Overscan Color register (AR11 on page 3-69). When this bit is ‘1’, normal video is displayed.
4:0	**Attribute Controller Index [4:0]:** This field is the index into the Data registers in the Attribute Controller block.

3.56 AR0-ARF: Attribute Controller Palette Registers

I/O Port Address: PCI	3C0h/3C1h
Index	00h–0Fh
Size (bits):	8
MMI/O Offset	–
Access Type	Read/Write

Bit	Description
7:6	Reserved
5	Secondary Red
4	Secondary Green/Intensity
3	Secondary Blue/Monochrome
2	Red
1	Green
0	Blue

In 16-Color Text and Graphics modes, these digital palette entries are selected by the four bits of pixel data, and point to the VGA palette entries. The VGA palette entries are normally programmed so that the DAC outputs reflect these values. That is, the VGA palette simulates standard EGA colors.

Bit	Description
7:6	**Reserved**
5:0	**Palette Entries**

3.57 AR10: Attribute Controller Mode Register

I/O Port Address: PCI	3C0h/3C1h
Index	10h
Size (bits):	8
MMI/O Offset	–
Access Type	Read/Write

Bit	Description
7	AR14 Video Source Enable
6	Pixel Double Clock Select
5	Pixel Panning Compatibility
4	Reserved
3	Blink Enable
2	Line Graphics Enable
1	Display Type
0	Graphics Mode

This register contains some miscellaneous control bits for the attribute controller.

Bit	Description
7	**AR14 Video Source Enable:** If this bit is '1', AR14[1:0] are used as the source for the Lookup Table Address bits [5:4]. This allows the rapid selection of four 16-color palettes. This bit is ignored for deeper color modes. If this bit is '0', the Palette registers AR0-F[5:4] are used as the source for the Lookup Table Address bits [5:4].
6	**Pixel Double Clock Select:** If this bit is '1', pixels are clocked on every other clock cycle and AR0–F is bypassed. This is used with mode 13. The sequencer logic operates at twice the pixel rate. If this bit is '0', pixels are clocked on every cycle.
5	**Pixel Panning Compatibility:** If this bit is '1', a line compare match in the CRTC forces the output of the Pixel Panning register to '0' until the next VSYNC occurs. This allows the panning of Screen A without Screen B. If this bit is '0', the two parts of a split screen pan together.
4	**Reserved**
3	**Blink Enable:** If this bit is '1', character blinking is enabled at the vertical refresh frequency divided by 32. If this bit is '0', character blinking is disabled.
2	**Line Graphics Enable:** If this bit is '1', the ninth bit of a nine-bit-wide character cell is made the same as the eighth bit for character codes in the range C0 through DF. If this bit is '0', the ninth bit of a nine-bit-wide character cell is the same as the background.

3.57 AR10: Attribute Controller Mode Register *(cont.)*

Bit **Description**

1 **Display Type:** This bit is useful only if the CL-GD546X is in AN (Alphanumeric) modes. If this bit is '1', the contents of the Attribute byte are treated as MDA-compatible attributes. The following table shows examples of monochrome attributes:

Blink Bit 7	Background Bit [6:4]	Intensity Bit 3	Foreground Bit [2:0]	Hex Code	Attribute
0	0	0	7	07	Normal
0	0	1	7	0F	Intense
0	0	0	1	01	Underline
0	0	1	1	09	Underline intense
0	7	0	0	70	Reverse
1	7	0	0	F0	Blinking reverse

If this bit is '0', the contents of the Attribute byte are treated as color attributes.

0 **Graphics Mode:** If this bit is '1', the attribute controller functions in APA (Graphics) mode. If this bit is '0', the attribute controller functions in AN modes.

3.58 AR11: Overscan (Border) Color Register

I/O Port Address: PCI	3C0h/3C1h
Index	11h
Size (bits):	8
MMI/O Offset	–
Access Type	Read/Write

Bit	Description
7:6	Reserved
5	Secondary Red
4	Secondary Green
3	Secondary Blue
2	Red
1	Green
0	Blue

This register points to the entry in the LUT that defines the border color. Typically, the LUT entries are programmed so that the color defined above is the color that actually results. The border is defined as that portion of the raster between blanking and active video, on all four sides. Refer to Figure 3-1 on page 3-23.

Bit	Description
7:6	**Reserved**
5:0	**Border Color [5:0]:** Either four or six of these bits are used to select the LUT entry for the border color in CGA and EGA modes.

3.59 AR12: Color Plane Enable Register

I/O Port Address: PCI	3C0h/3C1h
Index	12h
Size (bits):	8
MMI/O Offset	–
Access Type	Read/Write

Bit	Description
7:6	Reserved
5:4	Video Status Mux [1:0]
3:0	Enable Plane [3:0]

This register contains a field to enable the four planes into the Attribute Controller Palette registers. It also contains a field to select the inputs for the Diagnostic bits in STAT[5:4].

Bit **Description**

7:6 **Reserved**

5:4 **Video Status Mux [1:0]:** This field selects the inputs for the Diagnostic bits in STAT[5:4] as indicated in the following table:

AR12[5]	AR12[4]	STAT[5]	STAT[4]
0	0	P[2]	P[0]
0	1	P[5]	P[4]
1	0	P[3]	P[1]
1	1	P[7]	P[6]

3:0 **Enable Color Plane [3:0]:** If any bit in this field is ‘1’, the data from the corresponding display memory plane is enabled in choosing the Attribute Controller Palette register. If any bit in this field is ‘0’, the data from the corresponding display memory plane is forced to ‘0’ in choosing the Attribute Controller Palette register.

3.60 AR13: Pixel Panning Register

I/O Port Address: PCI	3C0h/3C1h
Index	13h
Size (bits):	8
MMI/O Offset	–
Access Type	Read/Write

Bit	Description
7:4	Reserved
3:0	Pixel Panning [3:0]

This register specifies the number of pixels the display data shifts to the left. This field functions both in the APA (Graphics) and AN (Alphanumeric) modes.

Bit	Description
7:4	**Reserved**
3:0	**Pixel Panning [3:0]:** This field specifies the number of pixels the display data shifts to the left. This field is interpreted as indicated in the following table:

AR13[3:0]	9-bit Characters	8-bit Characters	Mode 13
0	1 bit left	(none)	(none)
1	2 bits left	1 bit left	(none)
2	3 bits left	2 bits left	1 bit left
3	4 bits left	3 bits left	1 bit left
4	5 bits left	4 bits left	2 bits left
5	6 bits left	5 bits left	2 bits left
6	7 bits left	6 bits left	3 bits left
7	8 bits left	7 bits left	3 bits left
8-F	no shift	1 bit right	3 bits left

3.61 AR14: Color Select Register

I/O Port Address: PCI	3C0h/3C1h
Index	14h
Size (bits):	8
MMI/O Offset	–
Access Type	Read/Write

Bit	Description
7:4	Reserved
3:0	Color Bit C [7:4]

This register contains two fields that are involved in the selection of addresses into the LUT.

Bit	Description
7:4	**Reserved**
3:2	**Color Bit C [7:6]:** These two bits are concatenated with the six bits from the Attribute Controller Palette register to form the address into the LUT and drive P[7:6]. These bit are ignored in 8-, 16-, and 24-bit Pixel modes.
1:0	**Color Bits C [5:4]:** If AR10[7] is '1', these two bits replace the corresponding two bits from the Attribute Controller Palette register to form the address into the LUT and drive P[5:4]. If AR10[7] is '0', these two bits are ignored. These bits are ignored in 8-, 16-, and 24-bit Pixel modes.

