Appendix B3

Configuration Notes

CONFIGURATION NOTES

1. INTRODUCTION

When RST# is not active (the positive edge), the CL-GD546X loads the levels on a number of pins into internal latches. These latches control fundamental properties of the device, such as the BIOS size.

2. CONFIGURATION SUMMARY

The pins used for configuration have an internal pull-up resistor (nominally 250 kΩ). The default (if no pull-down resistor is installed) is '1'. If '0' is to be loaded into the latch, an external pull-down resistor (typically 6.8 kΩ) must be installed. Table B3-1 provides an overview of the Configuration bits.

Table B3-1. CL-GD546X Configuration Bits

CL-GD5462		CL-GD5464		Level		Description	Note
Pin Name	Pin No.	Pin Name	Pin No.	CL-GD5462	CL-GD5464		
P21	125	RA7	107		0	Pin Scan mode	
					1	Normal mode	
P18	128	RA3	102		0	Disable VGA operation	
					1	Enable VGA operations	
P20	124	RA2	101		0	RCLK drives VCLK	Factory test only
					1	Normal operation	
ROMCS#	62	ROMCS#	62		0	Motherboard mode	
					1	Add-On Card mode	
RA3	102	RA1	100		0	Bypass mode	Factory test only
					1	Normal mode	
RA[5:4]	104, 103	RA[6:4]	106, 104, 103	00	000	C-CUBE CL480	VMI 'A'
					010	16-bit Intel® I/O port	
				01	011	No GPIO	VMI 'B'
					100	8-bit Intel® I/O port	
					001	CL-GD5464 only	VMI 'B'
				10, 11	101–111	Reserved	
n/a	n/a	RA8	108		0	Test mode	Factory test only
					1	Normal mode	
INTA#	205	INTA#	205		0	No interrupt claimed	
					1	Interrupt claimed	

3. CONFIGURATION DETAILS

BIOS SIZE (PCI Configuration): If a pull-down resistor is installed on RA15, the BIOS extent for PCI configuration is 32 Kbytes. If no pull-down resistor is installed on RA15, the BIOS extent for PCI configuration is 64 Kbytes.

Pin-Scan Mode: If a pull-down resistor is installed on P21/RA7 (or more likely, the pin is driven low by a tester), the CL-GD546X enters Pin-Scan mode. See Appendix B5, "Pin Scan", for a detailed description. If no pull-down resistor is installed on P21/RA7, the CL-GD546X operates normally.

VGA Operation: If a pull-down resistor is installed on P18/RA3, VGA operation is disabled. The PCI subclass field returns the value 80h and no VGA registers are visible. If no pull-down is installed on P18/RA3, VGA operation is enabled. The PCI subclass field returns the value 00h and the VGA registers are visible.

Clock-Test Mode: If a pull-down resistor is installed on P20/RA2, RCLK drives the internal VCLK. This is for factory testing only. If no pull-down resistor is installed on P20/RA2, the CL-GD546X operates normally.

Motherboard/Add-in: If a pull-down resistor is installed on ROMCS# or if ROMCS# is tied to ground, the CL-GD546X is configured for motherboard operation. The ROM BIOS decode is disabled. In most configuration bits, the pin cannot be tied directly to ground. ROMCS# is an exception in this respect. Since ROMCS# is in the middle of Rambus channel 'A', it is more convenient to connect it to ground than to route a connection from a resistor. Since it is not used, a connection to hard ground is acceptable. This is the only configuration bit that can be treated in this manner.

If no pull-down resistor is installed on ROMCS# and ROMCS# is not tied to ground, the CL-GD546X is configured for add-in card operation. The ROM BIOS decode is enabled.

Bypass Mode: If a pull-down resistor is installed on RA3/RA1, the CL-GD546X powers up in Bypass mode. This mode is used for low-speed testing on a tester (factory testing only). If no pull-down resistor is installed, the CL-GD546X operates normally.

General-Purpose I/O Port Configuration: To configure the general-purpose I/O port**,** pull-down resistors can be installed on RA[5:4]. This is summarized in Table B3-2. See Appendix B7, "General-Purpose I/O Port", for more details.

Table B3-2. Local Peripheral Bus Configuration

V-Port™ Mode	GPIO 2:0 Configuration	
	CL-GD5462 RA[5:4]	CL-GD5464 RA[6:4]
C-CUBE CL480 (VMI mode 'A')	00	000
Reserved	01	001, 101–111
16-bit Intel® configuration	10	010
GPIO disabled	11	011
8-bit Intel® configuration (VMI mode 'B')	n/a	100

Host Bus: If no pull-down resistor is installed on P19/RA0, the CL-GD546X is configured for the PCI bus. Do not install a pull-down resistor on P19/RA0.

NOTE: The VESA VL-Bus is not supported on the CL-GD546X.

Test Mode: If a pull-down resistor is installed on RA8, the CL-GD5464 is configured for factory test mode. Do not install a pull-down resistor on RA8.

INTA#: If a pull-down resistor is installed on the INTA# pin, no PCI interrupt pin is claimed. The output driver is disabled. If no pull-down resistor is installed on the INTA# pin, the interrupt is claimed.

