Rambus® Registers

7. RAMBUS® REGISTERS

The Rambus registers in the CL-GD546X are summarized in Table 7-1. These registers are only accessible with memory-mapped I/O (that is, in the address space defined in PCI10).

Table 7-1. Rambus® Registers Quick Reference

Register Name	MMI/O Offset	Size (Bits)	Page
RIF Control	200h	16	7-3
RAC Control	202h	16	7-5
Rambus Transaction	204h	16	7-7
Rambus Data	240h	32	7-8

7.1 RIF Control Register

Size (bits):	16
MMI/O Offset	200h
Access Type	Read/Write

Bit	Description	Reset State
15:14	RAMBUS_ACK [1:0]	X
13	READ_HIT [1]	0
12	READ_HIT [0]	1
11	STOP_REFRESH	0
10	CLEAN_MISS [2]	0
9	CLEAN_MISS [1]	1
8	CLEAN_MISS [0]	0
7	SOUT	X
6	DIRTY_MISS [2]	1
5	DIRTY_MISS [1]	0
4	DIRTY_MISS [0]	0
3	INIT	0
2:0	N_BANKS [2:0]	1

This register controls the operation of the RIF (Rambus interface). No application program should ever write to this register.

Bit	Description
15:14	**RAMBUS_ACK [1:0]:** These two bits return the two-bit acknowledge packet during the last Rambus transaction. Usually, this is used only during initialization to determine when the last RDRAM was initialized. As long as the RDRAM AckDelay is not modified from its default value, this field is valid.
13:12	**READ_HIT [1:0]:** This two-bit field specifies the number of CLK cycles between accepting a request packet from the requester (ACK is '1'), and returning read data (RDY is '1'). The value programmed is four less than the actual number of cycles. The reset state is '01b', which implies five cycles.
11	**STOP_REFRESH:** When this bit is set to '1', DRAM refresh cycles are not performed.
10:8	**CLEAN_MISS [2:0]:** This three-bit field specifies the number of CLK cycles to retry access for a clean miss. The value programmed is four less than the actual number of cycles. The reset state is '010b', which implies six cycles.
7	**SOUT:** This bit controls the SOUT pin. This pin is used to initialize the RDRAMs.
6:4	**DIRTY_MISS [2:0]:** This three-bit field specifies the number of CLK cycles to retry access for a dirty miss. The value programmed is four less than the actual number of cycles. The reset state is '100', which implies eight cycles.

7.1 RIF Control Register *(cont.)*

Bit	Description
3	**INIT:** When this bit is '0' (the reset state), it is a signal to the RIF that the RDRAM timing parameters are not initialized. It also signals that the default RDRAM timing parameters need to be used. Only RReg, WReg, and WREGB cycles are supported prior to RDRAM initialization. This bit is programmed to '1' after the RDRAM initialization.
2:0	**N_BANKS [2:0]:** This three-bit field is programmed with the number of RDRAM banks. This determines the number of RDRAMs that must be refreshed with each refresh cycle.

7.2 RAC Control Register

Size (bits):	16
MMI/O Offset	202h
Access Type	Read/Write

Bit	Description	Reset State
15	STOP_EN	1
14	EXTBE	1
13	RAC_RESET	0
12	RESERVED	1
11	PH_STALL	X
10	IOST	0
9	BIST	0
8	BIST_FLAG	R/O
7	CCTL_EN	1
6	CCTL_LD	0
5:0	CCTL [5:0]	X

This register controls the operation of the RAC (Rambus ASIC cell). No application program should ever write to this register.

Bit	Description
15	**STOP_EN:** If this bit is ‘1’, the transmit and receive clocks are stopped when not needed. This is a power saving feature. This is also the reset state. If this bit is ‘0’, the clocks run continuously. Program this bit to ‘0’ to perform the built-in self test.
14	**EXTBE:** This bit controls the RAC ExtBE (external bus enable) port. See the RDRAM reference manual for details.
13	**RAC_RESET:** If this bit is ‘1’, the RAC is reset. This bit must be set prior to enabling BIST, extended BIST, or IOST modes. RAC_RESET does not reset the RAC Control registers.
12	**Reserved**
11	**PH_STALL:** When this bit is programmed from ‘0’ to ‘1’ (when a rising edge occurs), the phase of SYNCLK is delayed by one BUSCLK.
10	**IOST:** I/O self test is for device test only.
9	**BIST:** Built-in self test is for device test only.
8	**BIST_FLAG:** This read-only bit returns the result of the built-in self test. The value ‘1’ indicates pass; the value ‘0’ indicates failure.
7	**CCTL_EN:** When this bit is ‘1’, the current auto-calibration circuit in the RAC is enabled. This is the normal reset state. When this bit is ‘0’, the value from CCTL[5:0] is used. This bit is intended for device test only.

7.2 RAC Control Register *(cont.)*

Bit	Description
6	**CCTL_LD:** When this bit is '1', a new current control value is loaded into the RAC output drivers. This value comes from the auto-calibration circuit or the CCTL[5:0] field, depending on the state of CCTL_EN. Normally, CCTL is automatically loaded by the RIF during refresh cycles; this bit provides a manual method. Do not set CCTL_LD to '1' when the RAC is transmitting anything on the Rambus channel.
5:0	**CCTL [5:0]:** This value controls the current level on all high-speed Rambus drivers (RAD[8:0], RAC, and RAE) if CCTL_EN is programmed to '0'. Normally CCTL_EN is programmed to '1' and this value is ignored.

7.3 Rambus® Transaction Register

Size (bits):	16
MMI/O Offset	204h
Access Type	Read/Write

Bit	Description
15	Broadcast
14:12	Reserved
11:8	DEV_ADDR [23:20]
7:4	Reserved
3:0	REG_ADR [5:2]

This register specifies the RDRAM and the register to be read or written. In addition, a broadcast register write can be selected.

Bit	Description
15	**Broadcast:** If this bit is '1', a broadcast write transaction is requested.
14:12	**Reserved**
11:8	**DEV_ADDR [23:20]:** This four-bit field specifies the device for the transaction. This field corresponds to Rambus address [23:20].
7:4	**Reserved**
3:0	**REG_ADR [5:2]:** This four-bit field specifies the RDRAM register address for the transaction. This field corresponds to Rambus address [5:2].

7.4 Rambus® Data Register

Size (bits):	32
MMI/O Offset	240h
Access Type	Read/Write

Bit	Description
31	Rambus Data [31:0]

A write or a read to this register triggers a Rambus register read or write. Write data actually goes to the write FIFO or read data latches, the same as it would for a memory read or write.

Bit	Description
31:0	**Rambus Data [31:0]:** This value is the actual Rambus register contents.

