6. ELECTRICAL SPECIFICATIONS

6.1 Absolute Maximum Ratings

Ambient temperature under bias .....0°C to 70°C
Storage temperature .....–65°C to 150°C
Voltage on any pin .....GND – 0.5 V to V_{DD} + 0.5 V (volt)
Voltage on 5-V tolerant pin ..... GND – 0.5 V to 5.5 V
Operating power dissipation ..... 2.0 W (watt)
Power supply voltage ..... 5.0 V
Injection current (latch-up testing) ..... 100 mA

CAUTION: Stresses above those listed may cause permanent damage to system components. These are stress ratings only. Functional operation at these or any conditions above those indicated in the operational ratings of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect system reliability.

6.2 DC Specifications

(V_{DD} = 3.3 V ± 0.15 V, T_A = 0°C to 70°C, unless otherwise specified)

Symbol	Parameter	MIN	MAX	Units	Test Conditions	Note
V_{DD} (+3.3 V)	Power supply voltage	3.15	3.45	V	Normal operation	
V_{IL}	Input low voltage	–0.5	0.3 V_{DD}	V	(non 5-V tolerant)	
V_{IH}	Input high voltage	0.7 V_{DD}	1.05 V_{DD}	V	(non 5-V tolerant)	
V_{IH5T}	Input high voltage	0.7 V_{DD}	5.5V	V	(5-V tolerant)	1
V_{OL}	Output low voltage	–	0.1 V_{DD}	V	I_{OL} = 3.2 mA	2
V_{OH}	Output high voltage	0.9 V_{DD}	–	V	I_{OH} = –200 µA	3
I_{DD} (+3.3 V)	Supply current	–	–	–	V_{DD} nominal	4
I_{IH}	Input high current	–	10	µA	V_{IL} = V_{DD}	
I_{IL}	Input low current	–10	–	µA	V_{DD} = 3.45, V_{IL} = 0	
I_{IHP}	Input high current (pull-up)	–	–10	µA	V_{IL} = V_{DD}	
I_{ILP}	Input low current (pull-up)	–45	–12	µA	V_{DD} = 3.45, V_{IL} = 0	
I_{OZ}	Input leakage	–10	10	µA	0 < V_{IN} < V_{CC}	
C_{IN}	Input capacitance	–	10	pF		5
C_{OUT}	Output capacitance	–	10	pF		5

NOTES:

1) 5-V tolerant pins — all except Rambus access channel, SOUT, and ROMCS#.
2) I_{OL} is specified for a standard buffer. See Section 1.2 for further information.
3) I_{OH} is specified for a standard buffer. See Section 1.2 for further information.
4) I_{DD} is measured with PCLK and BCLK as indicated below:

Device	PCLK	BCLK	I_{DD} (+3.3 V)
CL-GD5462	170 MHz	300 MHz	750 mA
CL-GD5464	230 MHz	300 MHz	tbd

5) This is not 100% tested, but is periodically sampled.
6) 'tbd' indicates to be determined.

6.3 DAC Characteristics

(V_{CC} = 3.3 V ± 0.15 V, T_A = 0°C to 70°C, unless otherwise specified)

Symbol	Parameter		MAX	Units	Test Conditions	Note
R	Resolution		8	Bits		
IO	Output current		30	mA	VO < 1 V	
TR	Analog output rise/fall time		3	ns		1, 2, 3
TS	Analog output settling time		15	ns		1, 2, 4
TSK	Analog output skew		tbd	ns		1, 2, 5
FDT	DAC-to-DAC correlation		2.5	%		5, 6
GI	Glitch impulse	Typical	tbd	pV – sec.		1, 2, 5
IL	Integral linearity		1.5	LSB		
DL	Differential linearity		1.5	LSB		1

NOTES:

1) Load is 37.5 Ω and 30 pF per analog output.
2) 130-Ω resistor to DACVSS on VREF pin.
3) TR is measured from 10% to 90% full-scale.
4) TS is measured from 50% of full-scale transition to output remaining within 2% of final value.
5) Outputs loaded identically.
6) About the mid-point of the distribution of the three DACs measured at full-scale output.
7) ‘tbd’ indicates to be determined.