Appendix B1

Layout Guidelines

LAYOUT GUIDELINES

1. INTRODUCTION

The CL-GD546X controllers are highly integrated, mixed-signal circuits with high operating frequencies. These devices are designed into graphics subsystems with very high bandwidth buses. To obtain a board that performs to expectations, the board design team should carefully follow these guidelines.

In addition to the host and enhanced V-Port interfaces, the CL-GD546X connects to one or two Rambus channels. This appendix includes detailed instructions that make the Rambus channel layout straight-forward and less error-prone than the standard DRAM memory interface.

The Cirrus Logic Desktop Applications Group has built a number of reference designs and have helped many customers solve performance and FCC problems.

2. REFERENCE DESIGNS

Complete reference designs for PCI bus adapter cards are available from Cirrus Logic. These designs have been rigorously tested in the laboratories of Cirrus Logic Desktop Applications Group and have FCC certification. Interested customers should contact their sales office representative.

3. PARTS PLACEMENT

The first consideration is parts placement. This section discusses the placement of the CL-GD546X and the peripheral logic onto PCI adapter cards.

3.1 PCI Bus Adapter Card

Figure B1-1 indicates how the components should be positioned on the PCI adapter card. The CL-GD546X device is placed very close to the PCI interface and approximately centered on the interface. The device is rotated so that pin 1 is at the bottom left corner, placing the PCI bus interface next to the connector.

Rambus Channel A is at the right-hand of the CL-GD546X, Rambus Channel B is at the left. The spacing between the CL-GD546X and the Rambus channels is fixed. Actually, the layout of the Rambus channels should be considered to be extensions of the CL-GD546X. The two sections are very closely integrated.

The VGA connector, reference oscillator, feature connector, and BIOS ROM are all in a line across the top of the board. This diagram does not show the discrete components on both sides of the board.

This reference design does not implement the general-purpose I/O port or the enhanced V-Port.

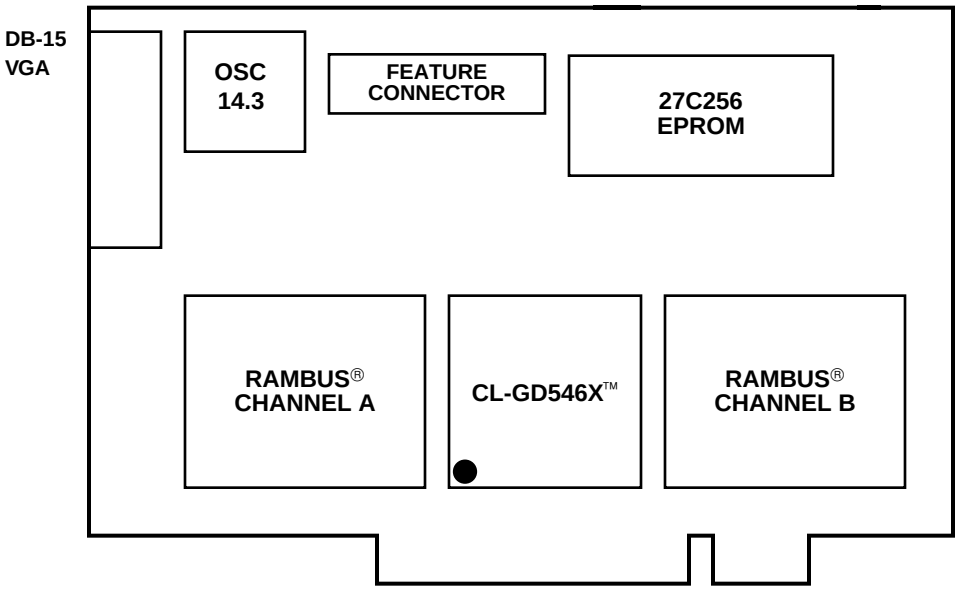

Figure B1-1. PCI Adapter Board Parts Placement

Questions regarding the PCI specification or membership in the PCI Special Interest Group can be forwarded to:

PCI Special Interest Group
M/S HF3-15A
5200 N.E. Elam Young Parkway
Hillsboro, OR, 97124-6497
(503) 696-2000

3.2 Motherboard

Parts placement is as important in a motherboard design as in an adapter card. The Cirrus Logic controller must simultaneously be close to the Rambus channel(s), the CPU, and the core logic. At the same time, these components must be well away from components on the motherboard that could induce noise, such as the main memory, keyboard controller and other peripherals, and the adapter slots.

4. POWER

Cirrus Logic recommends the use of multi-layer boards for its components, especially when designed into high-performance systems. As frequencies continue to get higher, it becomes less and less likely that acceptable results can be obtained with a two-layer board. One plane must be dedicated exclusively to the distribution of power, and one plane must be dedicated exclusively to ground.

Figure B1-2 shows how power is isolated for the CL-GD546X. The PCI reference is given as an example. This drawing is an artist's conception. The actual artwork should be used as a reference.

The 5-V rail is brought onto the board from the PCI bus. A section of the power plane around the periphery of the board is 5 V. This section powers the reference oscillator and the BIOS EPROM, and is shaded in the diagram.

A 3.3-V fixed voltage three-pin regulator reduces the 5-V rail to 3.3 V. The unshaded section of the power plane in the diagram is 3.3-V. Cirrus Logic recommends a local regulator rather than using 3.3 V off the PCI bus since this provides better control over the supply. Within the 3.3-V section, there are two cutouts that are completely isolated and powered by LC filters. These cutouts power RABVDD and DACVDD. Each power filter is made up of a ferrite bead plus 10-µF and 0.1-µF capacitors.

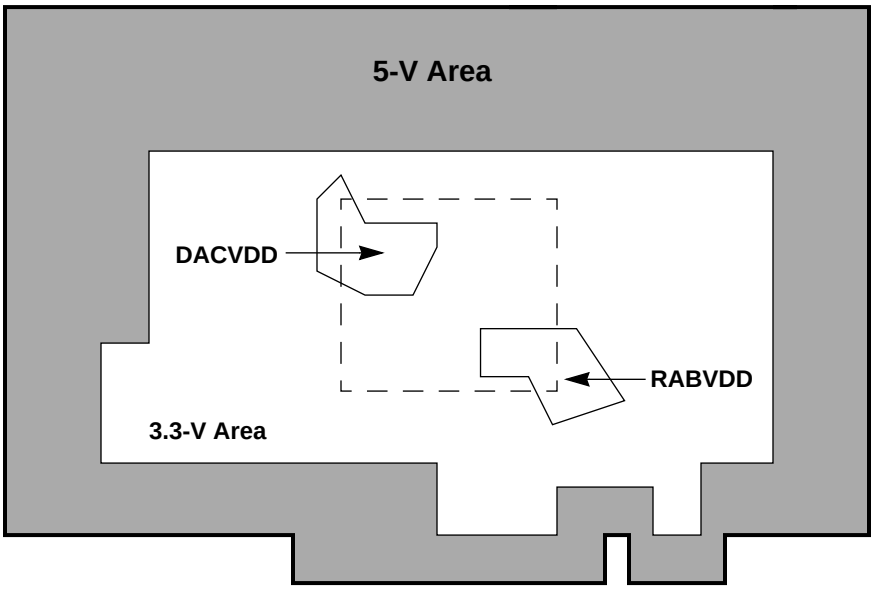

Figure B1-2. Power Isolation and Conditioning

5. GROUND

One plane on the board must be dedicated to ground. The ground must have cuts that suppress currents between the various areas (but that do not provide complete isolation). These cuts are shown in Figure B1-3 for the PCI reference design.

There is a certain amount of art involved in the exact positioning and size of the cuts in the ground and power planes. Some experimentation may be required to obtain satisfactory results.

The power and ground plane cuts must follow each other. It is critical that an isolated ground or power plane does not overlay a noisy digital power or ground plane. If such an overlay were allowed, the result would be a capacitor composed of the overlay conductors separated by the relatively thin dielectric between the two pieces of epoxy that make up a four-layer board. Noisy buses (such as data or address) must not be allowed to cross any isolated area.

The ground plane underneath the Rambus channel should not be cut or discontinued in any way. Also, the layer stacking should be so that the ground plane is under the component side.

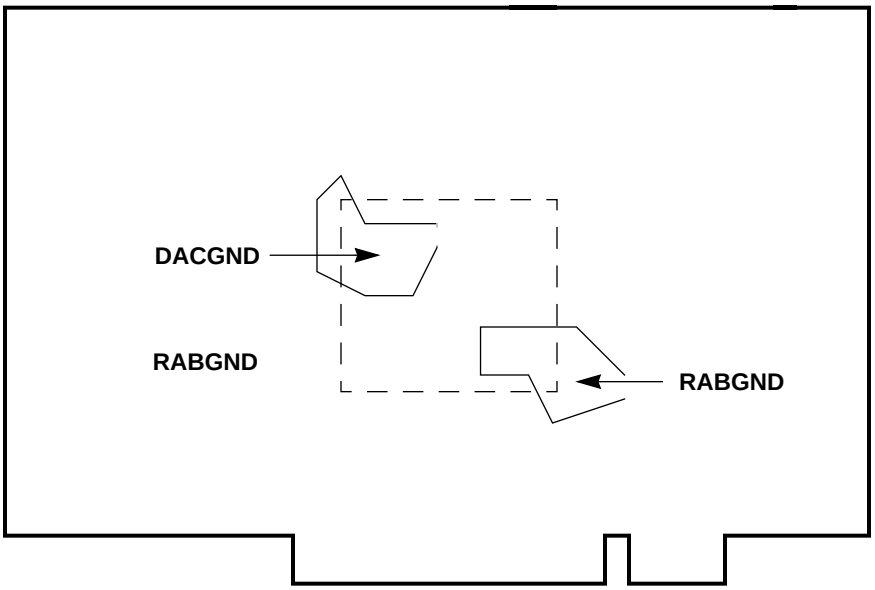

Figure B1-3. Ground Isolation

Designers with prior experience using discrete RAMDACs and clock sources may have found that such care with power distribution and isolation is not necessary, especially at relatively low frequencies. The integrated solution available from Cirrus Logic, operating at high frequencies has changed this, making these precautions necessary.

6. DECOUPLING CAPACITORS

The CL-GD546X operates at high frequencies (up to 300 MHz). Adequate power decoupling is absolutely crucial to a successful design. Each power pin on the device must have a 0.1-µF capacitor returned to the local ground. These capacitors must be placed as close to the respective power pins as possible. These capacitors must have excellent high-frequency characteristics; Cirrus Logic has found that the surface-mount ceramic chip capacitors perform adequately.

The Rambus channel has decoupling requirements that must be addressed carefully. These requirements are discussed in Section 8.

7. RGB LINES

The RGB traces are likely to be fairly long. The rise and fall times on these traces are on the order of 2–4 ns, causing them to behave as transmission lines. This means that the characteristic impedance must be controlled and must be close to the nominal monitor termination value of 75 Ω.

There must be π LC filters on each of the RGB lines, as shown in the reference designs. The recommended component values are 10 pF for the capacitors. The inductor is a ferrite bead, with 10–20 Ω impedance at 100 MHz.

There is a trade-off involved in the selection of these component values. Obtaining crisp video on the screen requires the rise and fall times to be as short as possible. However, to obtain acceptable emissions testing results, one would like relatively slow rise and fall times. As the pixel rates get higher and higher, there is less margin between these two conflicting requirements. The component values represent the best engineering judgement at the time of this publication. The filter components must be placed as closely as possible to the VGA DB15 connector.

8. RAMBUS® CHANNELS

The Rambus channel is designed taking into account the analog nature of a very high-frequency interconnection. The result is an electrical environment capable of supporting signals with edges every 1.9 ns that can be successfully fabricated using traditional PCB manufacturing technology. Issues such as, trace length, trace width, characteristic impedance, capacitive loading, and routing have been considered and specified.

The two Rambus channels are electrically identical. The layout for Rambus Channel B is made by rotating Channel A 180º and translating it to the left of the CL-GD546X device.

8.1 Physical Layout

Figure B1-4 is the presentation of the actual layout of the component side and solder side of the PCI reference design. The CL-GD546X is at the left end of the Rambus channel and the terminators are at the right end. The RSocket is adjacent to the CL-GD546X. The two RDRAMs are between the RSocket and the terminators. All active components (the CL-GD546X and the RDRAMs) are placed on the component side of the board. Some passive devices are placed on the solder side.

8.2 CL-GD546X Layout

As previously discussed, excellent power bypassing is important. The ceramic-chip capacitors are placed as close as possible to each power pin on the CL-GD546X and are connected with very short traces. The smallest standard case size (0805) was selected.

Excellent bypassing for RAVREF is important, especially since the reference voltage is generated at a significant distance from the CL-GD546X and the RDRAMs. A ceramic-chip capacitor is placed as close as possible to RAVREF.

The control current for the Rambus interface is generated with two parallel resistors tied between VTERM and CCTL. This control current determines the output current driven by the CL-GD546X, and this determines the voltage swing. The CCTL signal also goes to the RSocket. If the RSocket is plugged in, an additional resistor is used to lower the parallel resistance value, increasing the current drive of the CL-GD546X. This allows the system to automatically configure for more current drive when an expansion module is inserted.

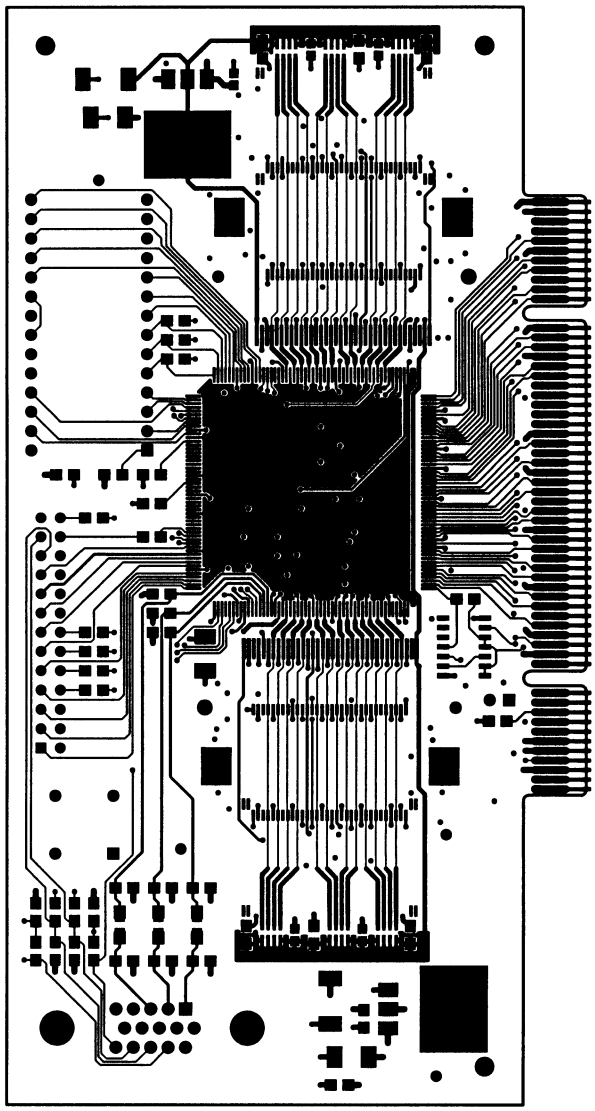

Figure B1-4. PCI Board — Component Side

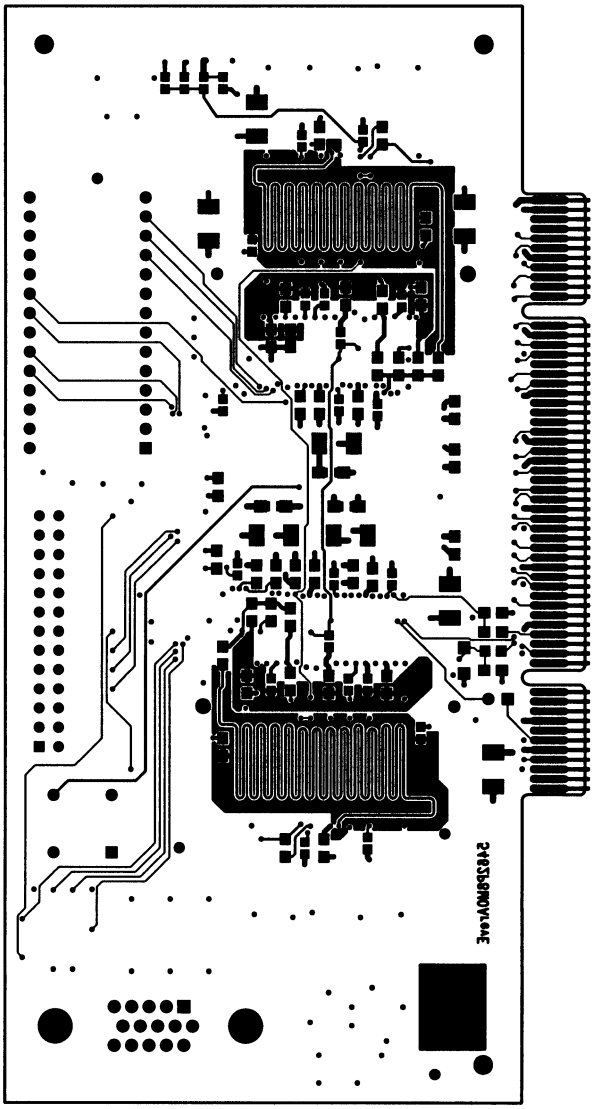

Figure B1-5. PCI Board — Solder Side

8.3 Rambus® Channel Clock

The Rambus channel clock is nominally 250 MHz and data is clocked on both edges (every 2.0 ns). Figure B1-6 shows how the clock is routed and how its name is changed.

The clock is generated in the CL-GD546X (the device boundary is shown as the dotted line at the left edge of the diagram) and comes out on the RABCLK pin. It is series-terminated in the nominal characteristic impedance at the source and pulled up to VTERM. It is routed in parallel with the Rambus channel (but not as part of the channel) to the end of the Rambus channel. At that point it is turned around and becomes RATCLK. It propagates to the CL-GD546X, turns around inside the CL-GD546X device to become RARCLK, propagates back out to the terminators, and is terminated to VTERM.

This scheme of driving the clock through the channel twice is fundamental to the Rambus and reduces the clock-to-data skew to an absolute minimum. When data is transferred from the RDRAMs to the CL-GD546X, it is clocked with RATCLK. This clock is propagating the same direction as the data and travels the same distance. When data is transferred from the CL-GD546X to the RDRAMs, it is clocked with RARCLK. Again, the clock is propagating the same direction and for the same distance as the data. For this scheme to work at its best, the clock traces must be identical to the data and control traces.

The clock is turned around at the CL-GD546X (changes from RATCLK to RARCLK) by connecting the two pads together inside the device (they are separated by a single ground pin). The purpose of making this connection inside the CL-GD546X is to equalize the package delays for the clock and data. Do not short these pins together externally.

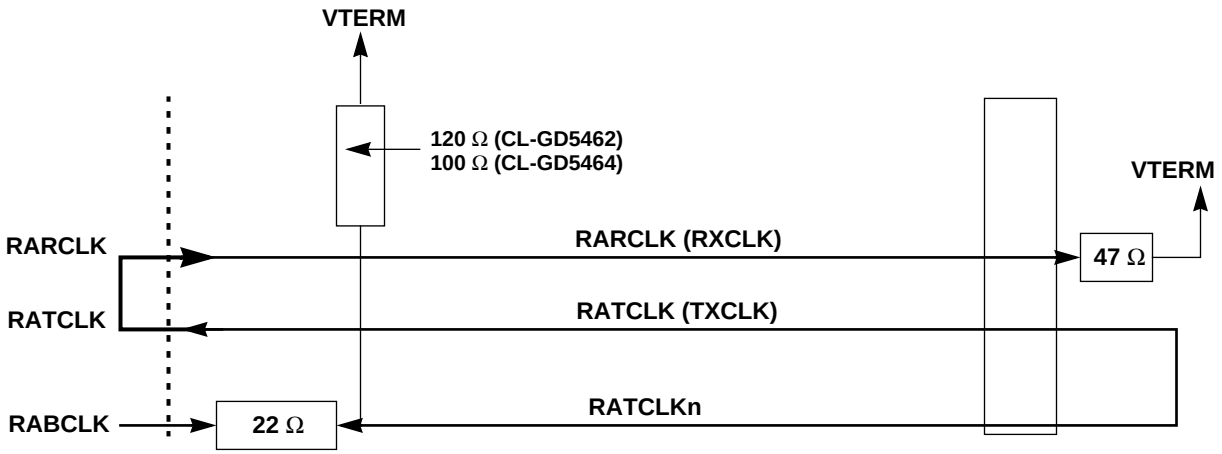

Figure B1-6. Rambus® Channel — Clock

8.4 RDRAM Array

Most of the signals travel in straight lines from the CL-GD546X, past the RSocket and RDRAMs, to the terminators. These high-speed signals must be routed on the component side of the board precisely as shown in Figure B1-4 on page B1-8. The SOUT/SIN chain is a low-speed signal and can be routed outside the channel or on the solder side of the board.

8.5 Expansion Socket

The RSocket is used for field upgrades. Systems designed for upgrading are shipped with one or two RDRAMs. The second module is plugged into the RSocket to increase the frame buffer size. The use of the RSocket has a few constraints.

The RSocket is located as close as possible (not more than 100 mils from pad to pad) to the CL-GD546X. This distance is selected to minimize reflections and ensure adequate noise immunity. RAVREF is decoupled with a 22-nF capacitor at the socket. This capacitor helps compensate for the fact that RAVREF has to transition to the solder side of the board underneath the RSocket. Three capacitors (22 nF, 0.1 μF, and 33 μF) decouple the 3.3-V rail at the RSocket.

8.6 Terminators

Each Rambus channel data, control, and clock line is terminated with a 47-Ω resistor to VTERM at its furthest point from the CL-GD546X. As noted later, 47 Ω is the nominal characteristic impedance of the transmission lines.

The layout requirements for terminating data signals are very strict for two reasons. The VTERM bypass capacitors must carry current for multiple signals and also be able to handle current to very low frequencies.

The VTERM is decoupled with six capacitors (one 1 μF and five each 0.1 μF). The layout of the terminators, the VTERM trace, and the bypass capacitors should be made exactly as shown. The VTERM is laid out as a very wide and a very low-impedance trace on the component side. The terminators and bypass capacitors are connected directly to the trace. The characteristic impedance of the traces must be controlled right up to the terminators. The traces should not be routed through vias or over breaks in the ground (or power) plane.

Low-inductance connections to ground vias must be used. Some design rules require thermal impedance patterns (thermal ‘wheels’) on the ground plane when using connections as wide as are required.

Because the data pattern on the Rambus channel is arbitrary, the current drawn from the VTERM has arbitrarily low and high frequencies. Therefore, the VTERM and regulation must be effective from DC to over 700 MHz. The regulator is combined with three types of bypass capacitors to span this range.

The regulator regulates itself from DC to approximately 50 kHz. The 100-μF regulator output capacitor has a reactance well under 1 Ω at these frequencies, much lower than the 12 terminators it bypasses.

8.7 VTERM and VREF Generation

The VTERM and VREF generator logic is shown in Figure B1-7.

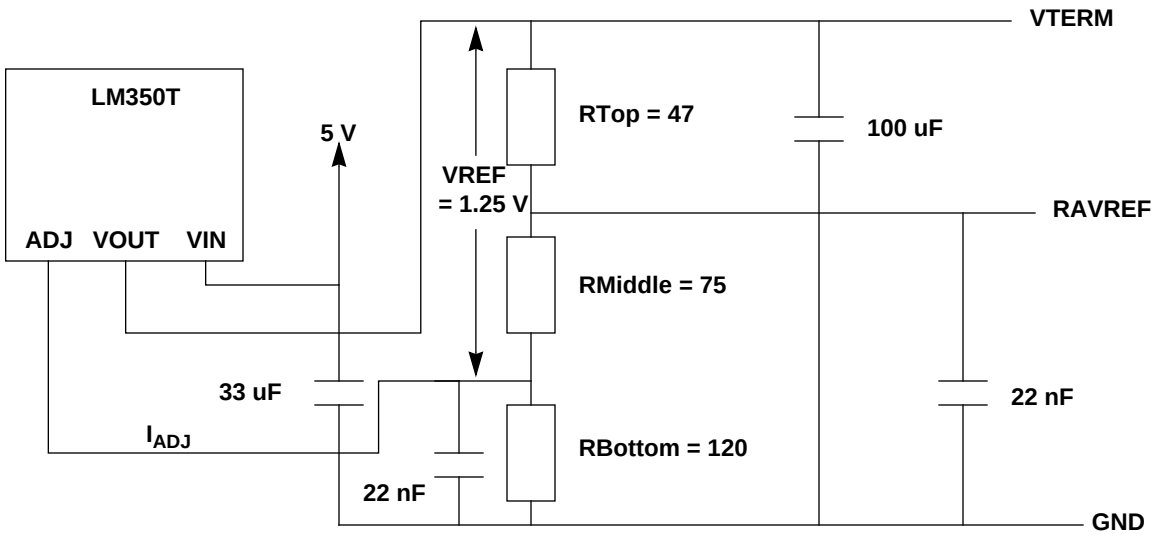

Figure B1-7. VTERM and VREF Generator

The equations for VTERM and RAVREF are as follows.

$$VTERM = VREF\left(1 + \frac{RBottom}{RTop + RMiddle}\right) + (IADJ \cdot RBottom)$$
$$= 2.49V$$

Equation B1-1

$$RAVREF = 1.25V \bullet \left[\frac{RMiddle + RBottom}{RTop + RMiddle}\right] = 2.09V$$
$$= VREF\left(\frac{RMiddle + RBottom}{RTop + RMiddle}\right) + (IADJ \cdot RBottom)$$
$$= 2.004V$$

Equation B1-2

8.8 Controlled Characteristic Impedance Traces

Due to the very high-frequency signals on the Rambus channel, it is necessary to control the characteristic impedance of most of the traces. The traces where the characteristic impedance must be controlled are the data, control, and clock lines.

Figure B1-8 shows an end view of a microstrip trace, defining the terms that are used in the following equations. The 'w' and 't' are the width and thickness of the trace, respectively. The 'h' is the dielectric thickness.

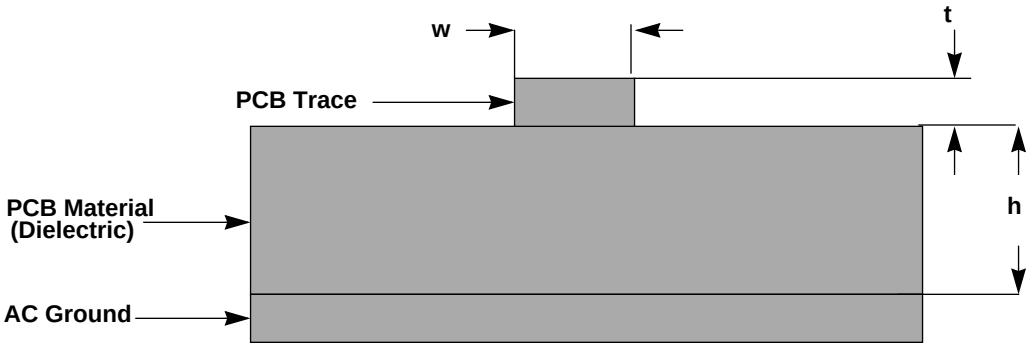

Figure B1-8. Microstrip Trace (End View)

The equation used to calculate characteristic impedance of a microstrip line is taken from the Fairchild ECL data book.

$$Zo = \left(\frac{87}{\sqrt{er + 1.41}}\right) \bullet \ln\left(\frac{5.98 \bullet h}{0.8 \bullet w + t}\right)$$ **Equation B1-3**

Using 4.0 as the dielectric constant, this equation can be simplified to:

$$Zo = 37.4 \bullet \ln\left(\frac{5.98 \bullet h}{0.8 \bullet w + t}\right)$$ **Equation B1-4**

This equation is evaluated for a number of values of ‘h’ and ‘w’ with ‘t’ fixed at 0.0015 in Table B1-1.

Table B1-1. Predicted Characteristic Impedance: *Zo*

Width	h = 0.006	h = 0.011
0.002	92	114
0.004	76	99
0.006	65	88
0.008	57	79
0.010	50	72
0.012	44	67
0.015	37	59
0.020	27	50

The desired characteristic impedance is on the order of 95 Ω when unloaded (47 Ω takes into account the capacitance of the RDRAM pad), and the maximum trace width is 8 or 10 mils. This requires some unusual board stacking.

8.9 Board Stacking

Non-traditional PCB stacking is needed to reduce the unloaded characteristic impedance to the required 95 Ω for four-layer boards. If this issue is not addressed, the impedance of the traces is not correct and the Rambus channel is noisy and may not work. In addition to controlling the stacking, the PCB vendor should be required to measure the trace impedance to demonstrate its accuracy.

Figure B1-9 shows the ‘traditional’ and ‘modified’ stacking for a four-layer PCB. The traditional stacking uses two pieces of 0.030 epoxy with a few mils of pre-preg between them. The modified stacking uses two pieces 0.011 epoxy with about 0.043 between them. This reduces the height (in the Equation B1-3 and Equation B1-4) to about 0.011 while retaining a total board thickness of 0.065.

Cirrus Logic and Rambus have approached several PCB vendors regarding this PCB geometry and have built a number of boards. There have been no technical or economic problems with it.

Note that using this method for four-layer motherboards (that already have controlled impedance traces) requires a reduction in the width of the controlled impedance traces.

For six- or eight-layer boards, an adaptation of this method can be used to get the top and bottom layers of epoxy to about 8 mils.

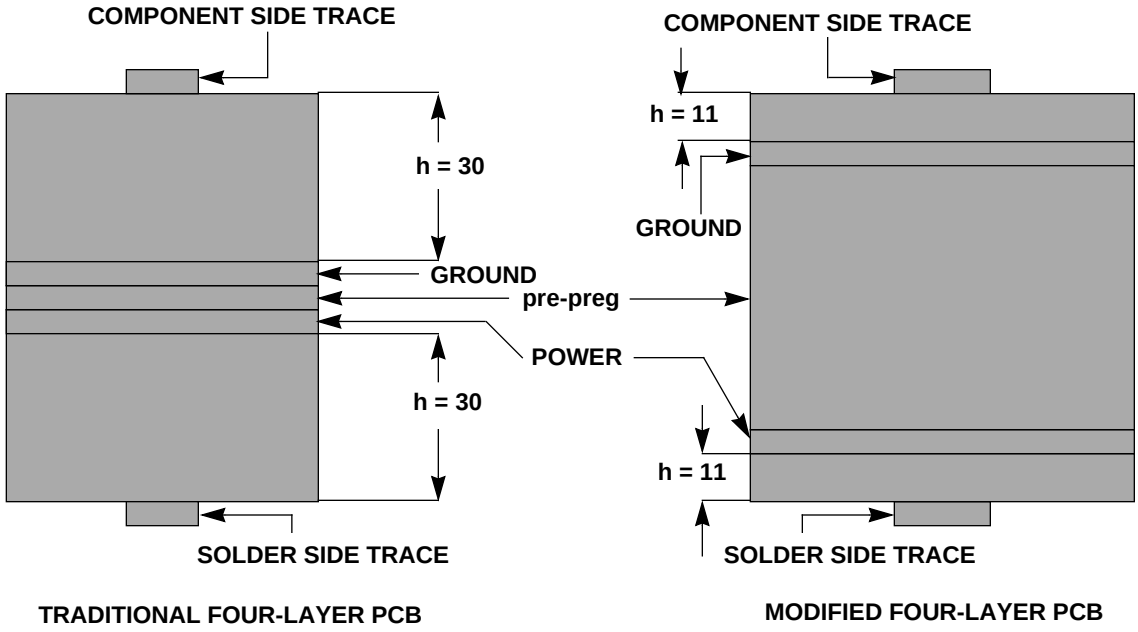

Figure B1-9. Four-Layer PCB Fabrication (Not to Scale)

8.10 PCB Design Rules

The design rules specified in this section are only for the geometry and impedance of the traces that carry the Rambus channel data and controls.

The geometric design rules specify minimum trace widths, trace spacing, via geometries, and other design properties of the board. These rules ensure high yields during manufacturing and assembly. The geometric rules proposed here allow the designer to specify a fine-pitch layout with the required vias and trace impedances.

The impedance rules help to guarantee the trace inductance and electrical properties of the finished assembly. To implement RSL traces, the PC board manufacturer needs only to control the impedance for a few trace widths on the component side. These trace impedances can be measured in the manufacturing process and on the finished boards.

Table B1-2. Printed Circuit Board Design Rules

Symbol	Parameter	English	Metric
ZO	Unloaded characteristic impedance	95 ± 10% Ω	95 ± 10% Ω
eR	Relative dielectric constant	4 ± 10% Ω	4 ± 10% Ω
W1	Trace width	6 ± 1 mil	0.15 ± 0.025 mm
S1	Trace spacing	6 ± 1 mil	0.15 ± 0.025 mm
d_v	Drilled via diameter (MIN)	15 mil	0.4 mm
d_p	Via pad diameter (MIN)	31 mil	0.8 mm
$(d_p–d_v)/2$	Pad annular clearance (MIN)	8 mil	0.2 mm

These design rules are selected to be cost effective, yet provide controlled impedance and 0.65-mm RDRAM pin pitch. If 5-mil traces with 5-mil spacing design rules are available, they provide better impedance control and tighter layouts.

The main constraints that RSL adds are:

- Microstrip construction, with signals on top and ground on layer 2 (next to the component layer)
- 10% impedance control
- Room for power and ground via pads between RSL signals. This constraint yields the following inequality:

$$w1 + s1 + dp + s1 \pounds 2 \times 0.65\ mm \qquad \textbf{Equation B1-5}$$

The dielectric constant of FR-4 PCB material is commonly given as er=4.3–4.7. Table B1-2 suggests a value of four. Measurements show that the dielectric constant of epoxy-glass PCB materials decreases with frequency. At GHz frequencies appropriate for RSL transition times, four is a better value. When working with PCB vendors, specify both impedance and delay in terms of high-frequency test methods.

8.11 PCB Geometry

8.11.1 Rambus® Channel Layout

Due to the high-speed nature of the Rambus channel signals, it is important to follow specific guidelines when the board layout is done. The designer must first choose a dielectric thickness for the board before proceeding to place components. The selection of a dielectric thickness determines the placement of the RDRAMs on the board. Figure B1-10 and Table B1-3 show the proper placement of components for various dielectric thicknesses. For manufacturing purposes, it may not be desirable to place the first RDRAM under the RSocket, optional layout parameters are provided for each dielectric thickness to extend the trace length to the first RDRAM.

NOTE: If a change in the dielectric thickness is required, a new board layout is needed.

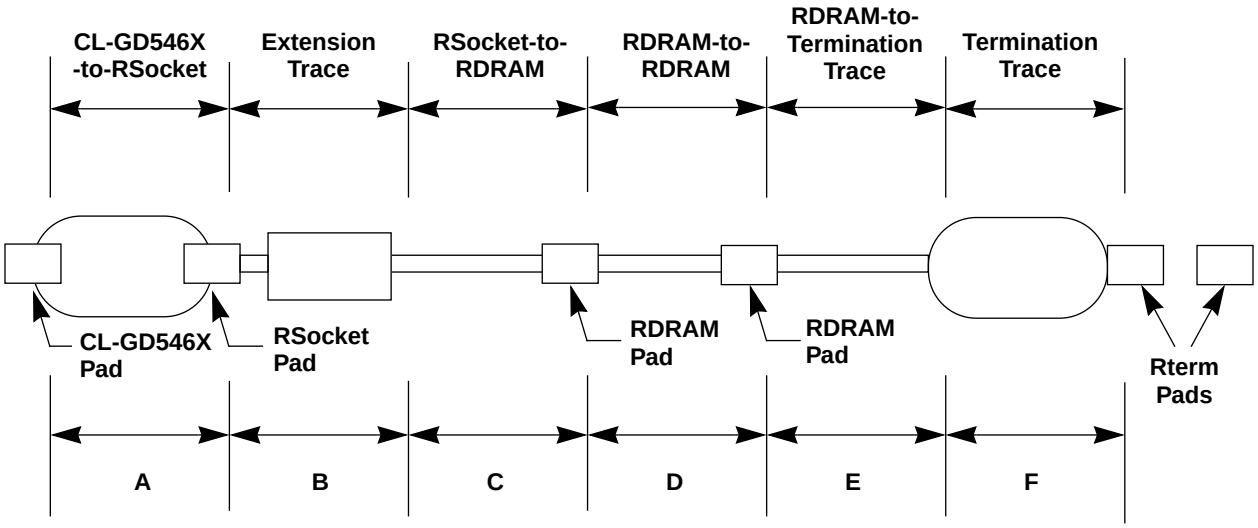

Figure B1-10. Line Length and Width for the CL-GD546X–Rambus® Channels

The extension trace (dimension B) is not required for a standard layout. It is therefore shown in Table B1-3 to have a length and width of zero when the standard placement locates the first RDRAM under the RSocket.

NOTE: These parameters must be strictly adhered to for proper impedance matching for a given dielectric thickness; however, alternative dielectric thickness parameters are available upon request.

Table B1-3. Trace Dimensions

Dielectric Thickness (mils)		11		6	
RDRAM Under RSocket?		Yes	No	Yes	No
A	length (mils) width (mils)	200 26	200 26	200 20	200 20
B	length (mils) width (mils)	0 0	477 21	0 0	205 11
C	length (mils) width (mils)	320 6	273 6	545 6	545 6
D	length (mils) width (mils)	545 6	545 6	1090 6	1090 6
E	length (mils) width (mils)	273 6	273 6	545 6	545 6
F	length (mils) width (mils)	≥ 300 21	≥ 300 21	≥ 0 11	≥ 0 11

All dimensions provided assume that the minimum spacing between traces is 6 mils and that all traces are free of vias. In addition, all traces should follow a straight line where possible and any necessary bends must be at 45º.

Dimension F is allowed an increase to support the placement of through-hole resistors; however, shorter traces are preferred and the lengths must not vary more than ± 100 mils from signal to signal.

8.11.2 Coplanar Waveguide (Serpentine) Clock Trace

To support the RSocket memory expansion modules (RModules), the transmit clock (TxCLK) trace length from the on-board RDRAMs back to the CL-GD546X must match that of the expansion modules. The best implementation routes the clock on the solder side of the board, causing the clock to be referenced against the power plane, which is undesirable. The solution is to route the clock as a coplanar waveguide that surrounds the high-speed clock signal by ground with a small air gap as shown in Figure B1-10.

NOTE: The BSCLK and TxCLK refer to the RABCLK/RBBCLK and RATCLK/RBTCLK signals of the CL-GD546X.

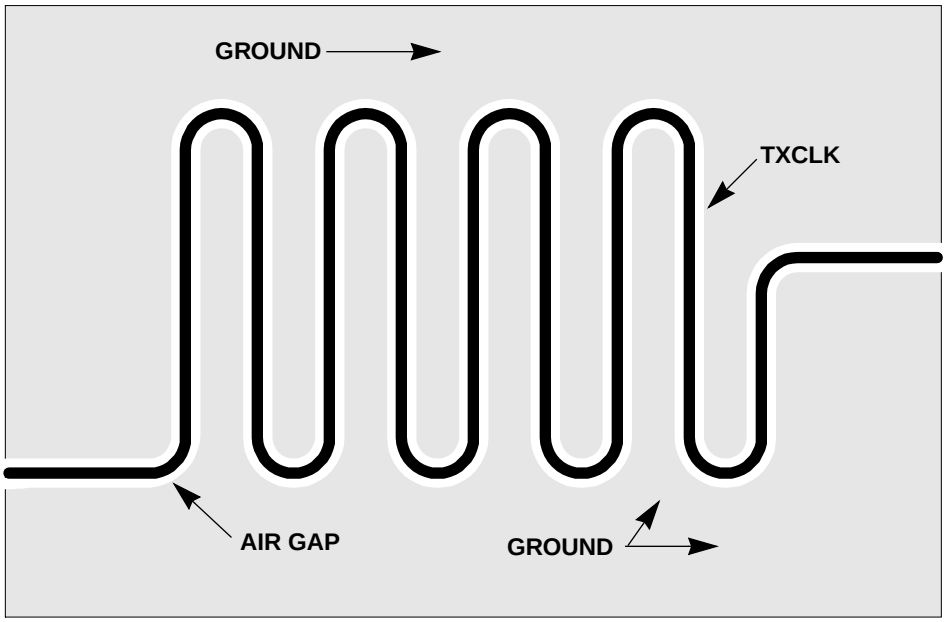

Figure B1-11. Coplanar Waveguide

The dimensions required for the clock trace is determined by the thickness of the selected dielectric, and requires a new layout if the dielectric thickness changes. The following table shows values that should be used for some suggested dielectric thicknesses. Alternative dielectric thickness parameters are available upon request.

Dielectric thickness (mils)	**11**	**6**
Air gap	6	8
Ground fingers	8	6
TxCLK	14	10

It is important to maintain a continuous air gap around the trace during all bends, and to connect the ground surrounding TxCLK to the ground plane by vias every 100 mils.

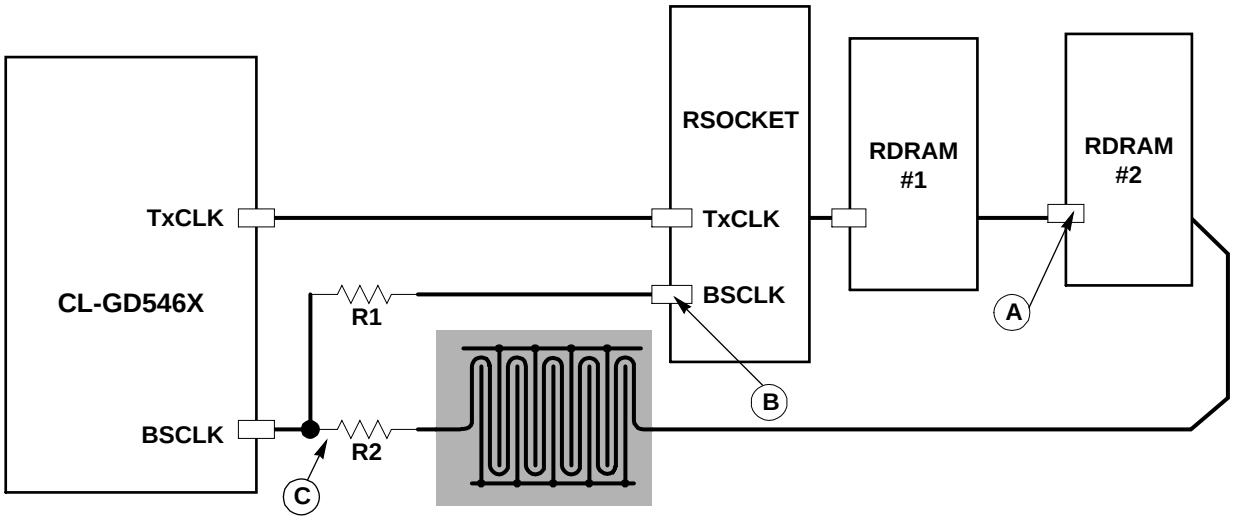

Figure B1-12. RDRAM Clock Layout

For proper RModule operation, the length of the TxCLK trace from A-to-C must be the same as that from B-to-C plus 10.7 inches (AC = BC + 10.7).

8.11.3 Component Side Clock Routing

If there is sufficient room to route the clock on the component side of the board or if there is a need to transition to the component side, the RDRAM clock traces should be routed using the following trace thicknesses while on the component side.

Dielectric Thickness (mils)	11	6
TxCLK	21	11

8.11.4 External Rambus® Clock Generator Circuit Layout

If the board includes the option of stuffing an external clock generator for the Rambus clock, place the clock generator (approximately centered) above the CL-GD546X. This reduces the differences between the clock lengths to the A and B channels of the CL-GD546X.

The circuit contains series resistors at both the source and destination of the clock signal. The zero-Ω resistors (R9, R10, R13, R14) should be placed as close as possible to the destination of the clock so that, when removed, there is only a short stub remaining in the signal path of the clock when it is being driven by the CL-GD546X. The larger (approximately 33 Ω) resistors (R5, R6, R7, R8) should be placed as close as possible to the clock generator to reduce the amplitude of the clock output. It is recommended that resistors in the 0603 package be used due to their better characteristics at higher speeds.

Routing of this clock should be done as a coplanar waveguide without any vias along its path. Although this can be difficult to do, moving the larger bulk capacitors (10 μF) slightly out from behind the device can help to reduce this problem with negligible effect on the supply voltage to the CL-GD546X.

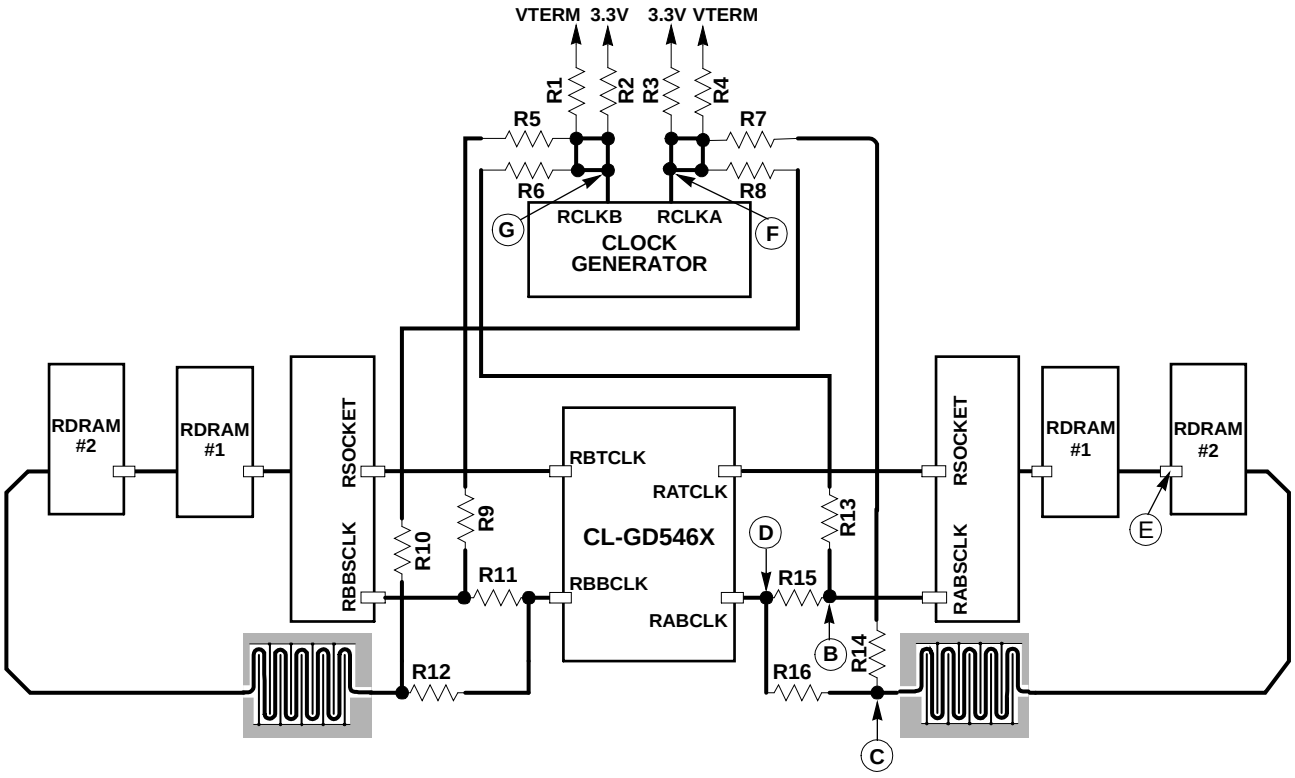

Figure B1-13. External RDRAM Clock Generator Layout

Line lengths for all Rambus clock signals are extremely important. Equation B1-6 and Equation B1-7 represent line lengths (in inches) that must be maintained between the indicated reference points in Figure B1-13:

$$DC + CE = DA + 10.7 \qquad \textbf{Equation B1-6}$$

$$FC + CE = GB + BA + 10.7 \qquad \textbf{Equation B1-7}$$

These equations represent the calculations for channel A on the CL-GD546X; however, the same relative calculations are required for channel B, with the additional requirement that equivalent clock signal lengths for channel A and channel B must be equal to within 1.0 inch.

8.11.5 VTERM Layout

The termination resistors and capacitors of the Rambus channels should be connected to a thick VTERM island that is roughly 100 mils wide. This island should be sourced from a normal thick trace of 8–12 mils as shown in Figure B1-13. All other required VTERM traces should also be 8–12 mils wide.

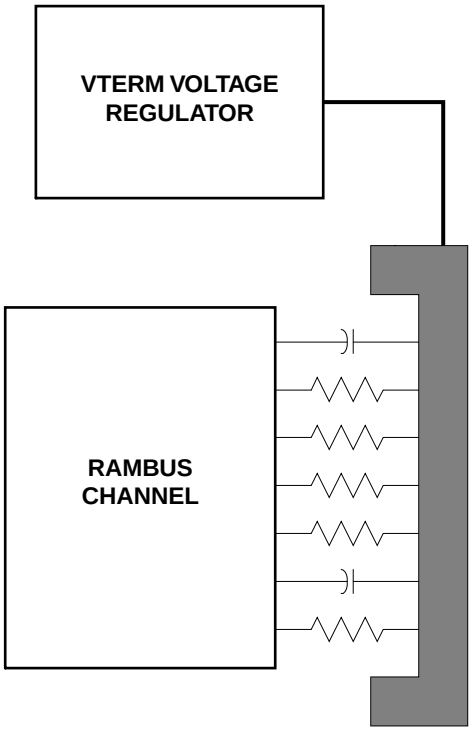

Figure B1-14. VTERM Layout

8.12 Notes

The designer must not omit power or ground vias. At RSL speeds, it is extremely important that each power pin be directly connected to the power plane. Each power and ground pin must connect to an adjacent via to the appropriate power plane. Each RDRAM has its own bypass capacitors. Care should be taken to make the traces to each power and ground via as short as possible.

Due to lack of space, ground and power traces need not extend through the unloaded sections. Some higher-impedance designs have room to extend these power traces. To minimize crosstalk, the designer should extend these power traces if possible.

N/C pins on the RDRAM must be left unconnected. Some RDRAM designs electrically connect these pins to the device substrate.

On occasion, traces need to go around corners. This is especially likely for the clock traces. Figure B1-15 shows how these corners should be designed. The outside of the corner should be trimmed. This reduces the excess capacitance that would be contributed by the outside of the corner (shown as a dotted line). The 1.8w rule also applies to obtuse angles. Bends greater than 90º should be broken into two bends, separated by at least twice the trace width, each compensated as shown in Figure B1-15.

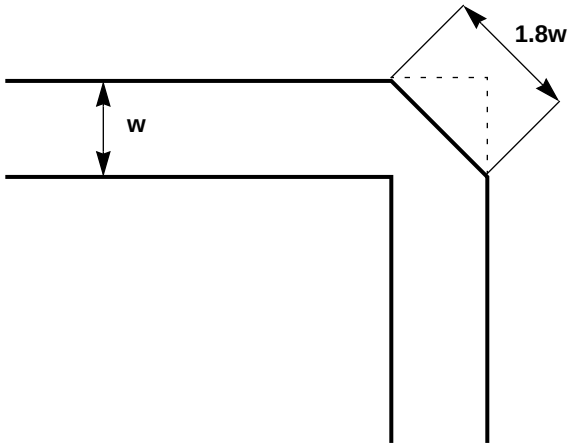

Figure B1-15. Trace Corner Design

8.13 Checklist

Overall, the layout should follow the example in Figure B1-1 on page B1-3. There are a number of subtle points that need to be verified. This checklist duplicates points already covered; it allows the designer to verify all design issues that have been checked.

Table B1-4. Rambus® Channel Checklist

Item	✔
Does the layout look like the layout in Figure B1-4?	
Are all the trace widths on all high-speed RSL signals correct as shown in Table B1-3?	
Is the next plane in the stacking, immediately below the component side, on the ground plane?	
Is the spacing from the component side to the ground plane correct as specified in Table B1-3?	
Are all power and ground vias as close as possible to their respective pads?	
Do any bent RSL traces (clock) conform to the bent trace rule shown in Figure B1-15?	
Is the trace width of the clock-to-end signal the proper width, as shown in Table B1-3?	
Is the Rambus channel clock signal routed as a coplanar waveguide when referenced to the power plane?	

