Appendix B2

PCI Bus Reference Design

PCI BUS REFERENCE DESIGN

1. INTRODUCTION

This appendix covers the schematics of the CL-GD5464 reference adapter board design for the PCI bus. This board can be populated with any of the CL-GD546X devices. The board can be populated with 2 to 8 Mbytes of RDRAM display memory.

The schematics are captured using OrCAD® SDT. These schematics and the associated Gerber files are available to Cirrus Logic customers on request. Board design notes are also included.

2. PCI BUS INTERFACE

2.1 Bus Connections

The CL-GD546X is designed for a glueless interface to the PCI bus. The pins on the CL-GD546X are directly connected to similarly named pins on the PCI bus. This is summarized in Table B2-1.

Table B2-1. PCI Bus Connections

Pin Names	Function	Note
AD[31:0]	Address/data bus	
PAR	Parity	
STOP#	Control	
C/BE[3:0]#	Control	
FRAME#	Control	
IRDY#	Control	
TRDY#	Control	
IDSEL	Control	
CLK	Clock	
RST#	Control	
DEVSEL#	Control	
INTR#	Interrupt request	Connected with jumper
REQ#/GNT#	Bus exchange	Not used on the CL-GD5462
TDI/TDO	System control	Tied together

The CL-GD546X is placed within an inch of the PCI connector and is approximately centered on the connector. The pin assignments on the CL-GD546X are carefully optimized to allow short and direct connections between the bus pins and the CL-GD546X pins.

2.2 INTA# Pin

The INTA# pin is connected from CL-GD546X with a jumper. Whether an interrupt is claimed can be configured. If no pull-down resistor is installed on INTA#, PCI3C is a read/write register and interrupt 2 can be claimed by writing the value ‘02h’. If a pull-down resistor is installed on INTA#, the PCI3C is a read-only register that always returns the value ‘00h’. In this case, no interrupt can be claimed by the CL-GD546X.

2.3 VGA BIOS

The CL-GD546X is designed to comply with the PCI requirement that a single load appear on each signal. This requirement precludes connecting the BIOS EPROM directly to the bus. Instead, the EPROM is connected only to the CL-GD546X. The EPROM address inputs are driven with dedicated pins on the CL-GD546X (RA[15:0]). The EPROM data pins are connected to RD[7:0]. The EPROM enables are both driven with the CL-GD546X ROMCS#.

A 27C256 EPROM contains the 32-Kbyte VGA BIOS. The address pins are connected directly pin-to-pin; no address bit swapping is used. RA15 from the CL-GD546X is not connected.

3. DISPLAY MEMORY INTERFACE

3.1 Memory Configurations

The display memory is made up of one or two RDRAMs soldered to the board, plus another mounted in a socket. Only Rambus channel A can be used with the CL-GD5462 and the CL-GD5464. Table B2-2 indicates the memory configurations available with this design.

Table B2-2. Display Memory Configurations

Capacity	Devices
2 Mbytes	U6
4 Mbytes	U6, U7
8 Mbytes	U6, U7, J3

3.2 Rambus® Access Channel Design

The layout of the RAC (Rambus access channel) is described in Appendix B1, “Layout Guidelines” on page B1-17. The terminators for Channel A, and the VTERM and VREF generators are shown in the schematic diagrams included in this appendix. The equations relating to the VTERM and VREF generators are also discussed in Appendix B1. The power conditioning for the RAC is shown in the schematic diagrams included in this appendix.

Rambus access Channel B is also shown in the schematic diagrams. This channel is not used for the CL-GD5462 or the CL-GD5464.

4. MONITOR INTERFACE

4.1 RGB Lines

The RGB lines are terminated in 75 Ω to DACVSS. This provides half of the nominal 37.5-Ω DC load; the other half is in the monitor.

The π filters on each RGB line control edge rates and reduce RFI (radio frequency interference) to an acceptable level. The component values in these filters represent a trade-off. For good crisp video, especially at higher frequencies, the cutoff frequency should be as high as possible. On the other hand, for reduced emissions the cutoff frequency should be fairly low.

The resistors are located as close as possible to the CL-GD546X. The filters are located very close to the DB-15 connector. The traces between the CL-GD546X and the filters are direct with no vias and no sharp corners. These traces must be designed with a characteristic impedance as close as possible to 75 Ω. The edge rates, especially before the filters, are fast enough that a trace as short as a few inches begins to behave as a transmission line.

4.2 Sync Lines

The HSYNC and VSYNC are isolated with the π LC filters of ferrite bead (17 Ω at 100 MHz) and 220-pF capacitor. The filter outputs connect directly to the DB-15 and VESA connectors.

4.3 Monitor ID

The BIOS requires information regarding the capability of the connected monitor so that it can program the appropriate refresh rates for the various video modes. In some cases, due to monitor capability, the higher resolution modes cannot be programmed at all.

The DDC2B is a bidirectional data channel based on the I^2C bus. The data clock is on MID3 (DB15 pin 15) and the bidirectional data is on MID1 (DB15 pin 12). DDC2B is an open-collector protocol. The logic in the controller must pull-up each of the two signals (MID1 and MID3) and drive each signal low. In addition, the software must be able to sense each line (MID1 and MID3). These signals are named SDAn and SCLn, respectively, in the schematic diagrams.

The SDAn is connected to the SDA pin and SCLn is connected to the SCL pin. Each of these pins can be driven low and can be sensed by the CL-GD546X. Refer to the *Laguna VisualMedia™ Accelerators Family — CL-GD546X Volume II (Software Reference Manual, Second Edition)* for programming examples.

5. VESA® CONNECTOR

5.1 Standard VESA® Interface

The VESA connector pins are tied to the corresponding pins on the CL-GD546X either directly or through an appropriate resistor. Table B2-3 shows the pins on the VESA connector.

Table B2-3. VESA® Connector Pins

Pin	Function	Note	Pin	Function	Note
Z1	GND		Y1	P0	
Z2	GND		Y2	P1	
Z3	GND		Y3	P2	
Z4	EVIDEO#	1 kΩ	Y4	P3	
Z5	ESYNC#	1 kΩ	Y5	P4	
Z6	EDCLK#	1 kΩ	Y6	P5	
Z7	SCL	a	Y7	P6	
Z8	GND		Y8	P7	
Z9	GND		Y9	DCLK	
Z10	GND		Y10	BLANK#	
Z11	GND		Y11	HYSNC	Filtered
Z12	VCLK	b	Y12	VSYNC	Filtered
Z13	SDA	c	Y13	GND	

a Z7 is a no connect in the VESA specification. Cirrus Logic uses this pin as the clock pin of an I2C interface.

b Z12 is no connect in the VESA specification. Cirrus Logic uses this pin for the video clock.

c Z13 is a no connect in the VESA specification. Cirrus Logic uses this pin as the data pin of an I2C interface.

5.2 Enhanced V-Port™

The Enhanced V-Port is not supported in this reference design.

5.3 I²C Interface

The I²C interface allows the host to communicate with devices using the standard TV tuner interface. The Z7 and Z13 on the VESA connector are used.

6. POWER DISTRIBUTION AND CONDITIONING

6.1 Introduction

The most common reason for unsatisfactory performance of a video subsystem is a failure on the part of the board designer to properly manage power distribution and conditioning. Dedicated power and ground planes are very strongly recommended for boards based on all the CL-GD546X devices.

6.2 Dedicated Ground Plane

A dedicated ground plane minimizes differential ground offsets and more nearly approximates the ideal notion of 'ground'. Additionally, a ground plane is necessary to predict and control the characteristic impedance of those traces that must be treated as transmission lines.

The ground plane has cuts to partially isolate the critical analog VSS sections from the relatively noisy digital VSS associated with the RDRAM array and the bus interface. These cuts can be studied in the Gerber plots. On the schematic diagram, there are three ground nodes. The digital ground is designated with a standard ground symbol. The two isolated grounds are designated DACVSS and RBAGND.

6.3 Dedicated Power Plane

A dedicated power plane allows low-impedance distribution of VCC, minimizing noise and coupling. A dedicated power plane also behaves as an AC ground, making it possible to predict and control the characteristic impedance of traces above it (the Rambus channel traces are all referenced to ground).

The CL-GD546X and the RDRAMs are 3.3-V devices. The EPROM and reference oscillator are 5-V devices. This leads naturally to a divided power plane as shown in Figure B2-1. The area around the periphery of the board is 5 V, and provides power to the oscillator and the EPROM. The area in the middle of the board provides power to the CL-GD546X and the RDRAMs. All the logic in the CL-GD546X, including the I/O buffers, is powered with 3.3 V. The 3.3 V is derived from 5 V with a standard three-terminal regulator as shown in the schematic diagrams.

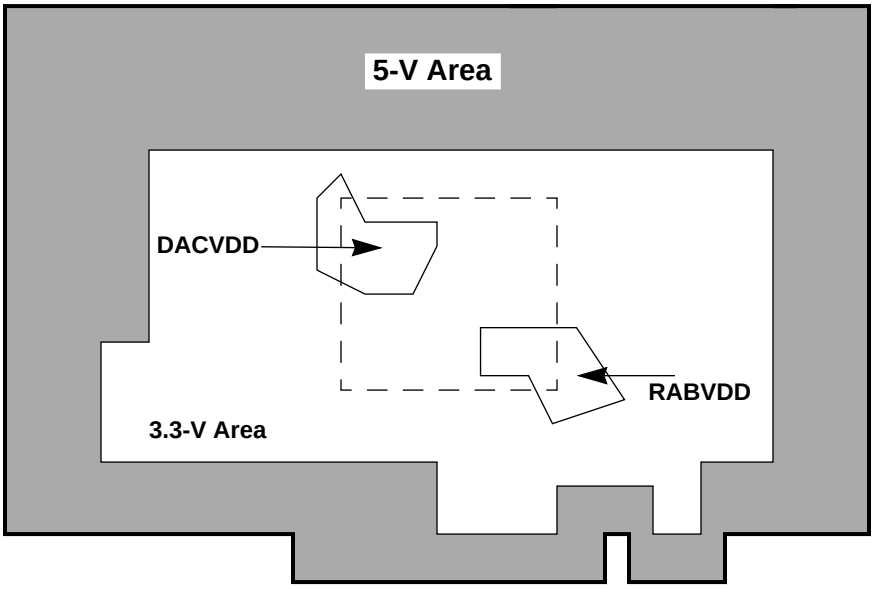


Figure B2-1. Power Plane

6.4 Power Bypassing

Bypass capacitors are used to minimize power sags caused by current spikes and reduce the power distribution impedance. Bulk bypassing is present in the area where power comes onto the board, around the DRAM array, and near the EPROM.

High-frequency bypass capacitors are distributed as needed on the board. Every digital V_{CC} pin on the CL-GD546X has a bypass capacitor located as close to the pin as possible. Each pin is connected to its capacitor – and the power plane – with a short, thick, direct lead. The ground connection of each capacitor is made with a via directly to the ground plane. The Rambus channels are heavily bypassed, and this is described in Appendix B1.

6.5 Power Conditioning

Two areas on the power plane are further isolated within the 3.3-V section.These are designated DACVDD and RBAVDD. Each is connected to the 3.3-V section through an LC filter consisting of a Ferrite bead and a 10-µF capacitor in parallel with a 0.1-µF capacitor. Each capacitor in each filter is returned to its respective cutout on the ground plane.

6.6 Configuration Resistors

The configuration resistors in Table B2-4 are shown in the schematic.

Table B2-4. Configuration Resistors

Pin	Use (if Installed)
RA15	32-Kbyte BIOS
RA6/RA5/RA4	GPIO configuration
RA3	Bypass mode CL-GD5462 (for testing only)/ VGA disable CL-GD5464

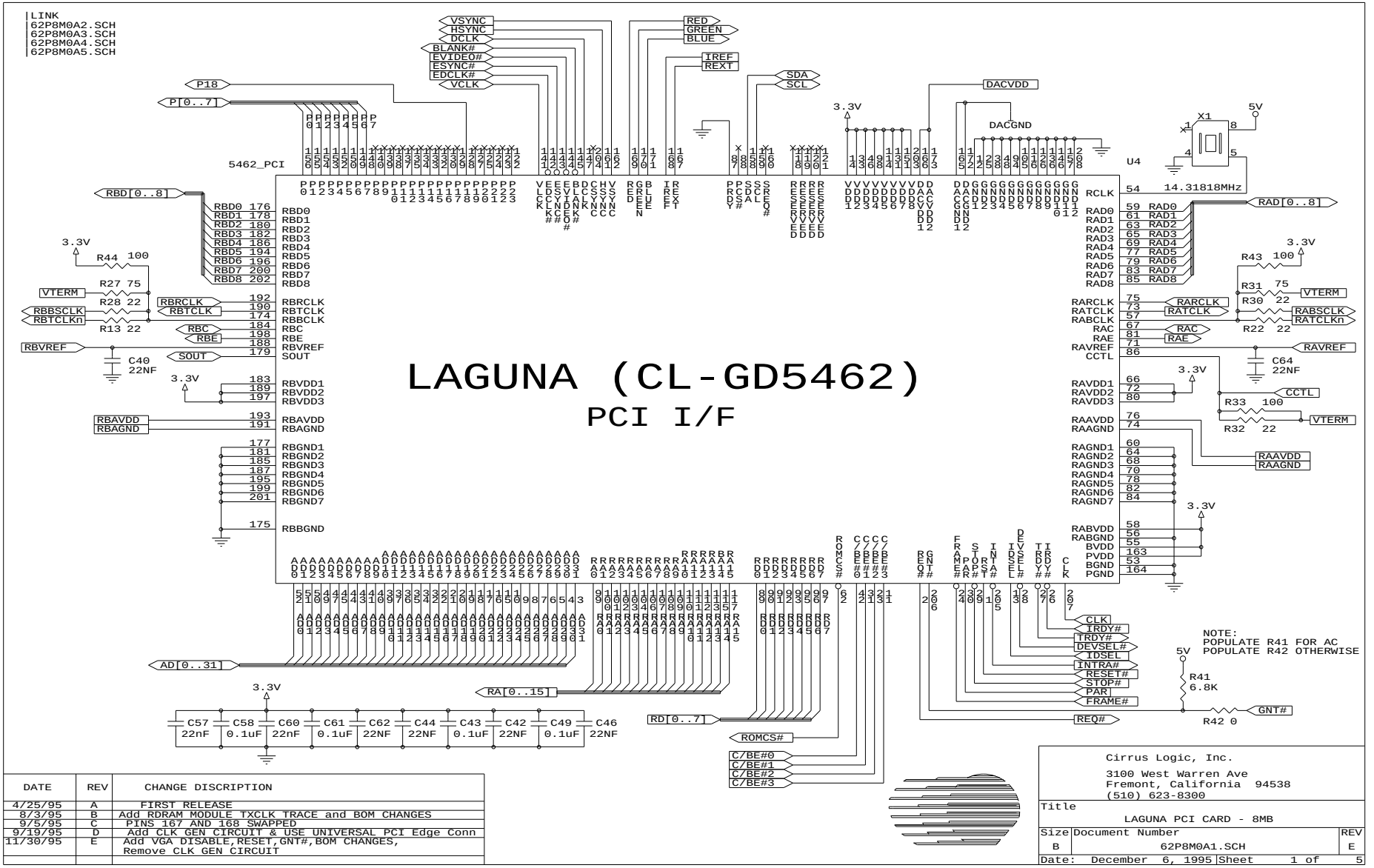
6.7 Synthesizer Reference

The 14.3-MHz reference required by the dual-frequency synthesizer is supplied by a crystal oscillator. This is connected directly to the RCLK pin.

6.8 Current Reference

The CL-GD546X has an integrated current reference that requires only a resistor to set the full-scale current level and a capacitor on IREF. The resistor value can be calculated with the Equation B2-1 where *load* is the DC load in ohms, and *VFullScale* is the desired full-scale voltage. This logic is shown in the schematic diagrams.

$$RSet = \frac{2.52V \bullet Load}{VFullScale}$$ **Equation B2-1**



DATE	REV	CHANGE DISCRIPTION
4/25/95	A	FIRST RELEASE
8/3/95	B	Add RDRAM MODULE TXCLK TRACE and BOM CHANGES
9/5/95	C	PINS 167 AND 168 SWAPPED
9/19/95	D	Add CLK GEN CIRCUIT & USE UNIVERSAL PCI Edge Conn
11/30/95	E	Add VGA DISABLE,RESET,GNT#,BOM CHANGES, Remove CLK GEN CIRCUIT

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Title		
LAGUNA PCI CARD - 8MB		
Size	Document Number	REV
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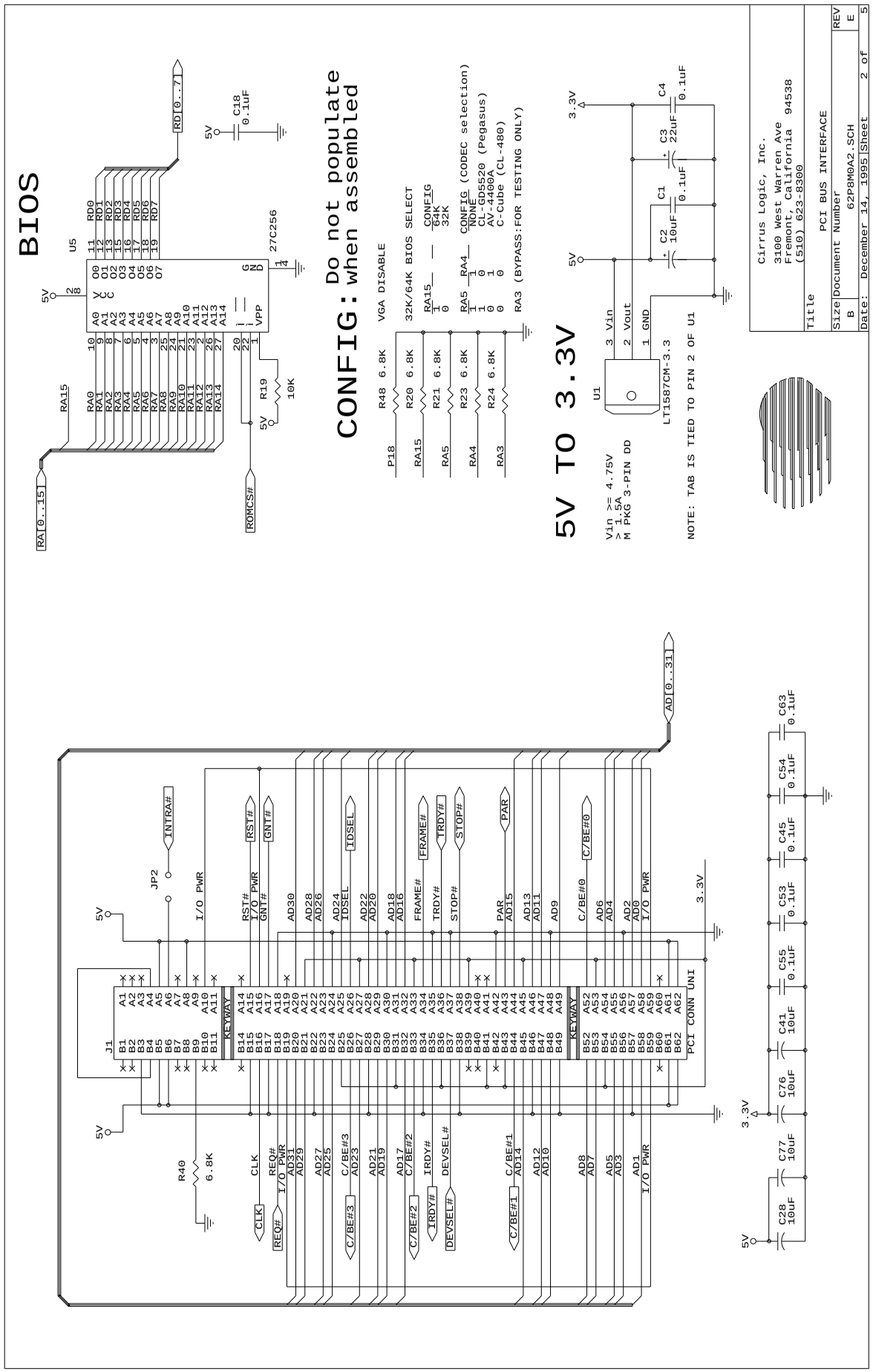
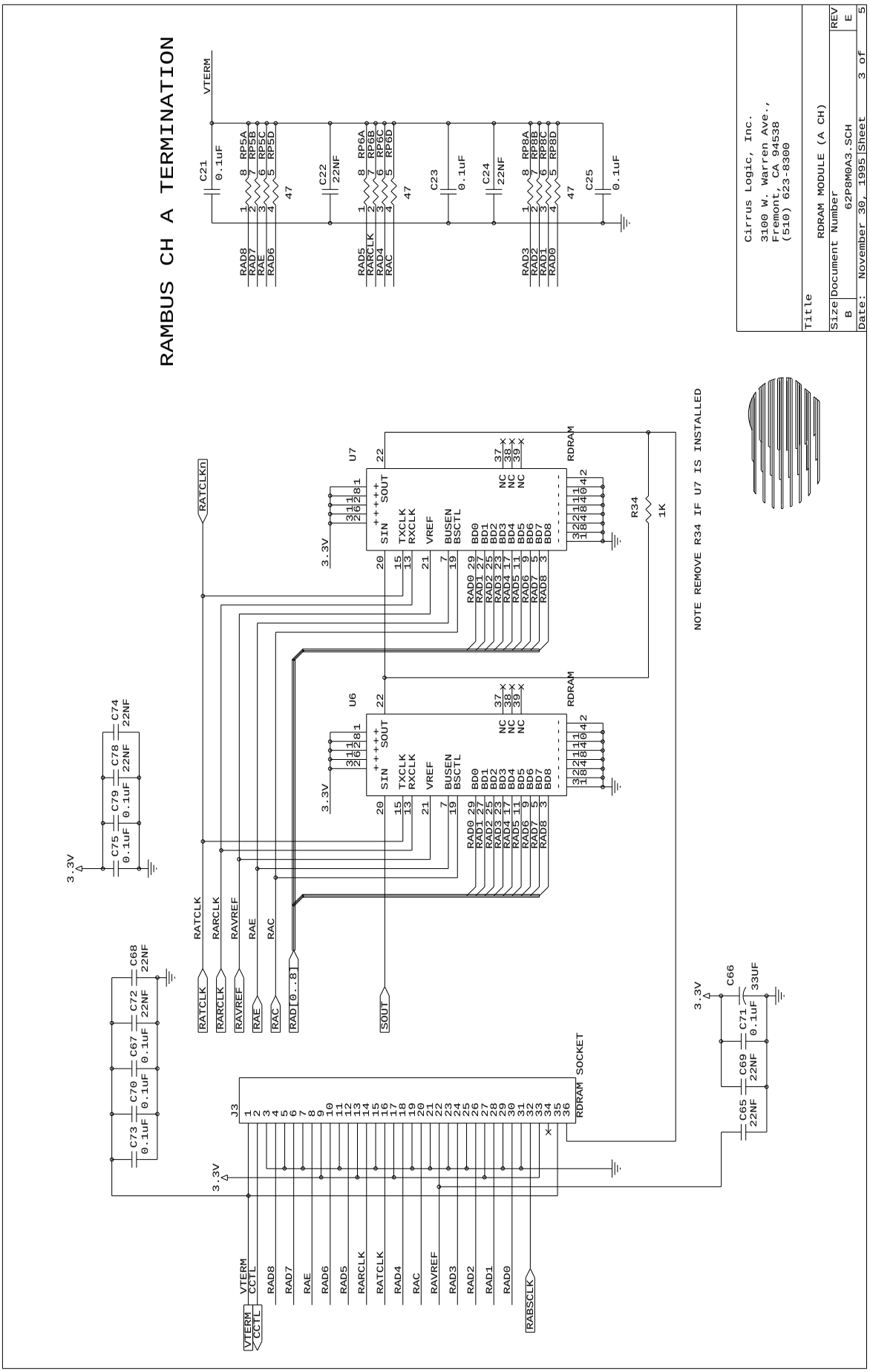
Date: December 6, 1995	Sheet 1 of 5	




RAMBUS CH A TERMINATION
NOTE REMOVE R34 IF U7 IS INSTALLED
RDRAM SOCKET
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RDRAM MODULE (A CH)
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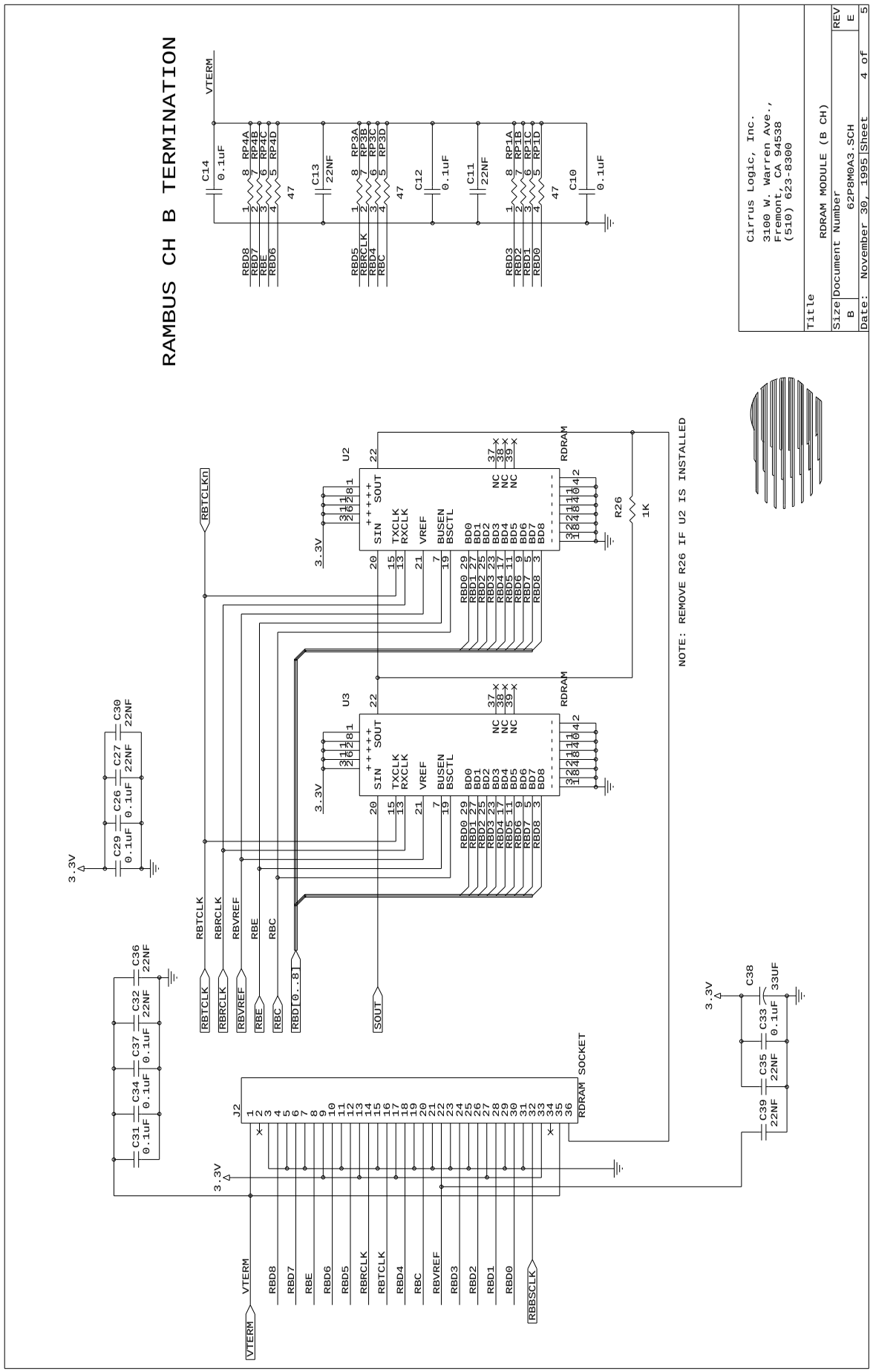
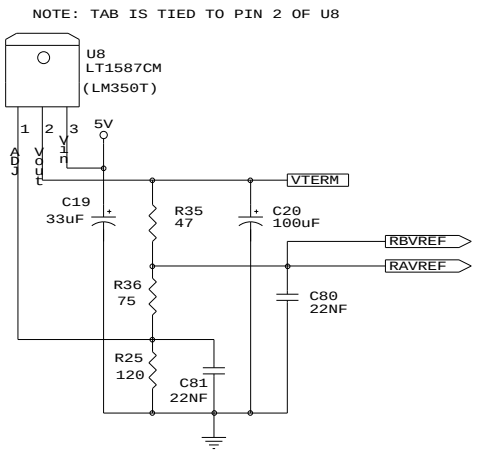
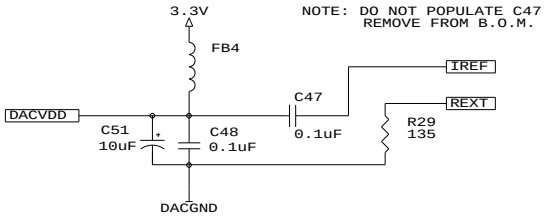


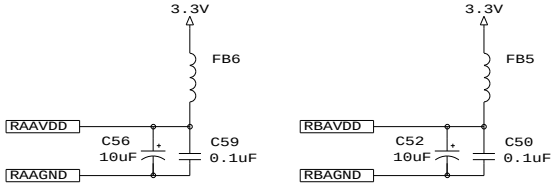
Vterm/Vref Generation



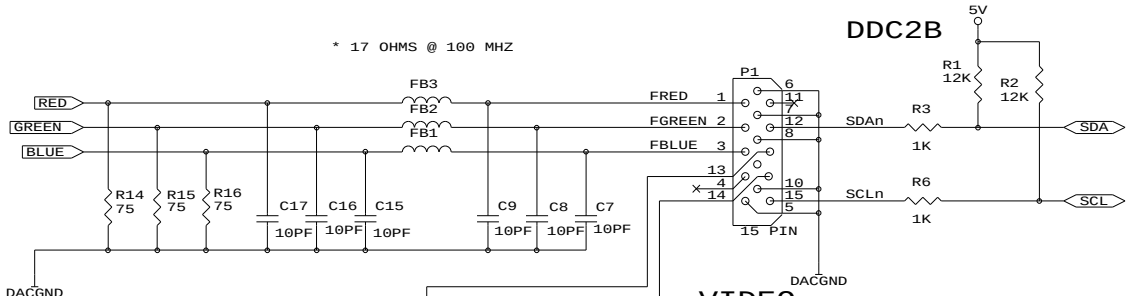
DAC VDD, GND, & RSET

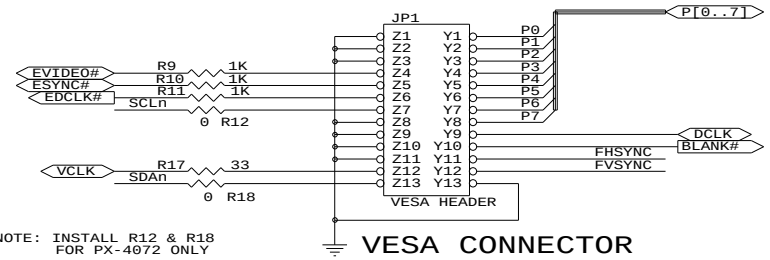


RAMBUS CHANNEL VDD & GND



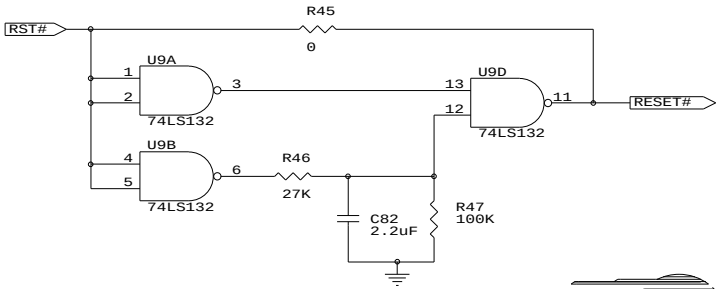
DDC2B





RESET CIRCUIT

NOTE: DO NOT POPULATE R45 FOR AC SILICON, POPULATE R45 FOR FUTURE SILICON ONLY.



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