2. DETAILED PIN DESCRIPTIONS

The following tables give a detailed description of each CL-GD546X pin by name and functional type. Functional pin types are abbreviated as follows:

Type	Abbreviation
Input	I
Output	O
Input/output	I/O
Tristate output	TS
Power	PWR

Type	Abbreviation
Ground	GND
Open collector	OC
'–'	Indicates ascending pin numbers
':'	Indicates decending pin numbers

2.1 Host Interface Pins

Table 2-1. Host Interface — PCI Bus

Name	Type	Description
RST#	I	**System Reset #:** This active-low input initializes the CL-GD546X to a known state. Configuration bits are loaded on the rising (trailing) edge of this signal. The Subsystem ID registers are loaded from the BIOS ROM after the trailing edge of this signal.
CLK	I	**Local Bus Clock:** This is the bus timing reference for the CL-GD546X. All synchronous bus activity is referenced to the rising edge of this clock.
AD[31:0]	I/O	**Address/Data:** These multiplexed and bidirectional pins are used to transfer system address and data during any memory or I/O operation. During the first clock of a transaction, these pins contain a 32-bit physical byte address. During subsequent clocks, they contain data.
CBE[3:0]#	I/O	**Command/Byte Enable #:** These multiplexed pins are used to transfer the bus command and the byte enables. During the address phase of the operation, CBE[3:0]# define the bus command (refer to Table 2-2). The CL-GD546X responds as a target to the values listed in the following table. When the CL-GD5464 is a bus master it generates memory read and memory write commands. During the data phase(s), these pins are used as byte enables.

Table 2-2. Commands

CBE[3:0]#	Command Type
02h	I/O read
03h	I/O write
06h	Memory read
07h	Memory write
Ah	Configuration read
Bh	Configuration write

Table 2-1. Host Interface — PCI Bus *(cont.)*

Name	Type	Description
FRAME#	I/O	**Cycle Frame #:** As an input, this pin is driven by the current master to indicate the beginning and duration of an access. For the CL-GD5464 as a bus master, this output is a sustained tristate as defined in the PCI specification. FRAME# is asserted to indicate the beginning of a bus transaction. While FRAME# is asserted, data transfers continue. The transaction is in its final data phase when FRAME# is deasserted.
IRDY#	I/O	**Initiator Ready #:** As an input, indicates the initiating agent's ability to complete the current data phase. For the CL-GD5464 as a bus master, this output is a sustained tristate as defined in the PCI specification. A data phase is completed on any clock cycles that IRDY# and TRDY# are both asserted.
TRDY#	I/O	**Target Ready #:** As an output, indicates the target agent's (the CL-GD546X) ability to complete the current data phase. This output is a sustained tristate as defined in the PCI specification. This pin is an input for palette snooping when the CL-GD546X is a target. For the CL-GD5464 as a bus master, this pin is an input.
DEVSEL#	I/O	**Device Select #:** This output is driven active-low when the CL-GD546X has decoded its address as the target of the current access. This output is a sustained tristate as defined in the PCI specification. This pin is an input for palette snooping when the CL-GD546X is a target. For the CL-GD5464 as a bus master, this pin is an input.
STOP#	I/O	**Stop #:** This active-low output indicates a request to the bus master to stop the current transaction. This output is a sustained tristate as defined in the PCI specification. This pin is an input for palette snooping when the CL-GD546X is a target. For the CL-GD5464 as a bus master, this pin is an input.
PAR	TS	**Parity:** This pin provides even parity across AD[31:0] and CBE[3:0]#. The CL-GD546X asserts correct parity when it drives the bus. The CL-GD546X does not check parity. Correct parity is asserted by the CL-GD546X (as a target) in the data phase of reads. For the CL-GD5464 as a bus master, correct parity is always provided in the address phase and for writes in the data phase.
IDSEL	I	**Initialization Device Select:** This input is a chip select in place of the upper 24 address bits during configuration read and write cycles.
INTA#	TS	**Interrupt Request #:** This active-low output indicates that the CL-GD546X has interrupt pending. See register CR11 for a description of the controls for this pin. This pin is functionally an open-drain output driver.
RD[7:0]	I/O	**ROM Data [7:0]:** These input pins accept data from the BIOS ROM, which is transferred to the PCI bus by AD[31:0]. These pins can also be configured as the data pins for the general-purpose I/O port. See Appendix B9 of the *CL-GD546X Technical Reference Manual*.
ROMCS#	O	**ROM Chip Select #:** This pin is an output to control the CS of the BIOS ROM. In addition, the level on this pin is sampled at the trailing edge of RST#. If this pin is tied low, the BIOS ROM decode is disabled. This pin is not 5-V tolerant, see Section 6.2 for additional information.
RA[15:0]	O	**ROM Address [15:0]:** These output pins are latched from the AD[31:0] bus, and are used to address the video system BIOS. These signals are connected directly to the corresponding address inputs of the BIOS ROM. Several of the RA lines are power-on configuration bits and may require pull-down resistors. See Appendix B9 of the *CL-GD546X Technical Reference Manual*.
PCS#	O	**Peripheral Chip Select #:** This output signal implements a general-purpose I/O port. See Appendix B9 of the *CL-GD546X Technical Reference Manual*.

Table 2-1. Host Interface — PCI Bus *(cont.)*

Name	Type	Description
PRDY	I	**Peripheral Ready:** This input implements a general-purpose I/O port. This signal allows the peripheral to extend the general-purpose I/O port cycle. See Appendix B9 of the *CL-GD546X Technical Reference Manual*.
GNT#	I	**Bus Grant #:** This active-low input indicates the arbiter has determined the CL-GD546X can become master of the PCI bus. This is not implemented on the CL-GD5462.
REQ#	O	**Bus Request #:** This active-low output requests mastership of the PCI the bus. This is not implemented on the CL-GD5462.

Table 2-3. General-Purpose I/O Port

Name	Type	Description
RD[7:0]	I/O	**ROM Data [7:0]:** These pins can be configured as the data pins for the general-purpose I/O port. See Appendix B9 of the *CL-GD546X Technical Reference Manual*.
RA[15:0]	O	**ROM Address [15:0]:** These pins can be configured to implement a general-purpose I/O port. The levels on RA[6:4] are latched at the rising edge of RST# to select the general-purpose I/O port type. See the description of the general-purpose I/O port in Appendix B9 of the *CL-GD546X Technical Reference Manual.*
PCS#	O	**Peripheral Chip Select #:** This output signal implements a general-purpose I/O port. See Appendix B9 of the *CL-GD546X Technical Reference Manual*.
PRDY	I	**Peripheral Ready:** This input implements a general-purpose I/O port. This signal allows the peripheral to extend the general-purpose I/O port cycle. See Appendix B9 of the *CL-GD546X Technical Reference Manual*.

Table 2-4. General-Purpose I/O Port Configuration

RA6 (Not CL-GD5462)	RA5	RA4	Configuration
1	X	1	Reserved
1	1	X	Reserved
1	0	0	8-bit (VMI Mode B)
0	1	1	Reserved
0	1	0	16-bit (VMI Mode B)
0	0	1	ATT® AV4400A
0	0	0	C-CUBE® CL-480 (VMI Mode A)

2.2 Rambus® Pins

The CL-GD5462 and CL-GD5464 have one Rambus Channel — Rambus Channel A. The pins for a Rambus Channel B are allocated, but not used on the CL-GD5462 or CL-GD5464.

The Rambus Channels must be designed properly for acceptable results. The trace routing, width, and spacing are all very important. Refer to Appendix B1 of the *CL-GD546X Technical Reference Manual* for Rambus Channel design information.

2.2.1 Rambus® Channel A

Table 2-5. Rambus® Channel A Pins

Name	Type	Description
RABCLK	O	**Rambus A Bus Clock:** This output is the clock source for Rambus Channel A. This output is programmable in the approximate range of 100 to 310 MHz. The nominal frequency is 250 MHz.
RAD[8:0]	I/O	**Rambus A Data [8:0]**: This is the bidirectional data bus for Rambus Channel A. These are low-swing signals as defined in the Rambus electrical specifications.
RARCLK	O	**Rambus A Receive Clock:** Data to the RDRAMS (request and write data packets) are aligned to this clock. This clock is used by the RDRAM to sample data it receives from the CL-GD546X.
RATCLK	I	**Rambus A Transmit Clock:** Data from the RDRAMS (read data and acknowledge packets) are aligned to this clock. This clock is transmitted by the RDRAM along with the data and used by the CL-GD546X to sample the data from the RDRAM.
RAC	I/O	**Rambus A Control:** This bidirectional pin is used to frame packets, to transmit part of the Rambus operation code, and to terminate transactions prematurely on Rambus Channel A. This is a low-swing signal as defined in the Rambus electrical specification.
RAE	O	**Rambus A Enable:** This output resets or enables the RDRAMs for Rambus Channel A. This is a low-swing signal as defined in the Rambus electrical specification.
RAVREF	I	**Rambus A Voltage Reference:** This is the logic threshold voltage for low-swing signals for Rambus Channel A.
CCTL	I/O	**Rambus Current Control Program:** This pin is used for the calibration of the RAC output current drivers for both channels. A resistor approximately the value of $1/2R_{TERM}$ must be connected between this pin and V_{TERM}.

2.2.2 Rambus® Channel B

The Rambus Channel B pins are not implemented on the CL-GD5462 or CL-GD5464 and are internally not connected to the pins (except SOUT, pin 179), but are reserved for future Laguna family members.

Table 2-6. Rambus® Channel B Pins

Name	Type	Description
RBBCLK	O	**Rambus B Bus Clock:** This output is the clock source for Rambus Channel B. This output is programmable in the approximate range of 100 to 310 MHz. The nominal output is 250 MHz.
RBD[8:0]	I/O	**Rambus B Data [8:0]**: This is the bidirectional data bus for Rambus Channel B. These are low-swing signals as defined in the Rambus electrical specification.
RBRCLK	O	**Rambus B Receive Clock:** Data to the RDRAMS (request and write data packets) are aligned to this clock. This clock is used by the RDRAM to sample data it receives from the CL-GD546X.
RBTCLK	I	**Rambus B Transmit Clock:** Data from the RDRAMS (read data and acknowledge packets) are aligned to this clock. This clock is transmitted by the RDRAM along with the data and used by the CL-GD546X to sample the data from the RDRAM.
RBC	I/O	**Rambus B Control:** This bidirectional pin is used to frame packets, to transmit part of the Rambus operation code, and to terminate transactions prematurely and Rambus Channel B. This is a low-swing signal as defined in the Rambus electrical specification.
RBE	O	**Rambus B Enable:** This output is used to reset or enable the RDRAMs for Rambus Channel B. This is a low-swing signal as defined in the Rambus electrical specification.
RBVREF	I	**Rambus B Voltage Reference:** This is the logic threshold voltage for low-swing signals for Rambus Channel B.
SOUT	O	**Rambus Serial Output:** This output initializes the RDRAMs in both Rambus Channels. It is used in performing refresh when the RDRAMs are in Power Down mode (this feature is not implemented in the CL-GD5464). This pin is not 5-V tolerant, see Section 6.2 for additional information.

2.3 Video Pins

Table 2-7. Video Pins

Name	Type	Description
RED	O	**Analog Red Video:** This analog output supplies current corresponding to the red value of the pixel being sent to the monitor. Each DAC output is typically terminated to monitor ground with a 75-Ω, 2-percent resistor. This resistor, in parallel with the 75-Ω resistor in the monitor, yields a 37.5-Ω impedance to ground.
GREEN	O	**Analog Green Video:** This analog output supplies current corresponding to the green value of the pixel being sent to the monitor. See the description of RED for information regarding the termination of this pin.
BLUE	O	**Analog Blue Video:** This analog output supplies current corresponding to the green value of the pixel being sent to the monitor. See the description of RED for information regarding the termination of this pin.
REXT	I	**DAC Current Set:** A resistor from this pin to DACVSS sets the full-scale current output of the DACs. The value of this resistor is typically 135 Ω. The following equation is derived in Appendix B5 of the *CL-GD546X Technical Reference Manual*. $$REXT = \frac{2.52\ V \bullet Load}{VFullScale}$$ **Equation 2-1**
IREF	I	**DAC Current Reference:** This pin is connected to a 0.1-µF capacitor that is returned to DACDVV. This capacitor stabilizes the internal DAC current reference.
HSYNC	I/O	**Horizontal Sync:** This output supplies the horizontal synchronization signal to the monitor. The polarity of this output is programmable. This pin is put into high-impedance when ESYNC# is low. This pin is an input for some configurations of the Enhanced V-Port.
VSYNC	I/O	**Vertical Sync:** This output supplies the vertical synchronization signal to the monitor. The polarity of this output is programmable. This pin is put into high-impedance when ESYNC# is low. This pin is an input for some configurations of the Enhanced V-Port.
CSYNC/ STEREO	TS	**Composite Sync:** This output supplies a composite synchronization signal to the monitor. CSYNC is the exclusive OR of HYSNC and VSYNC. This pin does not connect to the standard DB15 VGA connector. This pin can be configured to indicate the current STEREO frame.

2.4 Enhanced V-Port™ Pins

Table 2-8. Enhanced V-Port™ Pins

Name	Type	Description
P[23:8]	I	**Pixel Bus [23:8]:** These input pins are the extended pixel bus. P[7:0] correspond to the feature connector pixel bus.The extended pixel bus pins are always inputs and can be used to provide data to the frame buffer or drive data directly into the DACs. Several of the extended pixel bus pins are configurations inputs on the CL-GD5462 only. See Appendix B5 in the *CL-GD546X Technical Reference Manual*.
P[7:0]	I/O	**Pixel Bus [7:0]:** These bidirectional pins are the pixel bus. P[7:0] correspond to the feature connector pixel bus. In Feature Connector mode, if EVIDEO# is high, P[7:0] are outputs and reflect the least-significant byte of the pixel (whether it is an address into the palette or the actual color to the DACs); if EVIDEO# is low, P[7:0] are inputs and can be used to drive addresses into the RAMDAC or data directly into the DACs. In Video Capture mode, P[7:0] are inputs regardless of the state of EVIDEO#.
PRESENT#	I	**Present #:** This pin is used to indicate the presence of a video decoder and tristates all V-Port pins.
EDCLK#	I	**Enable Dot Clock #:** This input is used to the control the buffer on DCLK. In Feature Connector mode, if EDCLK# is high, DCLK is an output; if EDCLK# is low, DCLK is an input. In Video Capture mode, EVIDEO# is connected to the decoder's VREF (vertical reference) pin.
ESYNC#	I/O	**Enable Sync, and Blank #:** In Feature Connector mode, this input is used to control the buffers on HSYNC, VSYNC, and BLANK#; if ESYNC# is high, the controlled pins are outputs, and if ESYNC# is low, HSYNC and VSYNC are not driven. If ESYNC# is low, BLANK# is an input and controls the blank function of the integrated DACs. In Video Capture mode, ESYNC# becomes the VMI_ENABLE signal to enable output through a video decoder.
EVIDEO#	I	**Enable Video #:** This input is used to control the buffers on P[23:0]. If EVIDEO# is high, the Pixel Bus pins are outputs (some overlay modes can make the pixel bus inputs regardless of the level on EVIDEO#). If EVIDEO# is low, the Pixel Bus pins are inputs. When the CL-GD546X is configured to interface to the CL-PX4072 multi-standard decoder, EVIDEO# is connected to the CL-PX4072 VACT (video active) pin, and does not control the direction of the Pixel Bus pins.
BLANK#	I/O	**BLANK #:** In Feature Connector mode, the direction of this pin is controlled by ESYNC#; if ESYNC# is high, BLANK# is an output and its timing is controlled by the CRT controller logic, if ESYNC# is low, BLANK# is an input and controls the blank function of the integrated DACs. In Video Capture mode, EVIDEO# is connected to the decoder's HREF (horizontal reference) pin.
DCLK	I/O	**Dot Clock:** In Feature Connector mode, if EDCLK# is high, DCLK is an output and can be used to clock data on the pixel bus; if EDCLK# is low, DCLK is an input and is used to clock data into the DAC. In Video Capture mode, DCLK is an input regardless of the state of EDCLK# and is used to sample data on the P[23:0] pins.

2.5 I²C Bus Pins

Table 2-9. I²C Bus Pins

Name	Type	Description
SDA	I/O	**Serial Data:** This bidirectional pin is used for DDC2B data. It is normally connected to pin 12 of DB15 video connector. This pin has an internal pull-up, nominally 50 kΩ. The output is an open collector.
SCL	I/O	**Serial Clock:** This bidirectional pin is used for DDC2B clock. It is normally connected to pin 15 of video connector. This pin has an internal pull-up, nominally 50 kΩ. The output is an open collector.
SREQ#	I	**Serial Request:** This input can be used by a peripheral as a host interrupt. This pin is not implemented on the CL-GD546X.

2.6 Miscellaneous Pins

Table 2-10. Miscellaneous Pins

Name	Type	Description
RCLK	I	**14.31818-MHz Reference Clock:** This is the reference for the internal frequency synthesizers. Any deviation (long term or short term) from 14.31818 MHz is reflected in the synthesized frequencies. A crystal oscillator is recommended.

2.7 Power and Ground Pins

Table 2-11. Power and Ground Pins

Name	Type	Description
VDD[8:1]	PWR	**Digital Power [8:1]:** These eight pins supply power to the digital core and I/O logic. Each pin must be connected to the 3.3-V power plane and bypassed to GND with a 0.1-µF capacitor placed as close to the pin as possible.
GND[12:1]	GND	**Digital Ground [12:1]:** These 12 pins supply ground reference to the digital core and I/O logic. Each pin must be connected to the ground plane.
DACVDD[2:1]	PWR	**DAC Power [2:1]:** These two pins supply power to the integrated DACs. Each pin must be connected to the 3.3-V power plane and bypassed to DACGND with a 0.1-µF capacitor placed as close to the pin as possible.
DACGND[2:1]	GND	**DAC Ground [2:1]:** These two pins supply ground reference to the integrated DACs. Each pin must be connected to the DAC on the ground plane.
RAAVDD	PWR	**Rambus A Analog Power:** This pin supplies analog power to Rambus Channel A. This pin must be bypassed to RAAGND with a 10-µF capacitor in parallel with a 0.1-µF capacitor.
RAAGND	GND	**Rambus A Analog Ground:** This pin supplies analog ground to Rambus Channel A.

Table 2-11. Power and Ground Pins *(cont.)*

Name	Type	Description
RABVDD	PWR	**Rambus BCLK Power:** This pin supplies power to the internal driver that supplies the Rambus reference frequency to Channel B.
RABGND	GND	**Rambus A BCLK Ground:** This pin supplies ground to the RABCLK driver.
RAVDD[3:1]	PWR	**Rambus A Digital Power [3:1]:** These three pins supply power for the Rambus Channel A digital logic. Each pin must be bypassed to RAGND.
RAGND[7:1]	GND	**Rambus A Digital Ground [7:1]:** These seven pins supply ground reference to the Rambus Channel A digital logic.
RBAVDD	PWR	**Rambus B Analog Power:** This pin supplies analog power to Rambus Channel B. This pin must be bypassed to RBAGND with a 10-µF capacitor in parallel with a 0.1-µF capacitor.
RBAGND	GND	**Rambus B Analog Ground:** This pin supplies analog ground to Rambus Channel B.
RBBGND	GND	**Rambus BBCLK Ground:** This pin supplies ground to the RBBCLK driver.
RBVDD[3:1]	PWR	**Rambus B Digital Power [3:1]:** These three pins supply power for the Rambus Channel B digital logic. Each pin must be bypassed to RBGND with a 10-µF capacitor in parallel with a 0.1-µF capacitor.
RBGND[7:1]	GND	**Rambus B Digital Ground [7:1]:** These seven pins supply ground reference to the Rambus Channel B digital logic.
BVDD	PWR	**Rambus Synthesizer Power:** This pin supplies power to the Rambus BCLK synthesizer (common to both channels). This pin must be bypassed to BGND.
BGND	GND	**Rambus Synthesizer Ground:** This pin supplies ground reference to the Rambus BCLK synthesizer (common to both channels).
PVDD	PWR	**PCLK Synthesizer Power:** This pin supplies power to the pixel clock synthesizer. This pin must be bypassed to PGND.
PGND	GND	**PCLK Synthesizer Ground:** This pin supplies ground reference to the pixel clock synthesizer.