Extended I/O Registers

4

4.   EXTENDED I/O REGISTERS

The Extended I/O registers in the CL-GD546X are summarized in Table 4-1.

Table 4-1.   Extended I/O Registers Quick Reference

Register Name	PCI I/O Port	Index	MMI/O Offset	Page
PCI00: PCI Vendor ID	Conf 00h	–	300h	4-4
PCI02: PCI Device ID	Conf 02h	–	302h	4-5
PCI04: PCI Command	Conf 04h	–	304h	4-6
PCI06: PCI Status	Conf 06h	–	306h	4-8
PCI08: PCI Revision ID	Conf 08h	–	308h	4-9
PCI09: PCI Class Code	Conf 09h	–	309h	4-10
PCI0D: PCI Master Latency Timer (CL-GD5464 only)	Conf 0Dh	–	30Dh	4-11
PCI0E: PCI Header Type	Conf 0Eh	–	30Eh	4-12
PCI10: PCI MMI/O Base Address	Conf 10h	–	310h	4-13
PCI14: PCI Frame Buffer Base Address	Conf 14h	–	314h	4-14
PCI2C: PCI Subsystem Vendor ID	Conf 2Ch	–	32Ch	4-15
PCI2E: PCI Subsystem ID	Conf 2Eh	–	32Eh	4-16
PCI30: PCI Expansion ROM Base Address	Conf 30h	–	330h	4-17
PCI3C: PCI Interrupt Line	Conf 3Ch	–	33Ch	4-18
PCI3D: PCI Interrupt Pin	Conf 3Dh	–	33Dh	4-19
PCIF8: PCI VGA Shadow	Conf F8h	–	3F8h	4-20
PCIFC: PCI Vendor Specific Control	Conf FCh	–	3FCh	4-21
SR6: Unlock I/O Extension	3C5h	06h	–	4-24
SR7: Extended Sequencer Mode	3C5h	07h	–	4-25
SR9, SRA, SR14, SR15: Scratch Pad 0, 1, 2, 3	3C5h	09h, 0Ah, 14h, 15h	–	4-26
SR0B, SR0C, SR0D, SR0E: Denominator and Post-Scalar	3C5h	0Bh, 0Ch, 0Dh, 0Eh	84h (SR0E)	4-27
SR18: Signature Generator Control	3C5h	18h	90h	4-28
SR19, SR1A: Signature Generator Result	3C5h	19h, 1Ah	94h, 98h	4-30
SR1B, SR1C, SR1D, SR1E: VCLK 0, 1, 2, 3 Numerator	3C5h	1Bh, 1Ch, 1Dh, 1Eh	88h (SR1E)	4-31
GR9: Offset Register 0	3CFh	09h	–	4-32

Table 4-1. Extended I/O Registers Quick Reference *(cont.)*

Register Name	PCI I/O Port	Index	MMI/O Offset	Page
GRA: Offset Register 1	3CFh	0Ah	–	4-33
GRB: Graphics Mode Extensions	3CFh	0Bh	–	4-34
CR19: CRTC Interlace End	3?5h[a]	19h	64h	4-35
CR1A: CRTC Miscellaneous Control	3?5h	1Ah	68h	4-36
CR1B: CRTC Extended Display Control	3?5h	1Bh	6Ch	4-37
CR1D: CRTC Screen Start A Extension	3?5h	1Dh	74h	4-39
CR1E: CRTC Timing Overflow	3?5h	1Eh	78h	4-40
CSL: Current Scanline (CL-GD5464 only)	–	–	140h	4-41
CSLC: Current Scanline Comparison (CL-GD5464 only)	–	–	142h	4-42
SSA: Secondary Start Address (CL-GD5464 only)	–	–	144h	4-43
Multi-Buffering Control (CL-GD5464 only)	–	–	148h	4-44
TLUT_LOAD (CL-GD5464 only)	–	–	9Ch	4-45

[a] '?' in the above register addresses is 'B' in Monochrome mode and 'D' in Color mode.

4.1   PCI00: PCI Vendor ID Register

I/O Port Address: PCI	Configuration 00h
Index	–
Size (bits):	16
MMI/O Offset	300h
Access Type	Read only

Bit	Description	Reset Value
15:13	Vendor ID [15:13]	0
12	Vendor ID [12]	1
11:5	Vendor ID [11:5]	0
4	Vendor ID [4]	1
3:2	Vendor ID [3:2]	0
1:0	Vendor ID [1:0]	1

This is the vendor ID required for PCI compliance.

Bit	Description
15:0	**Vendor ID [15:0]:** This read-only field contains the vendor ID assigned to Cirrus Logic. The value returned is '1013h'.

4.2   PCI02: PCI Device ID Register

I/O Port Address: PCI	Configuration 02h
Index	–
Size (bits):	16
MMI/O Offset	302h
Access Type	Read only

Bit	Description	Reset Value
15:8	Device ID [15:8]	0
7:6	Device ID [7:6]	1
5	Device ID [5]	0
4	Device ID [4]	1
3	Device ID [3]	0
2	Device ID [2]	X
1:0	Device ID [1]	0
0	Device ID [0]	0

This is the device ID required for PCI compliance.

Bit	Description
15:0	**Device ID [15:0]:** This read-only field contains the device ID assigned to the specific member of the CL-GD546X family. The value returned for the CL-GD5462 is 'D0h'. The value returned for the CL-GD5464 is 'D4h'.

4.3   PCI04: PCI Command Register

I/O Port Address: PCI	Configuration 04h
Index	–
Size (bits):	16
MMI/O Offset	304h
Access Type	Read/Write

Bit	Description	Reset Value
15:10	Reserved	0
9	Bus Master Fast Back-to-Back Capable	0
8:6	Reserved	0
5	VGA Palette Snooping	0
4:3	Reserved	0
2	Bus Master Enable	0
1	Enable Memory Accesses	0
0	Enable I/O Accesses	0

This is the PCI Command register.

Bit	Description
15:10	**Reserved:** These bits are reserved and *must* be programmed to '0'.
9	**Bus Master Fast Back-to-back Capable (CL-GD5464 only):** This bit is always '0' indicating that as a PCI bus master the CL-GD5464 is not capable of fast back-to-back cycles.
8:6	**Reserved**: These bits are reserved and *must* be programmed to '0'.
5	**VGA Palette Snooping:** This bit controls the response of CL-GD546X to VGA palette write cycles (writes to I/O addresses 3C6h–3C9h) when not in VGA mode. If this bit is '1', CL-GD546X does not activate DEVSEL#. When it detects that the cycle is complete, it latches the data. It responds normally to read cycles. If this bit is '0', CL-GD546X ignores palette writes.
4:3	**Reserved:** These bits are reserved and *must* be programmed to '0'.

4.3   PCI04: PCI Command Register *(cont.)*

Bit	Description
2	**Bus Master Enable (CL-GD5464 only):** If set to '1', enables the CL-GD5464 as a PCI bus master.
1	**Enable Memory Accesses:** If this bit is programmed to '1', memory accesses are enabled on the CL-GD546X. If this bit is programmed to '0', memory accesses are not enabled on the CL-GD546X. Memory-mapped I/O access is controlled with this bit.
0	**Enable I/O Accesses:** If this bit is programmed to '1', I/O accesses are enabled on the CL-GD546X. If this bit is programmed to '0', I/O accesses are not enabled on the CL-GD546X. Configuration accesses are always enabled.

4.4   PCI06: PCI Status Register

I/O Port Address: PCI	Configuration 06h
Index	–
Size (bits):	16
MMI/O Offset	306h
Access Type	Read/Write

Bit	Description	Reset State
15:14	Reserved	0
13	Bus Master Master-Abort	0
12	Bus Master Target-Abort	0
11	Bus Slave Target-Abort	0
10:9	DEVSEL# Timing [1:0]	0
8	Reserved	0
7	Fast Back	1
6:0	Reserved	0

This is the PCI Status register.

Bit	Description
15:14	**Reserved**
13	**Bus Master Master-Abort (CL-GD5464 only):** This bit is set to '1' by CL-GD546X whenever, as a PCI bus master, it terminates a transaction with a master-abort.
12	**Bus Master Target-Abort (CL-GD5464 only):** This bit is set to '1' by CL-GD546X whenever, as a PCI bus master, it terminates a transaction with a target-abort.
11	**Bus Slave Target-Abort:** This bit is set to '1' by CL-GD546X whenever it terminates a transaction with a target-abort. This bit is cleared by writing '1' to it.
10:9	**DEVSEL# Timing [1:0]:** This read-only field always returns the value '00' to indicate fast DEVSEL# timing.
8	**Reserved**
7	**Fast Back:** This read-only bit returns '1', indicating CL-GD546X is capable of accepting fast back-to-back transactions when it is not the target of both transactions.
6:0	**Reserved**

4.5   PCI08: PCI Revision ID Register

I/O Port Address: PCI   Configuration 08h

Index   –

Size (bits):   8

MMI/O Offset   308h

Access Type   Read only

Bit	Description	Reset Value
7:0	Revision ID [7:0]	X

This register contains the revision status for the device.

Bit	Description
7:0	**Revision ID [7:0]:** This read-only field contains the revision ID assigned by Cirrus Logic. No application program should ever take any action based on the contents of this field.

4.6   PCI09: PCI Class Code Register

I/O Port Address: PCI	Configuration 09h
Index	–
Size (bits):	24
MMI/O Offset	309h
Access Type	Read only

Bit	Description	Reset Value
23:18	Base-Class Code [7:2]	0
17	Base-Class Code [1]	1
16	Base-Class Code [0]	1
15	Sub-Class Code [7]	X
14:8	Sub-Class Code [6:0]	0
7:0	Programming Interface [7:0]	0

This register contains the class code that identifies the type of CL-GD546X device.

Bit	Description
23:16	**Base-Class Code [7:0]:** This field returns the value '03h' for a display device.
15:8	**Sub-Class Code [7:0]:** This field returns the value '00h' for VGA-compatible controller, if RA3 (P18 on the CL-GD5462) has no configuration pull-down resistor. This field returns the value '80h' for other display controller, if RA3 (P18 on the CL-GD5462) has a configuration pull-down resistor. See Appendix B5, "Pin Scan".
7:0	**Programming Interface [7:0]:** This field returns the value '00h'.

4.7   PCI0D: PCI Master Latency Timer Register (CL-GD5464 only)

I/O Port Address: PCI	Configuration 0Dh
Index	–
Size (bits):	8
MMI/O Offset	30Dh
Access Type	Read/Write

Bit	Description	Reset Value
7:3	Latency Timer [7:3]	0
2:0	Reserved	0

This register specifies the latency timer value in PCI bus clocks. This register is written when enabling the CL-GD5464 as a PCI bus master.

Bit	Description
7:3	**Latency Timer [7:3]**
2:0	**Reserved**

4.8   PCI0E: PCI Header Type Register

I/O Port Address: PCI	Configuration 0Eh
Index	–
Size (bits):	8
MMI/O Offset	30Eh
Access Type	Read only

Bit	Description	Reset Value
7:0	Header Type [7:0]	0

This read-only register always returns the value '00h'.

Bit	Description
7:0	**Header Type [7:0]:** This field returns the value '00h'.

4.9   PCI10: PCI MMI/O Base Address Register

I/O Port Address: PCI	Configuration 10h
Index	–
Size (bits):	32
MMI/O Offset	310h
Access Type	Read/Write

Bit	Description	Reset Value
31:15	MMI/O Base Address [31:15]	0
14:4	Reserved	0
3	Prefetchable	0
2:1	Type [1:0]	0
0	Memory/IO Indicator	0

This register defines the base address for the CL-GD546X Memory-Mapped I/O registers. The register is sized to reserve a 32-Kbyte space.

Bit	Description
31:15	**MMI/O Base Address [31:15]:** Configure this read/write field to the base address of the Memory-Mapped I/O registers. Thirty-two Kbytes are addressable, as two sets of four byte-swapping apertures.
14:4	**Reserved:** Reads back as '0'.
3	**Prefetchable:** This bit always read as '0' to indicate the registers are not prefetchable.
2:1	**Type [1:0]:** This field returns '00b' to indicate that the MMI/O register mapping can be done anywhere in the 32-bit memory space.
0	**Memory/IO Indicator:** This read-only field indicates the type of address space requested. A '0' value indicates memory.

4.10 PCI14: PCI Frame Buffer Base Address Register

I/O Port Address: PCI	Configuration 14h
Index	–
Size (bits):	32
MMI/O Offset	314h
Access Type	Read/Write

Bit	Description	Reset Value
31:25	Frame Buffer Base Address [31:25]	0
24:4	Reserved	0
3	Prefetchable	0
2:1	Type [1:0]	0
0	Memory/IO Indicator	0

This register defines the base address for the CL-GD546X frame buffer. The register is sized to reserve a 32-Mbyte space.

Bit	Description
31:25	**Frame Buffer Base Address [31:25]:** Configure this read/write field to the base address of the frame buffer. Thirty-two Mbytes are addressable, as two sets of four byte-swapping apertures.
24:4	**Reserved**
3	**Prefetchable:** This bit always reads as '0' to indicate the frame buffer is not prefetchable.
2:1	**Type [1:0]:** This field returns '00b', indicating the frame buffer mapping can be anywhere in the 32-bit address space.
0	**Memory/IO Indicator:** This read-only field indicates the type of address space requested. A '0' value indicates memory.

4.11   PCI2C: PCI Subsystem Vendor ID Register

I/O Port Address: PCI   Configuration 2Ch
Index   –
Size (bits):   16
MMI/O Offset   32Ch
Access Type   Read only

Bit	Description
15:0	Subsystem Vendor ID [15:0]

This register, in conjunction with the Subsystem ID register, uniquely identifies the adapter card containing the CL-GD546X device.

Bit	Description
15:0	**Subsystem Vendor ID [15:0]:** This read-only field returns the value read from BIOS ROM locations, 7FF8h and 7FF9h. If no ROM is used (ROMCS# pin tied to ground), this register returns the value '0000h', indicating that this register is not implemented. This is appropriate if CL-GD546X is installed on the motherboard.
	This field identifies the vendor of the adapter card containing the CL-GD546X. It provides a method for adapter card vendors to distinguish their cards from one another even though they have the CL-GD546X devices in common. This is necessary, for example, to ensure the correct drivers are loaded when replacing cards.

4.12 PCI2E: PCI Subsystem ID Register

I/O Port Address: PCI	Configuration 2Eh
Index	–
Size (bits):	16
MMI/O Offset	32Eh
Access Type	Read only

Bit	Description
15:0	Subsystem ID [15:0]

This register, in conjunction with the Subsystem Vendor ID register, uniquely identifies the adapter card containing the CL-GD546X device.

Bit	Description
15:0	**Subsystem ID [15:0]:** This read-only field returns the value read from BIOS ROM locations, 7FFAh and 7FF8h. If no ROM is used (ROMCS# pin tied to ground), this register returns the value '0000h', indicating that this register is not implemented. This is appropriate if the CL-GD546X is installed on the motherboard.
	This field identifies the vendor of the adapter card containing the CL-GD546X. It provides a method for adapter card vendors to distinguish their cards from one another even though they have the CL-GD546X devices in common. This is necessary, for example, to ensure the correct drivers are loaded when replacing cards.

4.13   PCI30: PCI Expansion ROM Base Address Enable Register

I/O Port Address: PCI	Configuration 30h
Index	–
Size (bits):	32
MMI/O Offset	330h
Access Type	Read/Write

Bit	Description	Reset Value (PCI)
31:15	Expansion ROM Base Address [31:15]	0
14:1	Reserved	0
0	ROMCS# Enable	0

This 32-bit register defines the base address of the CL-GD546X expansion ROM.

Bit	Description
31:15	**Expansion ROM Base Address [31:15]:** This 17-bit field is programmed to the base address of the 32-Kbyte BIOS ROM.
14:1	**Reserved**
0	**ROMCS# Enable:** When this bit is programmed to '1' and PCI Command bit 1 is programmed to '1', the CL-GD546X responds to BIOS ROM accesses. When either of these two bits is programmed to '0', the CL-GD546X does not respond to BIOS ROM accesses.

4.14 PCI3C: PCI Interrupt Line Register

I/O Port Address: PCI	Configuration 3Ch
Index	–
Size (bits):	8
MMI/O Offset	33Ch
Access Type	Read/Write

Bit	Description	Reset Value
7:0	PCI Interrupt Line [7:0]	INTA# Strap

The value in this register indicates which interrupt request line (if any) is used by the CL-GD546X.

Bit	Description
7:0	**PCI Interrupt Line [7:0]:** If no configuration pull-down resistor is installed on the INTA# pin, this is a read/write register. At reset, this register is set to 'FFh' to indicate that the CL-GD546X is not claiming any interrupt line. The configuration software can program this register to '02h' to allow the CL-GD546X to use Interrupt 2 for compatibility with some VGA programs.
	If a configuration pull-down resistor is installed on the INTA# pin, this is a read-only register that always returns the value '00h'. In this case, no interrupt pin can be claimed by the CL-GD546X.

4.15 PCI3D: PCI Interrupt Pin Register

I/O Port Address: PCI	Configuration 3Dh
Index	–
Size (bits):	8
MMI/O Offset	33Dh
Access Type	Read only

Bit	Description	Reset Value
7:1	Interrupt Pin [7:1]	0
0	Interrupt Pin [0]	INTA#

This register indicates whether the CL-GD546X is configured to claim an Interrupt pin.

Bit	Description
15:8	**Interrupt Pin [7:0]:** If a pull-down configuration resistor is installed on INTA# pin, this register returns the value '00h', indicating that an interrupt is not being used. If INTA# pin is pulled up (this is the case if it is connected to INTA# pin on the motherboard), this register returns the value '01h', indicating that the CL-GD546X V-Port uses PCI Interrupt A.

4.16 PCIF8: PCI VGA Shadow Register

I/O Port Address: PCI	Configuration F8h
Index	–
Size (bits):	32
MMI/O Offset	3F8h
Access Type	Read/Write

Bit	Description	Reset Value
31:13	Reserved	0
12	VGA_GCI6	0
11:10	VGA_MM[1:0]	0
9	VGA_DSPL_MEM_EN	0
8	CRTC_ADRS	0
7:0	Reserved	0

This register contains copies of various register bits in the VGA device. They are updated as the corresponding VGA registers are written. This register can be written directly, but there is normally no need for it.

Bit	Description
31:13	**Reserved**
12	**VGA_GCI6:** When the value in the VGA Graphics Controller index is '06h' (3CEh), '1' is returned in this bit position. When the value is anything other than '06h', '0' is returned.
11:10	**VGA_MM[1:0]:** This field is a copy of the Memory Map field contained in GR6[3:2] (3CFh, index 06h).
9	**VGA_DSPL_MEM_EN:** This bit is a copy of the Enable Display Memory bit in MISC[1] (3C2h).
8	**CRTC_ADRS:** This bit is a copy of the CRTC I/O Address bit in MISC[0] (3C2h).
7:0	**Reserved**

4.17 PCIFC: PCI Vendor Specific Control Register

I/O Port Address: PCI	Configuration FCh
Index	–
Size (bits):	32
MMI/O Offset	3FCh
Access Type	Read/Write

Bit	**Description**	**Reset State**
31:29	Reserved	100
28	EXT_DISP	X
27:26	Reserved	00
25	SW_RESET	0
24	RABCLK_EN	1
23	TQFREE[3]	0
22:20	TQFREE[2:0]	1
19:18	Reserved	11
17	AD_CTRL	0
16	QUEUE_FLUSH	0
15	Reserved	00
14	TD_BRST_EN	0
13	FB_BRST_EN	1
12	HD_BRST_EN	1
11	Reserved	0
10	RETRY_EN	1
9	BRST_WS [1]	0
8	BRST_WS [0]	0
7:6	RAC_TX_LD[1:0]	1
5	RAC_RX_LD[1]	0
4	RAC_RX_LD[0]	1
3:1	Reserved	100
0	MEM_CFG_RSP	0

This register contains vendor-specific controls used for optimizing and controlling the host interface. No application program should ever write to this register.

Bit	**Description**
31:29	**Reserved**
28	**EXT_DISP:** If this bit is programmed to '1', Extended Display modes are enabled. If this bit is programmed to '0', standard IBM VGA Display modes are enabled.
27:26	**Reserved**
25	**SW_RESET:** If this bit is '1', the CL-GD546X is reset, but does not reload the configuration options. If this bit is '0', the CL-GD546X operates normally.
24	**RABCLK_EN:** If this bit is '1', it enables the RABCLK output driver. If this bit is '0', it disables the output driver and powers down the RABCLK PLL.
23:20	**TQFREE[3:0]:** This read-only field returns the number of entries available in the host interface transaction queue.

4.17   PCIFC: PCI Vendor Specific Control Register *(cont.)*

Bit	Description
19:18	**Reserved**
17	**AD_CTRL:** If this bit is programmed to '0', read data is driven onto the PCI bus asynchronous to the PCI clock. If this bit is programmed to '1', read data is driven onto the bus synchronous to the PCI clock when TRDY* is asserted.
16	**QUEUE_FLUSH (CL-GD5464 only):** If this bit is programmed to '1', the host interface read and transaction queues are reset (all entries are removed). If this bit is programmed to '0', the host interface transaction queue operates normally. This bit is reserved on the CL-GD5462.
15	**Reserved**
14	**TD_BRST_EN:** If this bit is programmed to '1', PCI bus burst write attempts to the HDATA_3D (coprocessor indirect port) at address 0x4800 are enabled and occur normally. If this bit is programmed to '0', PCI bus burst write attemps to the HDATA_3D port are broken into single PCI write cycles. The CL-GD546X assert the STOP# signal to cause a target disconnect. The CL-GD5464 does not permit burst to this address range. This bit is set to '0' at reset.
13	**FB_BRST_EN:** If this bit is programmed to '1', PCI bus burst attempts to the frame buffer are enabled and occur normally. If this bit is programmed '0', PCI bus burst attempts to the frame buffer are broken into single transactions. The CL-GD546X asserts the STOP# signal to cause a target disconnect. This effectively disables bursts to the frame buffer.
12	**HD_BRST_EN:** If this bit is programmed to '1', PCI bus burst attempts to the 2D-engine host data addresses are enabled and occur normally. If this bit is programmed '0', PCI bus burst attempts to the 2D-engine host data addresses are broken into single transactions. The CL-GD546X asserts the STOP# signal to cause a target disconnect. This effectively disables bursts to the 2D-engine host data.
11	**Reserved**
10	**RETRY_EN:** If this bit is programmed to '1', no more than 16-wait states are inserted into a PCI bus transaction before a retry occurs. If this bit is programmed to '0', wait states are inserted when it is necessary for completion of the transaction. No retry is ever done.
9:8	**BRST_WS [1:0]:** This two-bit field controls the number of wait states inserted between burst write data cycles on the PCI bus.

BRST_WS	Wait States
00b	0
01b	1
10b	2
11b	3

4.17   PCIFC: PCI Vendor Specific Control Register *(cont.)*

Bit	Description

| 7:6 | **RAC_TX_LD[1:0] (CL-GD5464 only):** This two-bit field determines on which BCLK phase the parallel data is loaded for transmission on the serial Rambus channel. These bits are decoded to drive RAC inputs BC_SEL[1:0], BE_SEL[1:0], and BD_SEL[3:0] according to the table below: |

RAC_TX_LD[1:0]	Bx_SEL[3:0]
00	0001
01	0010
10	0100
11	1000

| 5:4 | **RAC_RX_LD[1:0] (CL-GD5464 only):** This two-bit field determines on which BCLK phase the received serial Rambus data is loaded and available in parallel form. These bits are decoded to drive RAC inputs RC_SEL[3:0] and RD_SEL[3:0] according to the table below: |

RAC_RX_LD[1:0]	Rx_SEL[3:0]
00	0001
01	0010
10	0100
11	1000

Bit	Description
3:1	**Reserved**
0	**MEM_CFG_RSP:** If this bit is programmed to '0', the Configuration registers are not accessible in memory space. When this bit is programmed to '1', the Configuration registers are accessible in memory space. The reset state of this bit is '0'.

4.18   SR6: Unlock I/O Extensions Register

I/O Port Address: PCI	3C5h
Index	06h
Size (bits):	8
MMI/O Offset	–
Access Type	Read only

Bit	Description	Reset State
7:5	Extensions Register Access Value	0
4	Extensions Register Access Value	1
3:2	Extensions Register Access Value	0
1	Extensions Register Access Value	1
0	Extensions Register Access Value	0

This register provides compatibility with programs that use SR6 to identify Cirrus Logic products.

Bit	Description
7:0	**Extensions Register Access Value:** This read-only field returns the value '12h'.

4.19 SR7: Extended Sequencer Mode Register

I/O Port Address: PCI	3C5h
Index	07h
Size (bits):	8
MMI/O Offset	–
Access Type	Read/Write

Bit	Description	Reset State
7:1	Reserved	
0	8-bpp Packed Pixel	0

This register selects 8-bpp Packed-Pixel modes.

Bit	Description
7:1	**Reserved**
0	**8-bpp Packed Pixel:** If this bit is programmed to '1', 8-bpp (256 color) Packed-Pixel modes are enabled. For the VGA aperture, these are true Packed-Pixel modes in which consecutive pixels on the screen are stored consecutively in memory. If this bit is programmed to '0', Mode 13h or Mode X 8-bpp addressing is used. Chain-4 mode is used and consecutive pixels are stored at every fourth byte in the frame buffer.

4.20   SR9, SRA, SR14, SR15: Scratch Pad 0, 1, 2, 3 Registers

I/O Port Address: PCI	3C5h
Index	09h, 0Ah, 14h, 15h
Size (bits):	8
MMI/O Offset	–
Access Type	Read/Write

Bit   **Description**

7:0   R/W Data [7:0]

These four registers are reserved for the exclusive use of the CL-GD546X BIOS, and must never
be written to by any application program. This register description is included for completeness
only.

Bit	Description
7:0	**R/W Data [7:0]:** These bits are reserved for the Cirrus Logic BIOS.

4.21 SR0B, SR0C, SR0D, SR0E: Denominator and Post-Scalar Registers

I/O Port Address: PCI	3C5h
Index	0Bh, 0Ch, 0Dh, 0Eh
Size (bits):	8
MMI/O Offset	84h (SR0E)
Access Type	Read/Write

Bit	Description
7:1	VCLK Denominator [6:0]
0	VCLK Post-Scalar (÷2)

These registers, in conjunction with SR1B–SR1E, program the frequency of video clocks 0 (VCLK0) through 3 (VCLK3). The reset values for these four registers are in the VCLK Numerator description located on . Registers SRE and SR1E are accessible using MMI/O offset address.

Bit	Description
7:1	**VCLK Denominator [6:0]:** This seven-bit field is the denominator for the VCLK synthesizer.
0	**VCLK Post-Scalar (÷2):** If this bit is programmed to '1', the output of the synthesizer is divided by two. If this bit is programmed to '0', the output of the synthesizer is used without being divided by two.

4.22 SR18: Signature Generator Control Register

I/O Port Address: PCI	3C5h
Index	18h
Size (bits):	8
MMI/O Offset	90h
Access Type	Read/Write

Bit	Description
7:6	Byte Select [1:0]
5	Enable Data Generator
4:2	Bit Select [2:0]
1	Reset Signature Generator
0	Signature Generator Enable/Status

This register controls and monitors the status of the signature generator. The CL-GD546X signature generator does board-level testing of the video subsystem. Refer to Appendix B6, "Manufacturing Test", for a complete description of the signature generator, including sample code.

Bit	Description
7:6	**Byte Select [1:0]:** This two-bit field selects the byte in the video pipeline, which is tested. See the description of bits 4:2.
5	**Enable Data Generator:** If this bit is set to '1', pseudo-random data is placed on the memory data bus. This is used in conjunction with the signature generator. This mode is intended for factory testing only.
4:2	**Bit Select [2:0]:** This field is used to select the bit of the pixel bus that is used as the input for the signature generator according to the following table:

4:2	7:6 = 11	7:6 = 10	7:6 = 01
000b	P[0]	P[8]	P[16]
001b	P[1]	P[9]	P[17]
010b	P[2]	P[10]	P[18]
011b	P[3]	P[11]	P[19]
100b	P[4]	P[12]	P[20]
101b	P[5]	P[13]	P[21]
110b	P[6]	P[14]	P[22]
111b	P[7]	P[15]	P[23]

4.22   SR18: Signature Generator Control Register *(cont.)*

Bit	Description
1	**Reset Signature Generator:** When this bit is set to '1', the signature generator is reset to an initially defined condition. When this bit is set to '0', the signature generator is allowed to run under the control of SR18[0].
0	**Signature Generator Enable/Status:** When this bit is set to '1', the signature generator begins operation on the next VSYNC. It accumulates a signature from the Pixel Bus bit selected by SR18[7:6] and SR18[4:2] for one video frame and stops forcing this bit to '0'. By monitoring this bit, the program can determine when the signature is complete.

4.23   SR19, SR1A: Signature Generator Result Registers

I/O Port Address: PCI	3C5h
Index	19h, 1Ah
Size (bits):	8
MMI/O Offset	94h, 98h
Access Type	Read only

Bit	Description	Reset State
7:0	Signature Generator Result [7:0]	0

These two registers read the signature generator result. The least-significant byte is read from SR19. The most-significant byte is read from SR1A. The CL-GD546X signature generator board-level tests the video subsystem.

Bit	Description
7:0	**Signature Generator Result [7:0]**

4.24   SR1B, SR1C, SR1D, SR1E: VCLK 0, 1, 2, 3 Numerator Registers

I/O Port Address: PCI	3C5h
Index	1Bh, 1Ch, 1Dh, 1Eh
Size (bits):	8
MMI/O Offset	88h (SR1E)
Access Type	Read/Write

Bit	**Description**
7	Use MCLK (SR1E)
6:0	VCLK Numerator [6:0]

These registers, in conjunction with SR0B–SR0E, determine the frequency of the video clocks. Refer to the *Laguna VisualMedia™ Accelerators Family — CL-GD546X Volume II (Software Reference Manual, Second Edition, September 1996)*, "Programmer's Guide" chapter for complete programming information. Registers SRE and SR1E (VCLK3) are accessible using MMI/O offset address.

Bit	**Description**
7	**Use MCLK (SR1E):** For SR1E only, if this bit is programmed to '1', VCLK is driven by MCLK. This mode is intended for factory testing only. This bit is reserved on SR1B, SR1C, and SR1D.
6:0	**VCLK Numerator [6:0]:** The following table shows the values these registers are loaded at RESET time:

Clock	Freq. (MHz)	N	D	P	Numerator	Denominator/ Post-Scalar
VCLK0	25.180	102	29	1	66h	3Bh
VCLK1	28.325	91	23	1	5Bh	2Fh
VCLK2	41.165	69	24	0	45h	30h
VCLK3	36.082	126	25	1	7Eh	33h

4.25 GR9: Offset Register 0

I/O Port Address: PCI	3CFh
Index	09h
Size (bits):	8
MMI/O Offset	–
Access Type	Read/Write

Bit	Description
7:0	Offset 0 [7:0]

This register provides access to up to 1 Mbyte of display memory with 4-Kbytes granularity. The contents of this register are added to A[19:12] when Extension register GRB[0] is set to '0', or when GRB[0] is set to '1' and SA15 is '0'.

Prior to being modified by address-wrap controls, the Display Memory Address is called XMA. It is the sum of XA and an Offset register. XA is the address on the bus with bits 16 and 15 possibly forced to '0' as indicated in the following table:

Configuration	XA[16]	XA[15]	XA[14:0]
64K memory: GR6[3:2] = 0, 1 **and** Offset 1 disabled: GRB[0] = 0	0	SA[15]	SA[14:0]
64K memory: GR6[3:2] = 0,1 **or** Offset 1 enabled: GRB[0] = 1	0	0	SA[14:0]

The XA address is summed with the contents of an Offset register with the relative alignment indicated below.

0	0	0	XA[16]	XA[15]	SA[14]	SA[13]	SA[12]
+OFF[7]	OFF[6]	OFF[5]	OFF[4]	OFF[3]	OFF[2]	OFF[1]	OFF[0]
XMA[19]	XMA[18]	XMA[17]	XMA[16]	XMA[15]	XMA[14]	XMA[13]	XMA[12]

Bit	Description
7:0	**Offset 0 [7:0]:** This value is added to A[19:12] to provide the address into display memory. This Offset register is selected when GRB[0] is set to '0', or when GRB[0] is '1' and SA15 is '0'.

4.26   GRA: Offset Register 1

I/O Port Address: PCI	3CFh
Index	0Ah
Size (bits):	8
MMI/O Offset	–
Access Type	Read/Write

Bit　　　　**Description**

7:0　　　　　Offset 1 [7:0]

This register provides access to up to 1 Mbyte of display memory with 4-Kbytes granularity. The contents of this register are added to A[19:12] when Extension register GRB[0] is set to '1' and SA15 is '1'.

This provides an additional 32-Kbyte window into 1 Mbyte of display memory with 4-Kbytes granularity.

Bit	Description
7:0	**Offset 1 [7:0]:** This value is added to A[19:12] to provide the address into display memory. This Offset register is selected when GRB[0] is set to '1', and SA15 is '1'. If GRB[0] is set to '0', this register is unused.

4.27 GRB: Graphics Controller Mode Extensions Register

I/O Port Address: PCI	3CFh
Index	0Bh
Size (bits):	8
MMI/O Offset	–
Access Type	Read/Write

Bit	Description
7:1	Reserved
0	Enable Offset Register 1

This register enables or disables the second Offset register.

Bit	Description
7:1	**Reserved**
0	**Enable Offset Register 1:** If this bit is set to '1', then SA15 selects between Offset registers 0 and 1. If this bit is set to '0', Offset register 0 is always selected, regardless of the value of SA15.

4.28   CR19: CRTC Interlace End Register

I/O Port Address: PCI	3?5h
Index	19h
Size (bits):	8
MMI/O Offset	64h
Access Type	Read/Write

Bit	Description
7:0	Interlace End [7:0]

This register positions scanlines in the odd field so that they are halfway between scanline in the even field.

Bit	Description
7:0	**Interlace End [7:0]:** This value is the number of characters in the last scanline of the odd field in interlaced timing. This can be adjusted to center the scanlines in the odd field halfway between scanlines in the even field. This register is typically set to approximately half the horizontal total.

NOTE: '?' in the above register addresses is 'B' in monochrome mode and 'D' in color mode.

4.29 CR1A: CRTC Miscellaneous Control Register

I/O Port Address: PCI	3?5h
Index	1Ah
Size (bits):	8
MMI/O Offset	68h
Access Type	Read/Write

Bit	Description
7:6	Vertical Blank End Overflow [9:8]
5:4	Horizontal Blank End [7:6]
3	Static HSYNC
2	Static VSYNC
1	Enable Double Buffered Display Start Address
0	Enable Interlaced

This register contains timing overflow bits as well as some miscellaneous control bits.

Bit	Description
7:6	**Vertical Blank End Overflow [9:8]:** This two-bit field extends the vertical blank end value to 10 bits. Refer to Chapter 3, "VGA Core Registers", Table 3-2 on page 3-24 for the description of register CR0 and a table containing all the timing value bits. When CR1B[5] is set to '1', or if CR1B[7] is set to '1', these bits are enabled.
5:4	**Horizontal Blank End Overflow [7:6]:** This two-bit field extends the horizontal blanking end value to eight bits. Refer to Chapter 3, "VGA Core Registers", Table 3-2 on page 3-24 for the description of register CR0 and a table containing all the timing value bits. If CR1B[5] is set to '1', or if CR1B[7] is set to '1', these bits are enabled.
3	**Static HSYNC:** If this bit is programmed to '1', HSYNC is forced to '0'. The RAM-DAC is powered down if this bit is set to '1'. If this bit is programmed to '0', HSYNC is controlled by the CRTC timing logic normally. If both HSYNC and VSYNC are set to '1', VCO is also powered down.
2	**Static VSYNC:** If this bit is programmed to '1', VSYNC is forced to '0'. The RAM-DAC is powered down if this bit is set to '1'. If this bit is programmed to '0', VSYNC is controlled by the CRTC timing logic normally. If both HSYNC and VSYNC are set to '1', VCO is also powered down.
1	**Enable Double Buffered Display Start Address:** If this bit is set to '1', the display start address is updated on the VSYNC following a write to start address low. This provides control of display frame switching without the need to explicitly monitor VSYNC.
0	**Enable Interlaced:** If this bit is set to '1', interlaced timing is enabled. Interlaced timing means interlaced sync in Text mode, and interlaced sync and video data in Graphics mode. In addition, IRQ requests are generated only at the end of odd fields; that is, at the end of a frame. For interlaced sync and data in Graphics mode, set the CRTC Scan Double bit (CR9[7]) to '0'. Graphics modes 4 and 6 must always be non-interlaced.

NOTE: '?' in the above register addresses is 'B' in monochrome mode and 'D' in color mode.

4.30   CR1B: CRTC Extended Display Control Register

I/O Port Address: PCI	3?5h
Index	1Bh
Size (bits):	8
MMI/O Offset	6Ch
Access Type	Read/Write

Bit	Description
7	Enable Blank End Extensions
6	Reserved
5	Blanking Control
4	Offset [8]
3:2	Screen Start A Address [18:17]
1	Enable Extended Address Wrap
0	Extended Display Start Address [16]

This register contains a number of bits that control extended display functions.

Bit	Description
7	**Enable Blank End Extensions:** When this bit is set to '0', the Vertical and Horizontal Blank End Extension bits in CR1A are disabled if CR1B[5] is also '0'. If this bit is set to '1', the Vertical and Horizontal Blank End Extension bits in CR1A are enabled, regardless of how the CR1B[5] is programmed.
6	**Reserved**
5	**Blanking Control:** If this bit is set to '0', the DAC blanking is controlled by the Blanking signal generated by the CRTC. In this case, the border can be used (refer to the description of *AR11: Overscan (Border) Color Register* on page 3-69).
	If this bit is set to '1', the DAC blanking is controlled by display enable. The DAC is blanked during the time when the border is normally displayed. This signal can be directed to the feature connector or to control an external overlay circuit. Finally, programming this bit to '1' enables the Vertical and Horizontal Blank End Extension bits in CR1A.
4	**Offset [8]:** This bit extends the CRTC Offset register (CR13) by one bit. Refer to the description of CR0 on page 3-25, and summary of CRTC Timing registers on page 3-24.
	This bit allows for offsets of greater than 2048 bytes, and is used with 24-bit color modes to simplify pixel address calculations.
3:2	**Screen Start A Address [18:17]:** These two bits extend the Screen Start A Address.

4.30   CR1B: CRTC Extended Display Control Register *(cont.)*

Bit	Description
1	**Enable Extended Address Wrap:** If this bit is set to '0', the display memory address wraps at 64K maps (256K total memory). This provides VGA compatibility. If this bit is set to '1', the display memory address wraps at the total available memory size. In particular, this bit provides the following functions:
	If this bit is set to '1', and Chain4 addressing is selected (SR4[3] is '1'), then DRAM addresses A0 and A1 are supplied from addresses XMA[16] and XMA[17]. The XMA[18:12] addresses are the sum of XA[16:12] and either Offset register 0 or 1.
	If this bit is set to '1' and CRTC DoubleWord addressing is selected (CR14[6] is '1'), then DRAM Addresses A0 and A1 are supplied from CRTC Addresses CR[14] and CR[15]. This provides four pages that can be displayed in Video mode 13h. Character counter addresses, CA[16] and CA[18], provide up to 256 Kbytes in each bit plane, or 1 Mbyte of packed-pixel memory.
	If this bit is set to '0', the CRTC character address counter is 16-bits wide, providing VGA compatibility. If this bit is set to '1', the CRTC character address counter is 19-bits wide.
0	**Extended Display Start Address [16]:** This is bit 16 of the Extended Display Start Address.

NOTE: '?' in the above register addresses is 'B' in monochrome mode and 'D' in color mode.

4.31   CR1D: CRTC Screen Start A Extension Register

I/O Port Address: PCI	3?5h
Index	1Dh
Size (bits):	8
MMI/O Offset	74h
Access Type	Read/Write

Bit	Description
7:5	Reserved
4:3	Screen Start A Address [20:19]
2:1	Reserved
0	Offset [9]

This register contains extension bits for the screen start A address and the offset.

Bit	Description
7:5	**Reserved**
4:3	**Screen Start A Address [20:19]:** This field extends the Display Start Address by two additional bits. Refer to the description of CR0 on page 3-25, and summary of CRTC Timing registers on page 3-24.
2:1	**Reserved**
0	Offset [9]: This bit extends the offset field by one additional bit. Refer to the description of CR0 on page 3-25, and summary of CRTC Timing registers on page 3-24.

NOTE: '?' in the above register addresses is 'B' in monochrome mode and 'D' in color mode.

4.32   CR1E: CRTC Timing Overflow Register

I/O Port Address: PCI	3?5h
Index	1Eh
Size (bits):	8
MMI/O Offset	78h
Access Type	Read/Write

Bit	Description
7	Horizontal Total [8]
6	Horizontal Display End [8]
5	Horizontal Blank Start [8]
4	Horizontal Sync Start [8]
3	Vertical Total [10]
2	Vertical Display End [10]
1	Vertical Blank Start [10]
0	Vertical Sync Start [10]

This register contains bits for extending the Horizontal and Vertical Timing Control registers. Refer to the description of CR0 in Chapter 3, "VGA Core Registers" for a summary of CRTC Timing registers.

Bit	Description
7	**Horizontal Total [8]:** This bit extends the horizontal total field to nine bits.
6	**Horizontal Display End [8]:** This bit extends the horizontal display end field to nine bits.
5	**Horizontal Blank Start [8]:** This bit extends the horizontal blank start field to nine bits.
4	**Horizontal Sync Start [8]:** This bit extends the horizontal sync start field to nine bits.
3	**Vertical Total [10]:** This bit extends the vertical total field to 11 bits.
2	**Vertical Display End [10]:** This bit extends the vertical display end field to 11 bits.
1	**Vertical Blank Start [10]:** This bit extends the vertical blank start field to 11 bits.
0	**Vertical Sync Start [10]:** This bit extends the vertical sync start field to 11 bits.

NOTE: '?' in the above register addresses is 'B' in monochrome mode and 'D' in color mode.

4.33 CSL: Current Scanline Register (CL-GD5464 Only)

Size (bits):	16
MMI/O Offset	140h
Access Type	Read only

Bit	Description
15:12	Reserved
11:0	Current Scanline [11:0]

The Current Scanline register is provided to read back the scanline currently being displayed.

Bit	Description
15:12	**Reserved**
11:0	**Current Scanline [11:0]:** These bits are provided to support the DirectDraw Wait-ForVerticalBlank call and 3D-engine WAIT_FOR_SCANLINE command; these bits are not related to multi-buffering.

4.34 CSLC: Current Scanline Comparison Register (CL-GD5464 Only)

Size (bits):	16
MMI/O Offset	142h
Access Type	Read/Write

Bit   **Description**
15:12   Reserved
11:0   Compare Scanline [11:0]

The Current Scanline register is compared to the value in the Current Scanline Comparison register, and if the values are equal, the SCAN_EQUAL signal is asserted.

Bit	Description
15:12	**Reserved**
11:0	**Compare Scanline [11:0]:** This 12-bit field is used by the 3D-engine WAIT_FOR_SCANLINE command. The SCAN_EQUAL signal is synchronous to CCK, so it must be synchronized by the 3D-engine, but it is buffered by a flip-flop so it does not glitch when the scanline is incremented.

4.35 SSA: Secondary Start Address Register (CL-GD5464 Only)

Size (bits):   16

MMI/O Offset   144h

Access Type   Read/Write

Bit   **Description**
15:0   Screen Start Address [22:7]

This register specifies the starting address to be used for display following a buffer switch.

Bit	Description
15:0	**Screen Start Address [22:7]:** This 16-bit field allows the display to start on any 128-byte boundary (horizontal tile boundary); this granularity is required by the display logic, so all display fetches are tile-aligned.

4.36 Multi-Buffering Control Register (CL-GD5464 Only)

Size (bits):   8
MMI/O Offset   148h
Access Type   Read/Write

Bit	Description	Reset Value
7	VBLANK (Read only)	X
6	VSYNC (Read only)	0
5:4	Buffer Switch Delay [1:0]	0
3:2	Reserved	
1	Multi-Buffer Enable	0
0	SSA_ARM	0

This register specifies the multi-buffering control of the 3D engine.

Bit	Description
7	**VBLANK (Read only):** This read-only bit allows polling for VBLANK to issue a branch instruction to the 3D engine in Coprocessor mode.
6	**VSYNC (Read only):** This read-only bit is set by the leading edge of VSYNC. It is reset either by the falling edge of VSYNC or by reading this register (148h).
5:4	**Buffer Switch Delay [1:0]:** The BSD (buffer switch delay) specifies a minimum number of display frames to wait after a buffer switch before another switch can be performed. The default is '00b', which corresponds to a delay of zero frames, that is, a buffer switch can be done every frame. After the number of frames specified in BSD have completed, a buffer switch is still not performed until SSA_ARM is set by writing to the SSA register. This field is provided to help ensure an even animation frame rate. For example, if the time to render one frame or build a display list for the next frame was very close to one display frame time, the number of display frames per frame of animation might vary between one and two, (for example, 1,1,1,1,2,1,1,2,1,1,1,2,). The animation appears 'jerky'. In this case the BSD would be set to '01b', and the number of display frames per frame of animation rate is always two. While the average animation rate is less, the animation rate is smooth rather than 'jerky' and looks better.
3:2	**Reserved**
1	**Multi-Buffer Enable:** If this bit is set to '1', it selects the secondary start address rather than the normal start address (VGA CRC, CRD, CR1B, CR1D registers), and enables any other logic required for multi-buffering. If this bit is set to '0', it selects the normal start address (VGA CRC, CRD, CR1B, CR1D registers) for CRT display.
0	**SSA_ARM:** This read/write bit is set automatically in response to a write to the SSA register. It is used by the WAIT_ON_!ARM instruction, but is provided here for diagnostics. It can also be written directly to control execution of WAIT_ON_!ARM instructions.

4.37 TLUT_ LOAD Register (CL-GD5464 Only)

Size (bits):	32
MMI/O Offset	9Ch
Access Type	Read/Write

Bit	Description
31:24	CLUT Index [0–255]
23:16	Red Component Loaded
15:8	Green Component Loaded
7:0	Blue Component Loaded

This is the address for TLUT (texture lookup table) load. The TLUT index address is embedded within the register data written. A single address is used. Data (with embedded TLUT index) is written repeatedly to this address. In a display list, this address is mapped to however many palette writes are embedded in a WRITE_DEV_REGS instruction. That is, a write to 9Ch with 13 dwords will act as if all 13 were written to address 9Ch.

Bit	Description
31:24	**TLUT Index [0–255]:** TLUT index (0–255) where value is to be written.
23:16	**Red Component Loaded:** Red component to be loaded in the TLUT at the index given in bits 31:24.
15:8	**Green Component Loaded:** Green component to be loaded in the TLUT at the index given in bits 31:24.
7:0	**Blue Component Loaded:** Blue component to be loaded in the TLUT at the index given in bits 31:24.