2D Graphics Accelerator Registers

8.   2D GRAPHICS ACCELERATOR REGISTERS

The 2D Graphics Accelerator registers in the CL-GD546X are summarized in Table 8-1. These registers are only accessible with memory-mapped I/O (that is, in the address space defined in PCI10).

Table 8-1.   2D Graphics Accelerator Registers Quick Reference

Register Name	MMI/O Offset	Size (Bits)	Page
ALPHA_{A.B}	5E0h	32	8-4
BITMASK	5E8h	32[a]	8-5
BLTDEF	586h	16	8-6
BLTEXT_EX	700h	32	8-9
BLTEXT_XEX	600h	32	8-9
BLTEXTFF_EX	704h	32	8-10
BLTEXTFF_XEX	604h	32	8-10
BLTEXTR_EX	708h	32	8-11
BLTEXTR_XEX	608h	32	8-11
CHROMA_CNTL	512h	16	8-12
CHROMA_LOWER	5F0h	32	8-14
CHROMA_UPPER	5F4h	32	8-15
COMMAND	480h	32	8-16
CONTROL	402h	16	8-17
DRAWDEF	584h	16	8-19
HOST_DATA_PORT	800h–FFCh	32	8-20
LNCNTL	50Eh	16	8-21
MAJ_X	50Ah	16	8-23
MAJ_Y	502h	16	8-23
MIN_X	508h	16	8-23
MIN_Y	500h	16	8-23
ACCUM_X	50Ch	16	8-23
ACCUM_Y	504h	16	8-23
MBLTEXT_EX	720h	32	8-24
MBLTEXT_XEX	620h	32	8-24
MBLTEXTR_EX	728h	32	8-24

Table 8-1.   2D Graphics Accelerator Registers Quick Reference *(cont.)*

Register Name	MMI/O Offset	Size (Bits)	Page
MBLTEXTR_XEX	628h	32	8-25
MONOQW	588h	16	8-26
OFFSET_2D	405h	8	8-27
OP_opBGCOLOR	5E4h	32	8-28
OP_opFGCOLOR	5E0h	32	8-29
OP0_opMRDRAM	524h	32	8-30
OP1_opMRDRAM	544h	32	8-30
OP2_opMRDRAM	564h	32	8-30
OP1_opMSRAM	54Ah	16	8-31
OP2_opMSRAM	56Ah	16	8-31
OP0_opRDRAM	520h	32	8-32
OP1_opRDRAM	540h	32	8-32
OP2_opRDRAM	560h	32	8-32
OP0_opSRAM	528h	16	8-33
OP1_opSRAM	548h	16	8-33
OP2_opSRAM	568h	16	8-33
PATOFF	52Ah	16	8-34
QFREE	404h	8	8-35
RESIZEA_opRDRAM	408h	32	8-36
RESIZEB_opRDRAM	40Ch	32	8-36
RESIZEC_opRDRAM	410h	32	8-36
SHRINKINC	582h	16	8-37
SRCX	580h	16	8-38
STATUS	400h	16	8-39
STRETCH_CNTL	510h	16	8-40
TAG_MASK	5ECh	16	8-44
TILE_CTRL	407h	8	8-45
TIMEOUT	406h	8	8-46

[a] 32-bit registers can be operated on as two 16-bit registers.

8.1   ALPHA_{A,B} Register

Size (bits):	32
MMI/O Offset	5E0h
Access Type	Read/Write

Bit	Description
31:24	ALPHA_A (8 bits)
23:16	ALPHA_B (8 bits)
15:8	ALPHA_A (8 bits)
7:0	ALPHA_B (8 bits)

This register contains the two 8-bit values used in padding the Alpha channel in a:8:8:8 and a:5:5:5 modes.

IMPORTANT: This register is the same register as OP_opFGCOLOR on page 8-29.

In 16-bpp mode (that is, a:5:5:5 mode) only the most-significant bit of either Alpha channel is used (bit [31] in ALPHA_A or bit [23] in ALPHA_B). Note that in 16-bpp mode, only the lower word of the DWORD register need to be written due to the self-replicate nature of the register.

In 32-bpp mode (that is, a:8:8:8 mode) the Alpha data is 8-bits wide and is stored in dword format. The Alpha data is stored as ALPHA_A (bits [31:24]) and ALPHA_B (bits [23:16]).

Bit	Description
31:24	**ALPHA_A (8 bits)**
23:16	**ALPHA_B (8 bits)**
15:8	**ALPHA_A (8 bits)**
7:0	**ALPHA_B (8 bits)**

8.2   BITMASK Register

Size (bits):	32
MMI/O Offset	5E8h
Access Type	Read/Write

Bit	Description
31:0	BITMASK [31:0]

This register specifies which bits are written, when drawing into the frame buffer.

Bit	Description
31:0	**BITMASK [31:0]:** When drawing into the frame buffer, this 32-bit field controls which bits are written. This field is duplicated to create the 64-bit BITMASK in the RDRAMs. A write to this register initiates a mask-load cycle on the Rambus, if bit 13 of the DRAWDEF register is high. Bits in this field that are '1's enable writing to the corresponding bits in the RDRAM.
	This register must be completely filled, regardless of the pixel size. For example, in 16-bit pixels, the mask must be duplicated; in 8-bit pixels, the mask must be replicated to a total of four bytes to fill the register.

8.3   BLTDEF Register

Size (bits):   16
MMI/O Offset   586h
Access Type   Read/Write

Bit	Description
15	BD_Y_DIR
14:12	BD_RESULT [2:0]
11	BD_SAME
10:9	Reserved
8	BD_OP0
7	BD_OP1_PATTERN
6:4	BD_OP1 [2:0]
3	BD_OP2_PATTERN
2:0	BD_OP2 [2:0]

This register specifies the BitBLT direction, source of data for the three operands, and the destination of the result data.

Bit	Description
15	**BD_Y_DIR:** If this bit is programmed to '1', the BitBLT proceeds from a higher Y addresses to a lower Y addresses (from the bottom of the screen to the top of the screen). If this bit is programmed to '0', the BitBLT proceeds from a lower Y addresses to a higher Y addresses (from the top of the screen to the bottom of the screen).
14:12	**BD_RESULT [2:0]:** This three-bit field specifies the destination for the output of the ROP engine. OP0 and RESULT always share the same RDRAM and SRAM address.

BD_RES	Destination
000	Reserved
001	RDRAM color
010	Host color
011	Reserved
100	SRAM0 color
101	SRAM1 color
110	SRAM2 color
111	SRAM1 and SRAM2 color

Bit	Description
11	**BD_SAME:** If this bit is programmed to '1', it indicates OP1 and OP2 share the same RDRAM source, and only one RDRAM fetch must be performed for both SRAMs. Both OP1 and OP2 must have their pointers set to the same value.
10:9	**Reserved**

8.3   **BLTDEF Register** *(cont.)*

Bit	Description

8

BD_OP0: This bit specifies the source of OP0 within the ROP engine. OP0 is often referred to as the 'destination' operand. Each source defined with this bit has further destinations in other registers. Note that when the OP0 source is selected to be in RDRAM, it shares a common memory location as RESULT.

BD_OP2	Source
0	SRAM color
1	RDRAM color

7

BD_OP1_PATTERN: If this bit is '1', the pattern property of OP1 is enabled. If this bit is '0', the pattern property of OP1 is disabled.

6:4

BD_OP1 [2:0]: This three-bit field specifies the source of OP1 within the ROP engine. OP1 is often referred to as the 'source' operand. If the ROP has whiteness or blackness, this field must be programmed to '000b'.

BD_OP1	Source	Note
000	SRAM color	
001	RDRAM color	
010	Host color	
011	Reserved	
100	SRAM monochrome	X direction limited to 1792 pixels
101	RDRAM monochrome	X direction limited to 1792 pixels
110	Host monochrome	X direction limited to 1792 pixels
111	Color fill	Uses background color

3

BD_OP2_PATTERN: If this bit is '1', the pattern property of OP2 is enabled. If this bit is '0', the pattern property of OP2 is disabled.

8.3   BLTDEF Register *(cont.)*

Bit	Description
2:0	**BD_OP2 [2:0]:** This three-bit field specifies the source of OP2 within the ROP engine. OP2 is referred to as the 'pattern' or 'transparency' operand.

BD_OP2	Source	Note
000	SRAM color	
001	RDRAM color	
010	Host color	
011	Reserved	
100	SRAM monochrome	X direction limited to 1792 pixels
101	RDRAM monochrome	X direction limited to 1792 pixels
110	Host monochrome	X direction limited to 1792 pixels
111	Color color fill	Uses background color

8.4   BLTEXT_EX, BLTEXT_XEX Registers

Size (bits):	32
MMI/O Offset	700h (BLTEXT_EX)
MMI/O Offset	600h (BLTEXT_XEX)
Access Type	Read/Write

Bit	Description
31:29	Reserved
28:16	Y Extent [12:0]
15:12	Reserved
11:0	X Extent [11:0]

These registers define the BitBLT XY extents (the size of the destination pixel array). Each register can be accessed as a single 32-bit quality or two 16-bit quantities. Except for the difference in how they initiate the BitBLT operation, these two register addresses are the same. When BLTEXT_EX.pt.Y or BLTEXT_XEX.pt.X is written, a BitBLT operation is started.

Bit	Description
31:29	**Reserved**
28:16	**Y Extent [12:0]:** This is the Y size (height) of the result rectangle in scanlines.
15:12	**Reserved**
11:0	**X Extent [11:0]:** This is the X size (width) of the result rectangle in pixels. This value is converted to bytes when it is written. When it is read back, it is in bytes (even though it was written in terms of pixels).

8.5   BLTEXTFF_EX, BLTEXTFF_XEX Registers

Size (bits):	32
MMI/O Offset	704h (BLTEXTFF_EX)
MMI/O Offset	604h (BLTEXTFF_XEX)
Access Type	Read/Write

Bit	Description
31:29	Reserved
28:16	Y Extent [12:0]
15:12	Reserved
11:0	X Extent [11:0]

These registers define the XY extents (the size of the destination pixel array) for the Fast BitBLT operation. Each register can be accessed as a single 32-bit quality or two 16-bit quantities. Except for the difference in how they initiate the BitBLT operation, these two register addresses are the same. When BLTEXTFF_EX.pt.Y or BLTEXTFF_XEX.pt.X is written, a Fast BitBLT operation is started.

Bit	Description
31:29	**Reserved**
28:16	**Y Extent [12:0]:** This is the Y size (height) of the result rectangle in scanlines.
15:12	**Reserved**
11:0	**X Extent [11:0]:** This is the X size (width) of the result rectangle in pixels. This value is converted to bytes when it is written. When it is read back, it is in bytes (even though it was written in terms of pixels).

8.6   BLTEXTR_EX, BLTEXTR_XEX Registers

Size (bits):	32
MMI/O Offset	708h (BLTEXTR_EX)
MMI/O Offset	608h (BLTEXTR_XEX)
Access Type	Read/Write

Bit	Description
31:29	Reserved
28:16	Y Extent [12:0]
15:12	Reserved
11:0	X Extent [11:0]

These registers define the XY extents (the size of the destination pixel array) for the Resize BitBLT operation. Each register can be accessed as a single 32-bit quality or two 16-bit quantities. Except for the difference in how they initiate the BitBLT operation, these two register addresses are the same. When BLTEXTR_EX.pt.Y or BLTEXTR_XEX.pt.X is written, a Resize BitBLT operation is started. These extents specify the size of the result.

Bit	Description
31:29	**Reserved**
28:16	**Y Extent [12:0]:** This is the Y size (height) of the result rectangle in scanlines.
15:12	**Reserved**
11:0	**X Extent [11:0]:** This is the X size (width) of the result rectangle in pixels. This value is converted to bytes when it is written. When it is read back, it is in bytes (even though it was written in terms of pixels).

8.7 CHROMA_CNTL Register

Size (bits):	16
MMI/O Offset	512h
Access Type	Read/Write

Bit	Description
15	CMP_EN
14	DATA_SELECT
13	Reserved
12	CHROMA_TAG_EN
11:10	SEC_SEL [1:0]
9	RGB_OA_
8	SEC_OA_
7	SEC_EN
6	R_EN
5	G_EN
4	B_EN
3	SEC_IO_
2	R_IO_
1	G_IO_
0	B_IO_

This register allows chroma keying to be enabled or disabled on a pixel-component or global basis. This register also controls the selection of secondary chroma-key data, the selection of chroma-keying methods (AND or OR), and whether the chroma-key compare checks for values inside the specified value range or outside the specified value range. Related registers are CHROMA_LOWER (page 8-14), CHROMA_UPPER (page 8-15), and OP_opFGCOLOR (page 8-29).

Bit	Description
15	**CMP_EN:** This bit globally enables ('1') or disables ('0') the write-enable generation based on chroma-key comparison results.
14	**DATA_SELECT:** This bit selects whether chroma-key comparison occurs on raw pixel data or color converted RGB pixel data.
13	**Reserved**
12	**CHROMA_TAG_EN:** This bit enables the alpha channel selection capability of the chroma-key block. Global chroma keying must be disabled for this bit to have an effect.

8.7 CHROMA_CNTL Register *(cont.)*

Bit	Description
11:10	**SEC_SEL [1:0]**: This two-bit field selects which component of the input pixel is used in the secondary chroma-key compare process.

01	Green or U component
00	Blue or V component
10	Red or Y component
11	Reserved

Bit	Description
9	**RGB_OA_:** This bit selects the primary compare OR ('1') or primary compare AND ('0') process.
8	**SEC_OA_:** This bit selects secondary compare OR ('1') or secondary compare AND ('0') process.
7	**SEC_EN:** This bit enables ('1') or disables ('0') the secondary compare process.
6	**R_EN:** This bit enables ('1') or disables ('0') chroma keying on the Red or Y pixel component.
5	**G_EN:** This bit enables ('1') or disables ('0') chroma keying on the Green or U pixel component.
4	**B_EN:** This bit enables ('1') or disables ('0') chroma keying on the Blue or V pixel component.
3	**SEC_IO_:** This bit determines whether secondary compare checks for values inside ('1') or outside ('0') the compare boundaries.
2	**R_IO_:** This bit determines whether the Red or Y compare checks for values inside ('1') or outside ('0') the Red or Y compare boundaries.
1	**G_IO_:** This bit determines whether the Green or U compare checks for values inside ('1') or outside ('0') the Green or U compare boundaries.
0	**B_IO_:** This bit determines whether the Blue or V compare checks for values inside ('1') or outside ('0') the Blue or V compare boundaries.

8.8   CHROMA_LOWER Register

Size (bits):   32
MMI/O Offset   5F0h
Access Type   Write only

Bit	Description
31:24	Secondary Lower Boundary
23:16	Red or Y Lower Color Boundary
15:8	Green or U Lower Color Boundary
7:0	Blue or U Lower Color Boundary

This write-only register contains the lower-boundary values for the secondary compare, and the Red, Green, Blue, or (YUV) pixel component-compare processes.

Bit	Description
31:24	**Secondary Lower Boundary**
23:16	**Red or Y Lower Color Boundary**
15:8	**Green or U Lower Color Boundary**
7:0	**Blue or V Lower Color Boundary**

8.9   CHROMA_UPPER Register

Size (bits):	32
MMI/O Offset	5F4h
Access Type	Write only

Bit	Description
31:24	Secondary Upper Boundary
23:16	Red or Y Upper Color Boundary
15:8	Green or U Upper Color Boundary
7:0	Blue or U Upper Color Boundary

This write-only register contains the upper-boundary values for the secondary compare, and the Red, Green, Blue, or (YUV) pixel component-compare processes.

Bit	Description
31:24	**Secondary Upper Boundary**
23:16	**Red or Y Upper Color Boundary**
15:8	**Green or U Upper Color Boundary**
7:0	**Blue or V Upper Color Boundary**

8.10   COMMAND Register

Size (bits):	32
MMI/O Offset	480h
Access Type	Read only and Write only

Bit	Description
31:0	COMMAND (Read only) [15:0]
31:16	COMMAND CODE (Write only) [15:0]
15:0	COMMAND DATA (Write only) [15:0]

This register allows direct access to the Write FIFO input and output. Normally, accesses to this register are not required. This description is included for completeness only.

Bit	Description
31:0	**COMMAND [31:0] (Read only):** When this 32-bit register is read, the command, address, or data value is read from the Write FIFO. The command tag from CONTROL[7] should be read first. If the FIFO is empty, no error is generated. Allow the software at least 200 ns between two consecutive reads of COMMAND, or between a read of COMMAND and a read of CONTROL.
31:16	**COMMAND CODE [15:0] (Write only):** When this 16-bit field is written, the Command Code and Command Data are pushed onto the Write FIFO.
15:0	**COMMAND DATA [15:0] (Write only):** This 16-bit field must always be written together with the Command Code as a dword.

8.11   CONTROL Register

Size (bits):	16
MMI/O Offset	402h
Access Type	Read/Write

Bit	Description	Reset State
15	Reserved	0
14:13	BPP [1:0]	0
12:11	TILE_SIZE [1:0]	0
10	SWIZ_CNTL	0
9	Reserved	0
8	AUTO_BLT_EN	0
7	CNTL_TAG	X
6:4	Reserved	0
3	HALT_WR_FIFO	0
2	FLUSH_WR_FIFO	0
1	WAIT_WR_FIFO	0
0	Reserved	0

This register allows direct control of and returns the status of various parts of the command pipe and read/write FIFO. Except for the monochrome data swizzling that occurs prior to loading into memory, this register is only accessed during initialization.

Bit	Description
15	**Reserved**
14:13	**BPP [1:0]:** This two-bit field is the number of bits per pixel with normal encoding.

BPP Field	Bits Per Pixel
00	8
01	16
10	24
11	32

Bit	Description
12:11	**TILE_SIZE [1:0]:** This two-bit field specifies the tile control and tile size.

TILE_SIZE	Tiling	Tile Width
00	Enabled	128 byte
01	Enabled	256 byte
10	Disabled	128 byte
11	Disabled	256 byte

8.11 CONTROL Register *(cont.)*

Bit	Description
10	**SWIZ_CNTL:** When this bit is '1', bit order reverses if the host writes data through the HOSTDATA register. When this bit is '0', the bit order is not reversed. The reset state of this bit is '0'. **Programming Note:** When this bit is reprogrammed, the software must ensure that none of the other bits in the register are changed. This is typically done by reading the register, modifying this bit, and writing the results.
9	**Reserved**
8	**AUTO_BLT_EN:** When this bit is '0', the auto-BitBLT arm/trigger mechanism is disabled. When this bit is '1', the mechanism operates normally.
7	**CNTL_TAG (Read only):** This read-only bit returns the current command tag.
6:4	**Reserved**
3	**HALT_WR_FIFO:** When this bit is '1', popping the write FIFO is inhibited. When this bit is '0', the write FIFO operates normally.
2	**FLUSH_WR_FIFO**: When this bit is '1', the write FIFO is flushed. When this bit is '0', the write FIFO operates normally.
1	**WAIT_WR_FIFO:** When this bit is '1', the write FIFO is not written on consecutive clocks. A minimum of one wait state is inserted. This is intended for test purposes only. When this bit is '1', the write FIFO behaves normally.
0	**Reserved**

8.12 DRAWDEF Register

Size (bits):	16
MMI/O Offset	584h
Access Type	Read/Write

Bit	Description
15	DD_SAT1
14	DD_SAT2
13	BITMASK_EN
12:11	Reserved
10	PTAG
9	DD_TRANSOP
8	DD_TRANS
7:0	DD_ROP [7:0]

This register defines the ROPs, and specifies how transparency and color-to-monochrome conversion are handled for drawing operations.

Bit	Description
15	**DD_SAT1:** If this bit is '1', saturation-monochrome conversion is enabled for OP1.
14	**DD_SAT2:** If this bit is '1', saturation-monochrome conversion is enabled for OP2.
13	**BITMASK_EN:** If this bit is '1', writes to the BITMASK and TAGMASK registers are updated in the RDRAM.
12:11	**Reserved**
10	**PTAG:** The bit is written to RDRAM as the ninth bit. This identifies the type of data to the RAMDAC.
9	**DD_TRANSOP:** This bit specifies the transparency operation and is only used when DD_TRANS is '1'. See the table in bit 8 description.
8	**DD_TRANS:** This bit controls the transparency, in conjunction with DD_TRANSOP.

DD_TRANSOP	DD_TRANS	Result
0	0	Transparency disabled
0	1	Transparency enabled, equal
1	0	Transparency disabled
1	1	Transparency enabled, not equal

Bit	Description
7:0	**DD_ROP [7:0]:** This field specifies one of the 256 ternary (three operand) ROPs. For whiteness ('FFh') and blackness ('00h'), the programmer must specify that the OP1 source is SRAM.

8.13   HOST_DATA_PORT Register

Size (bits):	32
MMI/O Offset	800h–FFCh
Access Type	Read/Write

Bit	Description
31:0	HOST_DATA [31:0]

During host-to-screen and screen-to-host BitBLTs, this group of addresses is used for write and read data. This single 32-bit port is aliased across 2 Kbytes of address space. Host address bits 7:2 are ignored, allowing the use of MOVS instructions to transfer data in blocks. Access these ports as 32-bit quantities.

This port should only be written when supplying source data from the host for a BitBLT operation. This port should only be read to receive result data directed to the host from a BitBLT operation.

Bit	Description
31:0	**HOST_DATA [31:0]:** This port is written to send data to the 2D engine when the host is the source for a BitBLT. This port should be written only after the BitBLT is set up and started.
	This port is read to fetch data from the 2D engine when the host is the destination for a BitBLT. This port should be read only after the BitBLT is set up and started.

8.14 LNCNTL Register

Size (bits):   16
MMI/O Offset   50Eh
Access Type   Read/Write

Bit	Description
15:14	Reserved
13	UV HOLD
12	LOW PASS
11:10	Reserved
9	CHAIN
8	AUTO
7	Reserved
6:4	G_FORMAT [2:0]
3	YSHRINK
2	XSHRINK
1	YINTERP
0	XINTERP

This register specifies the Resize BitBLT and auto-BitBLT parameters, and is used for compatibility with the CL-GD546X 2D (revision 'AD'). It directly correlates to the new STRETCH_CNTL register. If any bits are written to the STRETCH_CNTL register, this register automatically changes to use those same bits. Caution should be taken when writing to this register as it directly affects the STRETCH_CNTL register.

Bit	Description
15:14	**Reserved**
13	**UV HOLD:** When this bit is '1', the first UV value is used for the AccuPak dword. When this bit is '0', the four UV values are averaged to obtain the value for the dword.
12	**LOW PASS:** When this bit is '1', the CL-GD546X performs a continuous average of chrominance data values across a line of AccuPak data during a stretch BitBLT. When this bit is '0', the averaging function is disabled.
11:10	**Reserved**
9	**CHAIN:** When this bit is '1', auto-BitBLTs fetch a new header. When this bit is '0', auto-BitBLTs do not fetch a new header. Program this bit to '0' for non-auto-Bit-BLTs.
8	**AUTO:** When this bit is '1', auto-BitBLTs are stretch BitBLTs. When this bit is '0', auto-BitBLTs are normal BitBLTs.
7	**Reserved**

8.14   LNCNTL Register *(cont.)*

Bit	Description

6:4   **G_FORMAT [2:0]:** This three-bit field specifies the format assumed by stretch Bit-BLTs. This field also determines the multiplication factor for automatic BitBLT coordinates. Program this field to a value consistent with the frame buffer format.

G_FORMAT	Format	Multiplication Factor
000	8-bpp palettized	1
001	16-bpp 1:5:5:5	2
010	16-bpp 5:6:5	2
011	YUV 4:2:2	2
100	32-bpp RGB	4
101	24-bpp RGB	3
110	AccuPak 4:1:1	1
111	Reserved	–

Bit	Description
3	**YSHRINK:** If this bit is programmed to '1', the resize operation is a shrink in the Y direction. If this bit is programmed to '0', the Y is stretched.
2	**XSHRINK:** If this bit is programmed to '1', a shrink in the X dimension is done. If this bit is programmed to '0', the operation is a stretch.
1	**YINTERP:** If this bit is programmed to '1', the Y lines are interpolated. If this bit is programmed to '0', the Y lines are decimated or replicated.
0	**XINTERP:** If this bit is programmed to '1', the X pixels are interpolated. If this bit is programmed to '0', the X pixels are decimated or replicated.

8.15   MAJ{X,Y}, MIN{X,Y}, ACCUM{X,Y} Registers

Size (bits):	16
MMI/O Offset	50Ah (MAJ_X)
MMI/O Offset	502h (MAJ_Y)
MMI/O Offset	508h (MIN_X)
MMI/O Offset	500h (MIN_Y)
MMI/O Offset	50Ch (ACCUM_X)
MMI/O Offset	504h (ACCUM_Y)
Access Type	Read/Write

Bit   **Description**

15:0   VALUE [15:0]

These six registers contain the values used by the stretch/shrink logic to calculate interpolation for the resize BitBLTs.

Bit	Description
15:0	**VALUE [15:0]:** These two sets of values are used by the stretch/shrink logic to calculate the interpolation. The MIN value is added to the respective ACCUM value. If the ACCUM value is negative, the respective MAJ value is added. These are two's complement numbers.

8.16   MBLTEXT_EX, MBLTEXT_XEX Registers

Size (bits):	32
MMI/O Offset	720h (MBLTEXT_EX)
MMI/O Offset	620h (MBLTEXT_XEX)
Access Type	Read/Write

Bit	Description
31:29	Reserved
28:16	Y_EXTENT [12:0]
15:12	Reserved
11:0	X_EXTENT [11:0]

These registers define the X and Y extents (the size of the destination pixel array in bytes and scanlines) for M (Mbyte) BitBLT operations. Each register can be accessed as a single 32-bit quality or two 16-bit quantities. Except for the difference in how they initiate the BitBLT operation, these two register addresses are the same. When MBLTEXT_EX.pt.Y or MBLTEXT_XEX.pt.X is written, an M BitBLT operation is started. The X extent is not byte converted.

Bit	Description
31:29	**Reserved**
28:16	**Y_EXTENT [12:0]:** This 13-bit field specifies the Y extent in scanlines.
15:12	**Reserved**
11:0	**X_EXTENT [11:0]:** This 12-bit field specifies the X extent in bytes. If monochrome data is part of the BitBLT, the software must set the MONOQW register with the number of monochrome qwords in the X direction.

8.17   MBLTEXTR_EX, MBLTEXTR_XEX Registers

Size (bits):	32
MMI/O Offset	728h (MBLTEXTR_EX)
MMI/O Offset	628h (MBLTEXTR_XEX)
Access Type	Read/Write

Bit	Description
31:29	Reserved
28:16	Y_EXTENT [12:0]
15:12	Reserved
11:0	X_EXTENT [11:0]

These registers define the X and Y extents (the size of the destination pixel array) for M (Mbyte) Resize BitBLT operations. Each register can be accessed as a single 32-bit quality or two 16-bit quantities. Except for the difference in how they initiate the BitBLT operation, these two register addresses are the same. When MBLTEXTR_EX.pt.Y or MBLTEXTR_XEX.pt.X is written, a resize operation is started. The X extent is not byte converted.

Bit	Description
31:29	**Reserved**
28:16	**Y_EXTENT [12:0]:** This 13-bit field specifies the Y extent in scanlines.
15:12	**Reserved**
11:0	**X_EXTENT [11:0]:** This 12-bit field specifies the X extent in bytes. This field is not byte converted by the hardware.

8.18 MONOQW Register

Size (bits):	16
MMI/O Offset	588h
Access Type	Read/Write

Bit	Description
15:6	Reserved
5:0	Monochrome QW Count [5:0]

This register specifies the monochrome qword count. Only set this register when the byte extent pointers are being used and monochrome data is part of the BitBLT. In this case, this register is programmed with the number of monochrome qwords required to satisfy the X extent register. Phase information is not included. When the normal extent pointers are used, this register is programmed to BLTEXT_EX.pt.X[11:6] plus BLTEXT_EX.pt.X[5:0].

Bit	Description
15:6	**Reserved**
5:0	**Monochrome QW Count [5:0]:** This six-bit field specifies the qword count of monochrome data.

8.19   OFFSET_2D Register

Size (bits):	8
MMI/O Offset	405h
Access Type	Read/Write

Bit	Description	Reset Value
7:0	OFFSET_2D [7:0]	0

This register specifies an offset to the Y component of the X,Y address in the 2D engine in increments of 16 lines. This register is reset to '00h'.

Bit	Description
7:0	**OFFSET_2D [7:0]:** This eight-bit field specifies the Y-component offset.

8.20 OP_opBGCOLOR Register

Size (bits):   32
MMI/O Offset   5E4h
Access Type   Read/Write

Bit	Description
31:0	BGCOLOR [31:0]

This register specifies the background color for the monochrome-to-color converter. Data is passed on to a selected OFU (operand function unit) for use with the selected raster operand. This register is used when the monochrome data is '0'.

Bit	Description
31:0	**BGCOLOR [31:0]:** This 32-bit register specifies the background color. The following table shows how this register is used for the various color depths.

Color Depth	31:24	23:16	15:8	7:0
8 bpp	Color	Color	Color	Color
16 bpp	Color		Color	
24 bpp	00h	Red	Green	Blue
32 bpp	Alpha[a]	Red	Green	Blue

[a] Alpha is typically zero.

8.21 OP_opFGCOLOR Register

Size (bits):	32
MMI/O Offset	5E0h
Access Type	Read/Write

Bit   **Description**

31:0   FGCOLOR [31:0]

This register specifies the foreground color for the monochrome-to-color converter. The data is passed on to a selected OFU for use with the selected raster operand. This register is used when the monochrome data is '1'.

IMPORTANT: This register is the same register as ALPHA_{A,B} (on page 8-4).

Bit   **Description**

31:0   **FGCOLOR [31:0]:** This 32-bit register specifies the foreground color. The following table shows how this register is used for the various color depths.

Color Depth	31:24	23:16	15:8	7:0
8 bpp	Color	Color	Color	Color
16 bpp	Color		Color	
24 bpp	00h	Red	Green	Blue
32 bpp	Alpha[a]	Red	Green	Blue

[a] Alpha is typically zero.

8.22   OP{0–2}_opMRDRAM Registers

Size (bits):	32
MMI/O Offset	524h (OP0_opMRDRAM)
MMI/O Offset	544h (OP1_opMRDRAM)
MMI/O Offset	564h (OP2_opMRDRAM)
Access Type	Read/Write

Bit	Description
31:30	Reserved
29:16	Y [13:0]
15:0	X [15:0]

These three registers specify the location of monochrome pattern or scanline data in the frame buffer (RDRAM) for the three pixel path operands: OP0, OP1, and OP2. The two fields in each register can be accessed as a single 32-bit quantity, or X and Y can be accessed as individual 16-bit quantities. Use these registers only when using monochrome data or when byte conversion is not needed.

Bit	Description
31:30	**Reserved**
29:16	**Y [13:0]:** This 14-bit field specifies the vertical position of the operand data in RDRAM memory. This field is specified in terms of scanlines.
15:0	**X [15:0]:** This 16-bit field specifies the horizontal position of the operand data in RDRAM memory. This field is specified in terms of bits for monochrome and bytes for non-monochrome.

8.23 OP{1–2}_opMSRAM Registers

Size (bits):	16
MMI/O Offset	54Ah (OP1_opMSRAM)
MMI/O Offset	56Ah (OP2_opMSRAM)
Access Type	Read/Write

Bit	Description
15:13	Reserved
12:0	SRAM Address [12:0]

These two registers specify the location of monochrome pixel data in operand 1 SRAM and operand 2 SRAM. The SRAM address specifies where the actual pixel data resides. Each register is accessed as a single 16-bit quantity. No pixel-to-byte conversion occurs with this command. These registers are write only, but can be read using the OP{1–2}_opSRAM addresses.

Bit	Description
15:13	**Reserved**
12:0	**SRAM Address [12:0]:** This 13-bit field specifies the horizontal position where pixel data resides in SRAM memory. Bits 5:0 specify the source phase.

8.24   OP{0–2}_opRDRAM Registers

Size (bits):	32
MMI/O Offset	520h (OP0_opRDRAM)
MMI/O Offset	540h (OP1_opRDRAM)
MMI/O Offset	560h (OP2_opRDRAM)
Access Type	Read/Write

Bit	Description
31:30	Reserved
29:16	Y [13:0]
15:13	Reserved
12:0	X [12:0]

These three registers specify the location of color pixel data in the frame buffer (RDRAM). This RDRAM address describes where pattern or scanline data resides. Each register can be accessed as a single 32-bit quality or two 16-bit quantities. These registers specify the phase for both RDRAM and host transfers. When OP1 or OP2 is sourced from the host, set the corresponding OPx_opRDRAM.pt.X with the phase of the host data. The same rotation calculation is used for RDRAM accesses. OP0_opRDRAM.pt.X calculates the result phase for destination to RDRAM, destination to host, and for all three SRAM results. In addition, OP0_opRDRAM is used to anchor the patterns. The RDRAM X address is converted to a byte address when written to the register, and reads back as a byte address. To set the monochrome address, the program should use the OP{0–2}_opMRDRAM register.

Bit	Description
31:30	**Reserved**
29:16	**Y [13:0]:** This 14-bit field specifies the vertical position of the operand data in RDRAM memory. This field is specified in terms of scanlines.
15:13	**Reserved**
12:0	**X [12:0]:** This 13-bit field specifies the horizontal position of the operand data in RDRAM memory. This field is specified in terms of pixels.

8.25   OP{0–2}_opSRAM Registers

Size (bits):	16
MMI/O Offset	528h (OP0_opSRAM)
MMI/O Offset	548h (OP1_opSRAM)
MMI/O Offset	568h (OP2_opSRAM)
Access Type	Read/Write

Bit	Description
15:7	Reserved
6:0	Color SRAM Address [6:0]

These three registers specify the location of color pixel data in the SRAM for operands 0–2. The SRAM address describes where the actual pixel data resides for read operations. These registers are accessed as 16-bit quantities. This register is converted to a byte address when written to the register, and reads back as a byte address. (Use OP{1–2}_opMSRAM to specify the location of monochrome data in the SRAM for operands 1–2.)

Bit	Description
15:7	**Reserved**
6:0	**Color SRAM Address [6:0]:** This seven-bit field specifies the horizontal position of the pixel data in SRAM memory. The phase is indicated with the least-significant bits as shown in the table below.

Pixel Depth (bytes)	Phase
1	2:0
2	1:0
4	0

8.26 PATOFF Register

Size (bits):	16
MMI/O Offset	52Ah
Access Type	Read/Write

Bit	Description
15:11	Reserved
10:8	Y [2:0]
7:3	Reserved
2:0	X [2:0]

This register specifies the pattern pixel offset that calculates offset for anchored patterns. To produce the offset into the pattern, each segment is added to OP0_opRDRAM before byte conversion.

Bit	Description
15:11	**Reserved**
10:8	**Y [2:0]:** This three-bit field specifies the Y offset.
7:3	**Reserved**
2:0	**X [2:0]:** This three-bit field specifies the X offset.

8.27   QFREE Register

Size (bits):   8

MMI/O Offset   404h

Access Type   Read Only

Bit	Description	Reset State
7:5	Reserved	
4	QFREE [4]	1
3	QFREE [3]	1
2	QFREE [2]	0
1	QFREE [1]	0
0	QFREE [0]	1

This read-only register returns the count of 32-bit words currently free in the data/command write FIFO.

Bit	Description
7:5	**Reserved**
4:0	**QFREE [4:0]:** This five-bit field returns the number of free entries in the command/data write FIFO.

8.28　RESIZE{A–C}_opRDRAM Registers

Size (bits):	32
MMI/O Offset	408h (RESIZEA_opRDRAM)
MMI/O Offset	40Ch (RESIZEB_opRDRAM)
MMI/O Offset	410h (RESIZEC_opRDRAM)
Access Type	Read/Write

Bit	Description
31	TRIGGER
30	ARM
29:16	Y [13:0]
15:0	X [15:0]

These three registers specify the location of source color pixel data for the automatic Resize Bit-BLT operation. Each register contains a separate source address, triggered when the screen refresh reaches the appropriate scanline. During an automatic BitBLT, the first line read from this address contains the Resize BitBLT parameters. When used for V-Port double buffering, write the RESIZE{A–C}_opRDRAM.pt.Y as an even address. This allows the V-Port controller to toggle between two buffers. In all cases, align the source address to the first byte in a tile.

Bit	Description
31	**TRIGGER:** If this bit is '1', the auto-BitBLT begins when this register is written. If this bit is '0', the CL-GD546X waits for the appropriate vertical count before beginning the auto-BitBLT.
30	**ARM:** If this bit is '1', the auto-BitBLT starts when the CRT controller reaches the appropriate vertical count. If this bit is '0', the auto-BitBLT must be armed externally.
29:16	**Y [13:0]:** This 14-bit field specifies the vertical location of the source data in the RDRAM. This field is programmed in terms of scanlines.
15:0	**X [15:0]:** This 16-bit field specifies the horizontal location of the source data in the RDRAM. This field is programmed in terms of bytes.

8.29   SHRINKINC Register

Size (bits):	16
MMI/O Offset	582h
Access Type	Read/Write

Bit	Description
15:8	Y [7:0]
7:0	X [7:0]

This register specifies the X and Y increments for skipping source shrink Resize BitBLT operations. The Y value is set equal to the shrink reduction factor (Y = n; where the shrink is n:1). When interpolation is disabled (see the LNCNTL register on page 8-21) the X value is also set to the shrink reduction factor n.

When interpolation is enabled, the X value is set to the shrink reduction factor minus one (n−1). For example:
2:1 shrink with decimation, X = 2 and Y= 2, or
4:1 shrink with averaging, X = 4 and Y = 3.

Bit	Description
15:8	**Y [7:0]:** This eight-bit field specifies the Y (scanline) increment value. The minimum value for this field is '1'. It is set equal to the shrink reduction factor.
7:0	**X [7:0]:** This eight-bit field specifies the X pixel increment value. This field is set equal to the shrink reduction factor when interpolation is disabled (decimation), and is set equal to the shrink reduction factor minus one when interpolation is enabled (averaging).

8.30 SRCX Register

Size (bits):	16
MMI/O Offset	580h
Access Type	Read/Write

Bit   **Description**

15:0   SRCX [15:0]

This register specifies the width, in bytes, of the source pixel array for Resize BitBLT operations.

Bit	Description
15:0	**SRCX [15:0]:** This 16-bit field specifies X extent (source pixel array width) in bytes.

8.31   STATUS Register

Size (bits):	16
MMI/O Offset	400h
Access Type	Read only

Bit	Description
15	RDQUEUE
14:3	Reserved
2	WF_EMPTY
1	BLT_FLAG
0	BLT_RDY

This read-only register returns the current completion status of 2D engine drawing operations.

Bit	Description
15	**RDQUEUE:** If this bit is '1', there is data available in the read queue.
14:3	**Reserved**
2	**WF_EMPTY:** If this bit is '0', the write FIFO is empty. If this bit is '1', the write FIFO is not empty.
1	**BLT_FLAG:** If this bit is '1', the BitBLT engine is not idle. If this bit is '0', the BitBLT engine is idle.
0	**BLT_RDY:** If this bit is '0', the BitBLT engine is ready for a new command. If this bit is '1', the BitBLT engine is not ready for a new command.

8.32   STRETCH_CNTL Register

Size (bits):	16
MMI/O Offset	510h
Access Type	Read and Write

Bit	Description
15:12	SRC_FMT
11:8	DST_FMT
7	CHAIN
6	AUTO
5:4	Reserved
3	YSHRINK
2	XSHRINK
1	YINTERP
0	XINTERP

The STRETCH_CNTL register is introduced in the CL-GD5464 of the CL-GD546X family of VisualMedia accelerators. This register defines the functions of stretch operations within the 2D logic. Related registers are BLTDEF (page 8-6), DRAWDEF (page 8-19), and OP_opFGCOLOR (page 8-29). The STRETCH_CNTL register is also linked directly with the LNCNTL register, any bits written to either register changes the other register.

This register replaces the function of the LNCNTL register in previous revisions of the CL-GD5462. Note that the LNCNTL register is still functional in the CL-GD5464, and is provided for software compatibility. The LNCNTL register does not allow for any of the format conversions provided by STRETCH_CNTL register.

CAUTION: Both registers affect the operation of the stretch logic. A write to the LNCNTL register affects the contents of the STRETCH_CNTL register as shown in the following table.
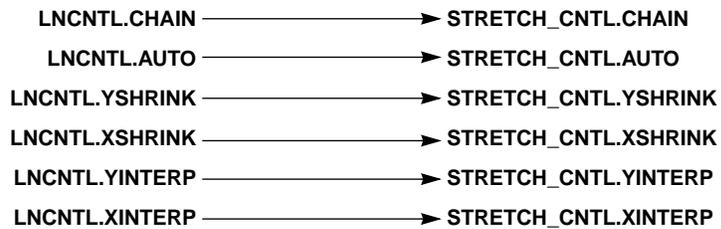
Table 8-2.   Conversion from LNCNTL to STRETCH_CNTL Operations

LNCNTL.G_FORMAT		STRETCH_CNTL.SRC_FMT		STRETCH_CNTL.DST_FMT	
Value	Corresponding Format	Value	Corresponding Format	Value	Corresponding Format
000	8-bpp CLUT	0000	8-bpp CLUT	0000	8-bpp CLUT
001	RGB 16-bpp 1:5:5:5	0001	RGB 16-bpp 1:5:5:5	0001	RGB 16-bpp 1:5:5:5
010	RGB 16-bpp 5:6:5	0010	RGB 16-bpp 5:6:5	0010	RGB 16-bpp 5:6:5
011	YUV 16-bpp 4:2:2	1001	YUV 16-bpp 4:2:2	1001	YUV 16-bpp 4:2:2
100	RGB 24-bpp 8:8:8 (packed TC)	0011	RGB 24-bpp 8:8:8 (packed TC)	0011	RGB 24-bpp 8:8:8 (packed TC)
101	RGB 32-bpp A:8:8:8 (alpha TC)	0100	RGB 32-bpp A:8:8:8 (alpha TC)	0100	RGB 32-bpp A:8:8:8 (alpha TC)
110	Reserved	1000	Reserved	1000	Reserved
111	n/a				

Table 8-3.   Expected STRETCH_CNTL Resize Operations/Conversions

Source Data	Destinations
8-bpp CLUT	8-bpp CLUT
RGB 16-bpp 1:5:5:5	RGB 16-bpp A:5:5:5
RGB 16-bpp 5:6:5	RGB 16-bpp 5:6:5
RGB 24-bpp 8:8:8 (packed TC)	RGB 24-bpp 8:8:8 (packed true color)
RGB 32-bpp A:8:8:8 (alpha TC)	RGB 32-bpp A:8:8:8 (alpha true color)
YUV 16-bpp 4:2:2	YUV 16-bpp 4:2:2 RGB 16-bpp A:5:5:5 RGB 16-bpp 5:6:5 RGB 24-bpp 8:8:8 (packed true color) RGB 32-bpp A:8:8:8 (alpha true color)
VYU 24-bpp 4:4:4	VYU 24-bpp 4:4:4 YUV 16-bpp 4:2:2 RGB 16-bpp A:5:5:5 RGB 16-bpp 5:6:5 RGB 24-bpp 8:8:8 (packed true color) RGB 32-bpp A:8:8:8 (alpha true color)

The correlation between the LNCNTL and STRETCH_CNTL registers is as follows:

LNCNTL.CHAIN ⟶	**STRETCH_CNTL.CHAIN**
LNCNTL.AUTO ⟶	**STRETCH_CNTL.AUTO**
LNCNTL.YSHRINK ⟶	**STRETCH_CNTL.YSHRINK**
LNCNTL.XSHRINK ⟶	**STRETCH_CNTL.XSHRINK**
LNCNTL.YINTERP ⟶	**STRETCH_CNTL.YINTERP**
LNCNTL.XINTERP ⟶	**STRETCH_CNTL.XINTERP**

8.32 STRETCH_CNTL Register *(cont.)*

Bit	Description

| 15:12 | **SRC_FMT:** Converted and non-converted format stretch operations are controlled by these bits. |

Standard stretch operations are performed by setting the source and destination formats to the same operation. Such as setting source and destination format to '0011' (24-bit-packed-pixel format) and performing the stretch operation.

Format conversion is performed by selecting source to one format, such as '1001' (9h) YUV 4:2:2 and setting the destination to '0010' (2h) RGB 5:6:5, an RGB function. Unlimited conversion is possible, but some modes produce random data. YUV formats 1001–1010 are converted to RGB formats 0001–0100.

Format conversion allows for an input data stream of YUV data stored into off-screen memory and resize converted to an RGB format of on-screen memory in the selected video format.

SRC_FMT	Source Data Format
0000	8-bpp CLUT
0001	RGB 16-bpp A:5:5:5
0010	RGB 16-bpp 5:6:5
0011	RGB 24-bpp 8:8:8 (packed TC)
0100	RGB 32-bpp A:8:8:8 (alpha TC)
0101–0111	n/a
1000	Reserved
1001	YUV 16-bpp 4:2:2
1010	VYU 24-bpp 4:4:4
1011–1111	Reserved

8.32   STRETCH_CNTL Register *(cont.)*

Bit	Description
11:8	**DST_FMT**: Formats '0001' and '0100' (A:5:5:5 and A:8:8:8) receive their alpha data from the OP_OPFGCOLOR register.

DST_FMT	Destination Data Format
0000	8-bpp CLUT
0001	RGB 16-bpp A:5:5:5
0010	RGB 16-bpp 5:6:5
0011	RGB 24-bpp 8:8:8 (packed true color)
0100	RGB 32-bpp A:8:8:8 (alpha true color)
0101–0111	n/a
1000	Reserved
1001	YUV 16-bpp 4:2:2
1010	VYU 24-bpp 4:4:4
1011–1111	Reserved

Bit	Description
7	**CHAIN:** When this bit is '1', auto-BitBLTs fetch a new header. When this bit is '0', auto-BitBLTs do not fetch a new header. Program this bit to '0' for non-auto-Bit-BLTs.
6	**AUTO:** When this bit is '1', auto-BitBLTs are stretch BitBLTs. When this bit is '0', auto-BitBLTs are normal BitBLTs.
5:4	**Reserved**: These bits were 4:1:1 (AccuPak) format functions.
3	**YSHRINK:** If this bit is programmed to '1', resize operation is a shrink in the Y direction. If this bit is programmed to '0', Y is stretched.
2	**XSHRINK:** If this bit is programmed to '1', a shrink in the X dimension is done. If this bit is programmed to '0', the operation is a stretch.
1	**YINTERP:** If this bit is programmed to '1', Y lines are interpolated. If this bit is programmed to '0', Y lines are decimated or replicated.
0	**XINTERP:** If this bit is programmed to '1', X pixels are interpolated. If this bit is programmed to '0', X pixels are decimated or replicated.

8.33 TAG_MASK Register

Size (bits):	16
MMI/O Offset	5ECh
Access Type	Read/Write

Bit	Description
15:3	Reserved
2	PT_MASK (Read only)
1	Reserved
0	PT_MASK (Write only)

This register specifies the pixel tag mask for use with 9-bit RDRAMs. When this register is written, a mask-load cycle is generated for the RDRAMs if bit 13 of DRAWDEF is high. The pixel tag is in the DRAWDEF register on .

Bit	Description
15:3	**Reserved**
2	**PT_MASK (Read only):** This read-only bit is a pixel mask that allows writing of the PTAG bit to read back to this bit.
1	**Reserved**
0	**PT_MASK (Write only):** This write-only bit is a pixel mask that allows writing of the PTAG bit to write back to this bit.

8.34 TILE_CTRL Register

Size (bits):   8
MMI/O Offset   407h
Access Type   Read/Write

Bit	Description	Reset
7:6	BANK_INTERLEAVE [1:0]	0
5	TILES_PER_LINE [5:]	0
4	TILES_PER_LINE [4]	1
3:0	TILES_PER_LINE [3:0]	0

This register controls memory (RDRAM) interleaving and tiling. This register is an immediate register.

Bit	Description
7:6	**BANK_INTERLEAVE [1:0]:** This two-bit field controls the memory interleave factor.

BANK_INTERLEAVE [1:0]	Interleave Mode
00b	No interleave
01b	2-way bank interleave
10b	4-way bank interleave
11b	Reserved

5:0   **TILES_PER_LINE [5:0]:** This six-bit field specifies the tiles per line. Values not shown in the table below are reserved and must not be programmed.

TILE_CTRL [5:0]	Tile Per Line	TILE_SIZE = 128 or 128L Total Pitch	TILE_SIZE = 256 or 256L Total Pitch
5d	5	640	1280
8d	8	1024	2048
10d	10	1280	2560
13d	13	1664	3328
16d	16	2048	4096
20d	20	2560	5120
26d	26	3328	6656
32d	32	4096	8192

8.35 TIMEOUT Register

Size (bits):	8
MMI/O Offset	406h
Access Type	Read/Write

Bit	Description
7	Reserved
6	TIMEOUT_OCCURRED
5	TIME_X16
4	TIMEOUT_EN
3:0	TIMEOUT [3:0]

After a cycle is initiated, this register specifies the number of system clocks that the CL-GD546X must make wait before releasing the host by asserting the ready signal. This is an immediate register. The intended use of this register is during device driver development to prevent bus lockups.

Bit	Description
7	**Reserved**
6	**TIMEOUT_OCCURRED:** If this bit is read as '0', it indicates a time-out has occurred. A '1' must be written to this bit by the software to clear the time-out indicator.
5	**TIMEOUT_X16:** If this bit is programmed to '1', the time-out period is increased by a factor of 16, and 'k' in the following equation is 240. If this bit is programmed to '0', 'k' in the following equation is 15.

$$TimeoutPeriod \ = \ (Timeout + 1) \bullet k \qquad \text{Equation 8-1}$$

Bit	Description
4	**TIMEOUT_EN:** If this bit is '1', the time-out bus release is enabled. This bit should not be set in normal operation or unreliable operation occurs when the device driver is busy.
3:0	**TIMEOUT [3:0]:** This field is the time-out period. See Equation 8-1.