

Laguna VisualMedia™
Accelerators Family
CL-GD546X

Software Technical Reference Manual

Second Edition



Notice

Cirrus Logic Inc. has made best efforts to ensure that the information contained in this document is accurate and reliable. However, the information is subject to change without notice. No responsibility is assumed by Cirrus Logic Inc. for the use of this information, nor for infringements of patents or other rights of third parties. This document is the property of Cirrus Logic Inc. and implies no license under patents, copyrights, or trade secrets. No part of this publication may be copied, reproduced, stored in a retrieval system, or transmitted, in any form or by any means, electronic, mechanical, photographic, or otherwise, or used as the basis for manufacture or sale of any items without the prior written consent of Cirrus Logic Inc. Cirrus Logic, AccuPak, CompactCard, CompactStor, DIVA, FastPath, FeatureChips, Good Data, Laguna, MediaDAC, MotionVideo, SimulSCAN, S/LA, SofTarget, TextureJet, TVTap, UXART, VisualMedia, V-Port, and WavePort are trademarks of Cirrus Logic Inc., which may be registered in some jurisdictions. Other trademarks in this document belong to their respective companies. CRUS and Cirrus Logic International, Ltd. are trade names of Cirrus Logic Inc.

Copyright Notice

This manual is copyrighted. All rights are reserved. No part of this publication may be copied, reproduced, stored in a retrieval system, or transmitted, in any form or by any means, electronic, mechanical, photographic, or otherwise, or used as the basis for manufacture or sale of any items without the prior written consent of Cirrus Logic Inc.

Copyright © 1996 — Cirrus Logic Inc. All rights reserved.
First edition was published in September 1995.

Contents

Table of Contents

1.	OVERVIEW	1-2
1.1	Architectural Overview	1-2
1.1.1	System Block Diagrams	1-2
1.1.2	Internal Architecture	1-3
1.2	Programming Model	1-5
1.2.1	VGA.....	1-5
1.2.2	Pixels.....	1-7
1.2.3	Bi-endian Support	1-11
1.3	Bus Model	1-13
1.3.1	Accessing Registers.....	1-13
1.3.2	Managing the Memory-Mapped Register	1-13
1.3.3	Initializing Configuration Registers	1-17
1.3.4	VGA Sleep Mode	1-17
1.4	Memory Organization	1-17
1.4.1	Frame Buffer Linear Addressing	1-18
1.4.2	Frame Buffer Addressing: VGA Compatibility	1-18
1.4.3	Linear and Tiled Modes.....	1-19
1.4.4	Registers	1-28
1.4.5	SRAM.....	1-33
2.	2D PROGRAMMER'S GUIDE	2-2
2.1	2D Graphics Engine	2-2
2.1.1	2D Frame Buffer.....	2-4
2.1.2	Bit Swizzle	2-5
2.1.3	Patterns	2-5
2.1.4	Monochrome-to-Color Expansion.....	2-6
2.1.5	Transparency	2-6
2.2	2D Graphics BitBLT Operations	2-6
2.2.1	Commonly Used BitBLT Control Registers	2-7
2.2.2	BitBLT Programming Overview	2-8
2.2.3	Monochrome-to-Color Conversion BitBLTs.....	2-11
2.2.4	Transparent BitBLTs	2-12
2.2.5	Pattern BitBLTs	2-12
2.2.6	Host BitBLTs	2-13
2.2.7	Byte BitBLTs (MBitBLTs).....	2-14
2.3	Tips and Tricks	2-15
2.4	BitBLT Programming Examples	2-15
2.4.1	Software Cursor Programming Example.....	2-16
2.4.2	Font Load Programming Example	2-19
2.4.3	Text BitBLT, Foreground/Background Color Programming Example	2-20
2.4.4	Text BitBLT, Monochrome Font from Host Programming Example	2-20
2.4.5	Text BitBLT, Transparent Background Programming Example ...	2-22
2.4.6	Simple Source Copy Programming Example.....	2-23

	2.4.7	Copy Frame Buffer-to-Host Programming Example.....	2-24
	2.4.8	Color-Pattern BitBLT Programming Example.....	2-25
	2.4.9	Monochrome-to-Color BitBLT Programming Example	2-26
	2.4.10	Solid-Color-Fill Programming Example	2-27
	2.4.11	Copy Host to SRAM to Frame Buffer Programming Example.....	2-28
	2.4.12	Transparent-Monochrome-Cursor Programming Example	2-30
	2.4.13	Color-Transparency BitBLTs Programming Example	2-32
	2.4.14	Monochrome-Pattern-Transparency Mask Programming Example	2-35
	2.4.15	Byte BitBLT Using MBitBLT and BitBLT for Color-Fills Programming Example.....	2-36
	2.4.16	Byte BitBLT Using MBitBLT to Off-Screen Cache Programming Example.....	2-37
2.5		Register Header Files	2-38
	2.5.1	Header File — lgtypes.h.....	2-38
	2.5.2	Header File — lgregs.h	2-39
2.6		2D Graphics Engine Initialization	2-50
3.		3D PROGRAMMER'S GUIDE	3-2
	3.1	Architectural Overview	3-2
	3.1.1	System Block Diagrams	3-2
	3.1.2	Internal Architecture	3-4
	3.2	3D Programming Model	3-8
	3.2.1	Direct Programming	3-8
	3.2.2	Coprocessor Indirect Programming.....	3-8
	3.2.3	Display List Programming	3-9
	3.2.4	Host Memory-Based Formats	3-9
	3.3	3D Rendering Overview	3-9
	3.3.1	Incremental Line-Drawing Algorithm	3-10
	3.3.2	Flat (Unshaded) Polygon.....	3-12
	3.3.3	Summary of Values Used for Flat Triangle	3-15
	3.3.4	Scaled Numbers.....	3-15
	3.3.5	Gouraud Shading	3-16
	3.3.6	X-Y Clipping	3-18
	3.3.7	Z-Buffering.....	3-18
	3.3.8	Color Transparency.....	3-20
	3.3.9	Lighting.....	3-22
	3.3.10	Saturation.....	3-22
	3.3.11	Alpha Blending	3-22
	3.3.12	Additional Notes on Lighting.....	3-24
	3.3.13	Data Path Equation	3-25
	3.3.14	Texture and Perspective Texture Mapping	3-26
	3.3.15	Quadrangles.....	3-29
	3.3.16	Lines and Points.....	3-30
3.4		3D Memory Organization	3-32
	3.4.1	System Memory Space View of Frame Buffer Memory	3-32

3.4.2	System Processor (Across PCI Bus) View of the Register Set....	3-32
3.4.3	System Memory Objects View from the CL-GD5464	3-37
3.4.4	READ_3D_REGISTER — Multiple Commands View of System Memory	3-39
3.5	CL-GD5464 3D Instruction Set	3-40
3.5.1	Instruction Summary	3-40
3.5.2	Instruction Field Tables	3-44
3.5.3	Instruction Listings	3-48
3.6	3D Register Header Files	3-73
3.6.1	trm.h	3-73
3.6.2	l3struct.h.....	3-82
3.6.3	l3types.h.....	3-89
3.6.4	modemon.h	3-90
3.7	Programming Examples	3-94
3.7.1	CL-GD5464 Setup.....	3-94
3.7.2	Z-Buffered Points	3-106
3.7.3	Alpha-Blended Points.....	3-108
3.7.4	Gouraud-Shaded Lines	3-110
3.7.5	Gouraud-Shaded, Dithered Polygon	3-111
3.7.6	Polygons with Z-Buffering, Flat-Shading, and Other Modifiers ..	3-112
3.7.7	Polygon Showing Z-Buffering, Stippling, and Constant Lighting	3-114
3.7.8	Polygons Showing Texture Mapping.....	3-116
3.7.9	Polygons Showing Filtered Texture Mapping.....	3-118
3.7.10	Initial Width Instruction Modifier	3-120
3.7.11	Double/Multi Buffering.....	3-120
3.7.12	2D Display Lists.....	3-121
3.7.13	Z-Collision Detection	3-121
3.7.14	2D BitBLT Examples	3-123
3.7.15	Process Synchronization.....	3-124
3.7.16	CL-GD5464 3D Events	3-125
3.7.17	Self Interrupts.....	3-125
4.	VIDEO PROGRAMMING	4-2
4.1	Resize BitBLTs	4-2
4.1.1	Required Parameters	4-3
4.1.2	Optional Parameters	4-3
4.2	Resize BitBLTs, Occlusion, and 9-bit Frame Buffers	4-7
4.3	Displaying 16-bit Video in an 8-bit Frame Buffer	4-9
4.4	Format Conversion Resize BitBLTs	4-10
4.5	Chroma-Key Programming for Resize BitBLTs	4-12
4.6	Programming Resize BitBLT Using Auto-BitBLT	4-13
4.7	Programming Safe Times for Auto-BitBLTs	4-15
4.8	Programming Considerations for Odd/Even Field Captured Data	4-16

5.	SYSTEM OPERATION	5-2
5.1	System Control and Initialization	5-2
5.1.1	Rambus® Initialization	5-2
5.1.2	Frame Buffer	5-28
5.1.3	Other Registers of Interest	5-28
5.1.4	Memory Tile Interleave Setup	5-31
5.1.5	Differences from Standard VGA.....	5-33
5.2	CRTC Programming	5-34
5.2.1	VESA® Timing Specifications	5-34
5.2.2	CRTC Timing.....	5-35
5.2.3	Programming VCLK	5-36
5.2.4	Programming BCLK	5-37
5.2.5	Non-Standard Timing Parameters.....	5-37
5.3	Hardware Cursor	5-38
5.3.1	Hardware Cursor Operation	5-38
5.3.2	Hardware Cursor Programming Example	5-41
5.4	Linear Offset in Tiled Mode	5-66
5.5	Palette	5-71
5.5.1	Programming the 8-bpp LUT.....	5-71
5.5.2	Programmable 6- or 8-bit Palette Entries	5-73
5.6	System-Level Considerations	5-73
5.6.1	Using Other Display Adapters	5-73
5.6.2	Using Multiple CL-GD546Xs	5-74
5.6.3	Monitor Identification	5-74
6.	BIOS SPECIFICATION	6-2
6.1	Requirements	6-2
6.1.1	Software and Hardware Environments.....	6-2
6.1.2	Support Capabilities	6-2
6.1.3	VGA BIOS Functions.....	6-5
6.1.4	VESA® BIOS Extended Functions	6-7
6.1.5	Cirrus Logic Specific BIOS Functions	6-8
6.1.6	Mode Switching	6-8
6.1.7	Register Mapping	6-9
6.2	SCRATCHPAD Register Usage	6-10
6.2.1	DDC Implementation	6-11
6.3	VGA BIOS	6-11
6.3.1	Overview	6-11
6.3.2	BIOS Configurations.....	6-12
6.3.3	Video BIOS Interrupt Vectors.....	6-14
6.3.4	INT10h: BIOS Video Function Contents.....	6-16
6.3.5	Description of Functions.....	6-19
6.3.6	Function: 0Bh	6-26
6.3.7	Function: 10h.....	6-28
6.3.8	Function: 11h.....	6-34

6.3.9	Function: 12h	6-46
6.3.10	Function: 13h — Write Teletype String	6-49
6.3.11	Function: 1Ah	6-50
6.3.12	Function: 1Bh — Collection of Video Information	6-51
6.3.13	Function: 1Ch	6-55
6.4	VGA Sleep Mode and Display Switching	6-57
6.4.1	Memory Map	6-57
6.5	VESA® BIOS Extensions	6-63
6.5.1	VBE Mode Numbers	6-63
6.5.2	VBE Functions	6-66
6.5.3	VBE Return Status	6-66
6.5.4	Protected Mode Considerations	6-66
6.6	Description of VESA®/VBE Functions	6-67
6.6.1	Description of the VbeInfoBlock Structure Fields	6-68
6.6.2	VBE Display PM (Power Management) Functions	6-84
6.6.3	VBE Display Identification (DDC) Functions	6-87
6.7	Cirrus Logic BIOS Extensions	6-90
6.7.1	Inquire VGA Type	6-90
6.7.2	Inquire BIOS Version Number	6-90
6.7.3	Inquire Cirrus Logic Design Revision Code	6-91
6.7.4	Return Installed Memory	6-91
6.7.5	Inquire User Options	6-92
6.7.6	Query Video Mode Availability	6-93
6.7.7	Read Monitor ID/Type	6-93
6.7.8	Set Monitor Type (Vertical)	6-94
6.7.9	Set Monitor Type (Horizontal)	6-95
6.7.10	Generic Fixup	6-96
6.7.11	Frame Buffer Set/Get Physical Address	6-96
6.7.12	Set/Get Memory-Mapped Registers	6-97
6.7.13	Enable_Tiled_Mode	6-97
6.7.14	Get FIFO/Format	6-98
6.8	Extended Modes in RAM	6-98
6.8.1	Extensions to the Save Area Table	6-98
6.9	BIOS Processing	6-99
6.10	Extended Mode Supplemental Parameters	6-99