Appendix A1

Connector Pins

CONNECTOR PINS

Table A1-2. VGA DB15

Pin Number	Standard VGA	DDC2B
1	Analog RED	Analog RED
2	Analog GREEN	Analog GREEN
3	Analog BLUE	Analog BLUE
4	Monitor ID 2	Monitor ID 2
5	n/c	DDC return
6	Analog RED return	Analog RED return
7	Analog GREEN return	Analog GREEN return
8	Analog BLUE return	Analog BLUE return
9	n/c	V_{CC} supply (optional)
10	Digital ground	Digital ground
11	Monitor ID 0	Monitor ID 0
12	Monitor ID 1	Data: SDA
13	HSYNC	HSYNC
14	VSYNC	VSYNC
15	n/c	Clock: SCL

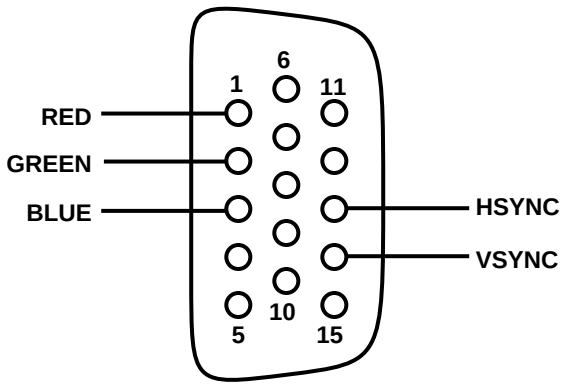
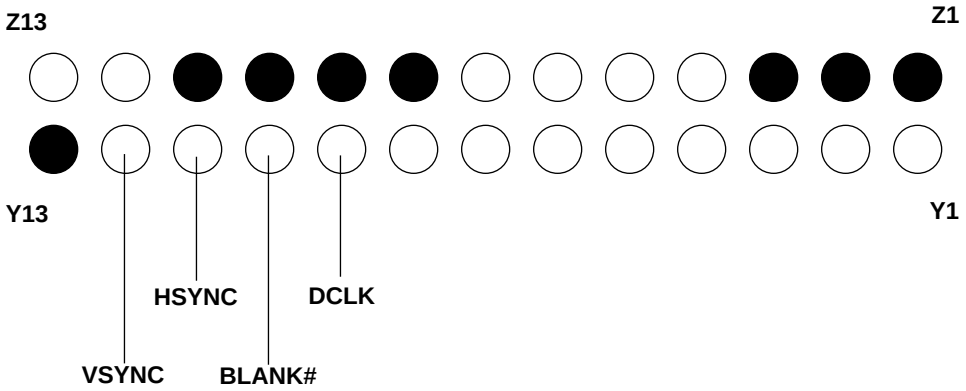


Figure A1-2. VGA DB15 Pin Connections

Table A1-3. VESA® Pass-Through Connector

Number	Z	Y
1	Ground	P[0]
2	Ground	P[1]
3	Ground	P[2]
4	EVIDEO#	P[3]
5	ESYNC#	P[4]
6	EDCLK#	P[5]
7	I^2C Clock[a]	P[6]
8	Ground	P[7]
9	Ground	DCLK
10	Ground	BLANK*
11	Ground	HSYNC
12	VCLK	VSYNC
13	I^2C Data[a]	Ground

[a] These pins are reserved by VESA.



NOTE: Ground pins are shown in black.
The connector is rotated 180 degrees on the PCI reference design.

Figure A1-3. VESA® Pin Connections – View from Component Side

Table A1-4. PCI Bus

Pin	Side B	Side A	Pin	Side B	Side A
1	–12V (not used)	TRST# (not used)	32	AD[17]	AD[16]
2	TCK (not used)	+12 V (not used)	33	C/BE[2]#	+3.3 V (optional)
3	Ground	TMS (not used)	34	Ground	FRAME#
4	TDO (not used)	TDI (not used)	35	IRDY#	Ground
5	+5 V	+5 V	36	+3.3 V (optional)	TRDY#
6	+5 V	INTA#	37	DEVSEL#	Ground
7	INTB# (not used)	INTC# (not used)	38	Ground	STOP#
8	INTD# (not used)	+5 V	39	LOCK#	+3.3 V (optional)
9	PRSNT1#	Reserved	40	PERR# (not used)	SDONE (not used)
10	Reserved	+VIO (not used)	41	+3.3 V (optional)	SBO# (not used)
11	PRSNT2#	Reserved	42	SERR# (not used)	Ground
12	Ground	Ground	43	+3.3 V (optional)	PAR
13	Ground	Ground	44	C/BE[1]#	AD[15]
14	Reserved	Reserved	45	AD[14]	+3.3 V (optional)
15	Ground	RST#	46	Ground	AD[13]
16	CLK	+VIO (not used)	47	AD[12]	AD[11]
17	Ground	GNT# (not used)	48	AD[10]	Ground
18	REQ# (not used)	Ground	49	Ground	AD[09]
19	+VIO (not used)	Reserved	50	(Connector key)	(Connector key)
20	AD[31]	AD[30]	51	(Connector key)	(Connector key)
21	AD[29]	+3.3 V (optional)	52	AD[08]	C/BE[0]#
22	Ground	AD[28]	53	AD[07]	+3.3V (optional)
23	AD[27]	AD[26]	54	+3.3 V (optional)	AD[06]
24	AD[25]	Ground	55	AD[05]	AD[04]
25	+3.3 V (optional)	AD[24]	56	AD[03]	Ground
26	C/BE[3]#	IDSEL	57	Ground	AD[02]
27	AD[23]	+3.3 V (optional)	58	AD[01]	AD[00]
28	Ground	AD[22]	59	+VIO (not used)	+VIO (not used)
29	AD[21]	AD[20]	60	ACK64# (not used)	REQ64# (not used)
30	AD[19]	Ground	61	+5 V	+5 V
31	+3.3 V (optional)	AD[18]	62	+5 V	+5 V

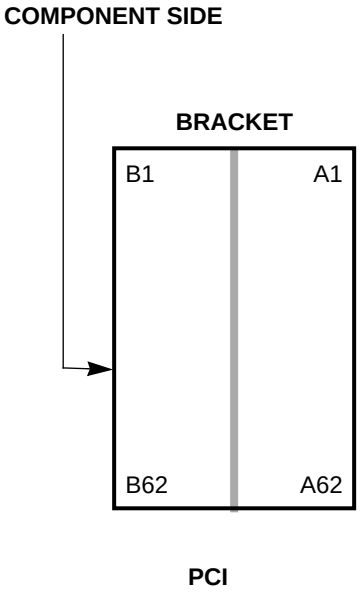


Figure A1-4. PCI Bus Pin Connections – View from Component Side

