3. FUNCTIONAL DESCRIPTION

3.1 General

The CL-GD546X embodies all the necessary hardware for a flexible multimedia display system, including an integrated palette DAC, clock generators, Enhanced V-Port bus for easy expandability, glueless PCI host interface, glueless Rambus Channels, and a 64-bit graphics engine featuring standard GUI acceleration hardware (such as BitBLT, color expansion, 3D engine, and hardware cursor). The CL-GD546X also offers advanced features such as stretch BitBLT and line acceleration, a general-purpose I/O port for expansion, video playback scaling, and color-space conversion for video applications.

Figure 3-1 shows the CL-GD546X connection to the host, monitor, and memory.

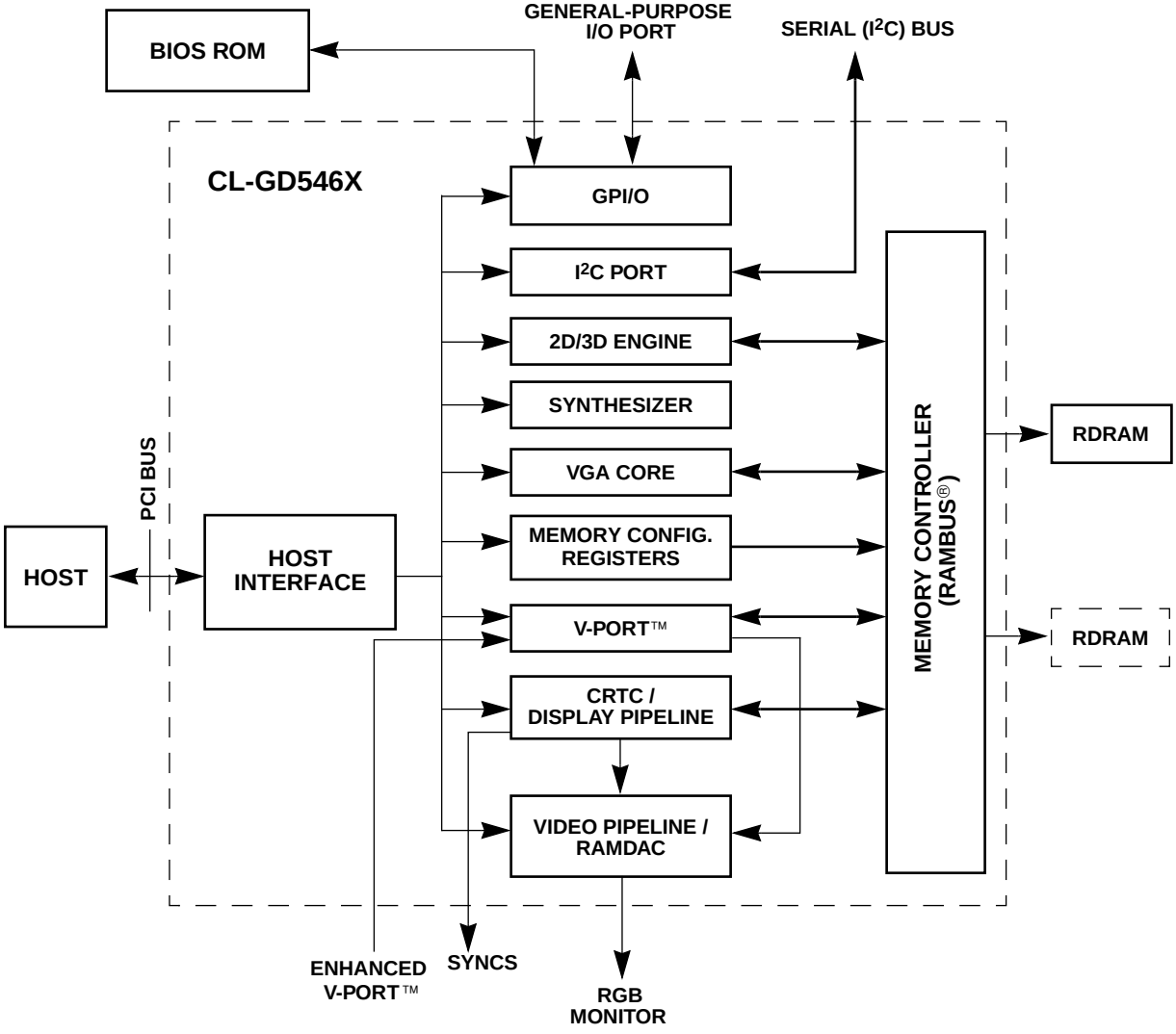

Figure 3-1. CL-GD546X Block Diagram

The CL-GD546X is a high-performance VisualMedia™ solution based on the latest Rambus technology. The CL-GD5462 and CL-GD5464 use one of two Rambus Channels providing 500 to 600 Mbytes/second of memory bandwidth, displaying true-color images at up to 1024 × 768 resolution, and 256-color modes that can reach a maximum of 1600 × 1200 resolution.

3.2 Functional Blocks

The following sections describe the functional blocks that are integrated into the CL-GD546X.

3.2.1 Host Interface

The CL-GD546X host interface offers PCI v2.1-compliant zero-wait-state burst write support up to 33 MHz, and meets single electrical load requirements by buffering the BIOS ROM and local peripheral bus. The CL-GD546X host interface implements byte-swapping on a WORD or DWORD basis for bi-endian support. There is no need for external glue logic because the CL-GD546X host interface decodes all 32 bits of address space. It also incorporates an eight-level command/data buffer that improves host throughput by releasing the CPU as soon as the command or data is written into the buffer.

The CL-GD5464 performs as a bus master to fetch instructions and parameters for the 3D engine and to allow texture, depth, and color data to be stored in system memory. Bus master accesses offer zero-wait-state read burst and write burst support for efficient use of the PCI bus.

3.2.2 2D Graphics Engine (CL-GD5462)

The 2D graphics engine in the CL-GD546X is an advanced 64-bit-three operand engine that accelerates BitBLTs as well as line draws, polygon draw, and polygon fill. The 2D engine is a fast single-cycle 75-MHz engine, matching the 600 Mbytes/second Rambus data speed that provides 8 bits of data every 1.67 ns (64 bits of data every 13.33 ns). This provides twice the bandwidth of most other graphics engines that require 32 ns to process 64 bits of data.

There is also hardware support in the 2D engine for color expansion in 8-, 16-, 24-, and 32-bpp modes. The CL-GD546X 2D engine performs video scaling with a stretch BLT feature that takes off-screen video data and scales it before placing it in on-screen memory. The data can be overlayed with video using color-key or chroma-key compares. This allows the on-screen memory to contain a homogeneous image. The CL-GD5464 supports YUV-to-RGB color-space conversion during the stretch.

The 2D engine incorporates a 25-entry command and data queue to further improve throughput by releasing both the host CPU and the Laguna host interface as soon as the command or data is recorded.

3.2.3 3D Graphics Engine (CL-GD5464)

The 3D graphics engine incorporated in the CL-GD5464 can draw randomly oriented triangles with Gouraud shading, texture mapping, alpha blending, and Z-buffering. The CL-GD5464 has support for copy, DECAL, and blended 2D/3D and modulated textures as well as bilinear, bilinear mip mapped, and trilinear textures. The 3D graphics engine uses PCI bus mastering to fetch instructions and parameters from system memory to render scenes with a minimum of host intervention.

3.2.4 Memory Controller (Rambus®)

The unique CL-GD546X memory controller is the gateway to the Rambus interface, offering up to 600 Mbytes per second bandwidth per channel. It efficiently allocates the memory bandwidth among the functions: CPU access, DRAM refresh, screen refresh, 2D/3D engine operations, and the Enhanced V-Port access. The CL-GD5462 and CL-GD5464 memory controllers are designed to manage a single Rambus Channel; however, some future members of the CL-GD546X family will take full advantage of both Rambus Channels.

3.2.5 VGA Core

The CL-GD546X VGA core is an independent unit that shares the memory bus and host interface with the other components of the CL-GD546X. It is enabled only during VGA modes and is totally compatible with the IBM VGA standard, supporting video modes 0h through 13h. A strapping option disables the VGA core, allowing operation as a grayscale controller.

3.2.6 Enhanced V-Port™ Bus

The V-Port interfaces directly to video decoders including multistandard TV decoder, MPEG decoder, video codec, C-CUBE® CL480 MPEG decoder. In addition, it can interface with other video peripherals compatible with the VGA advance feature connector interface.

Depending on the interface mode, video data is overlaid directly on the graphics display or stored into off-screen memory for scaling and frame rate conversion.

3.2.7 RAMDAC

The CL-GD546X RAMDAC contains the LUT (lookup table) as well as the true color digital-to-analog converter. The CL-GD546X RAMDAC supports 8-bpp LUT mode and Direct Data modes for 8-, 16-, and 24-bpp, along with Alpha channel support in 32-bpp modes. The color values in the LUT can be individually addressed, providing for gamma correction.

3.2.8 Video Pipeline

The CL-GD546X video pipeline is the data path from the frame buffer to the RAMDAC. It contains the YUV-to-RGB automatic data converter. The converter can be switched off on a pixel-by-pixel basis. This allows the frame buffer to contain mixed data types, each pixel being interpreted as YUV or RGB as appropriate.

3.2.9 Programmable Frequency Synthesizer

There are two programmable frequency synthesizers integrated into the CL-GD546X. One synthesizer generates the Rambus clock (250-MHz nominal frequency), and the other synthesizer generates the video clock and CRT controller timing reference (up to 170 MHz for the CL-GD5462 and up to 230 MHz for the CL-GD5464). Both clock synthesizers are programmable and use a 14.31818-MHz external source reference.

3.2.10 CRT Controller

The CL-GD546X CRTC (CRT controller) handles all screen-refresh activity and generates monitor timing signals (HSYNC and VSYNC) and BLANK#. It coordinates the fetching of data from the display memory and delivers it to the DACs for screen refresh. The CRTC also controls the hardware cursor.

3.2.11 I^2C Port

The CL-GD546X offers an I^2C interface, supporting VESA® DDC levels 1 and 2B. The CL-GD546X I^2C port is a software-programmable port that can also control external devices such as an NTSC decoder or a television tuner. This allows software to change channels on a TV tuner or provide setup information for a video decoder.

3.2.12 General-Purpose I/O Port (PCI Configuration)

The pins used to access the BIOS ROM can be configured to serve as a general-purpose I/O port. When a general-purpose I/O port is configured, the CL-GD546X provides hardware pins, PCI address decoding, and remapping of the device's registers into PCI memory address space. This allows a second device on an add-in card without violating the PCI bus single-load requirement. This does not interfere with the BIOS ROM.

3.3 Functional Operation

The following sections discuss the seven major operations handled by the CL-GD546X.

3.3.1 2D Graphics Engine

The CL-GD546X host accesses the registers within the 2D graphics engine to program the desired function. The host interface buffers the operation parameters in its command buffers, releasing the CPU to continue other tasks. To relieve traffic congestion on internal buses, a secondary buffer in the 2D engine also buffers commands and data. When the 2D engine completes the current operation, the parameters are transferred to the registers from this secondary queue to start the next graphics operation.

3.3.2 3D Graphics (CL-GD5464)

The host CPU constructs display lists containing 3D control and rendering instructions and stores them into host system memory. The CL-GD5464 then fetches the display lists from host system memory by becoming a PCI bus master and executing them to render the desired scene. The CL-GD5464 has a rich instruction set including rendering primitives such as DRAW_LINE, DRAW_POLYGON, and BitBLT; flow-control instructions such as BRANCH, CALL, and RETURN; animation-support instructions. The CL-GD5464 can provide status in the form of interrupts when it has reached an arbitrary point in the display list.

3.3.3 Display Refresh

The CL-GD546X CRTC controls and initiates display refresh cycles. The CRTC first fetches the data from the frame buffer by arbitrating for the memory bus. Once the access is granted, as much as of a scanline as can fit is fetched and buffered in the display FIFO to be passed to the RAMDAC for display on the monitor. Programmed for a specific display mode, the rate and timing at which display refresh operations occurs is controlled by the CRTC. A large display FIFO allows large Rambus transactions, reducing the overhead of memory data fetches and conflicts in the Rambus arbitrator.

3.3.4 Playback and Capture by the V-Port™ Bus

The CL-GD546X has a 24-bit V-Port bus that allows the display of video overlay. The CL-GD546X has a data path into the frame buffer, allowing for capture and scaling. Video capture is done by copying video data to an off-screen area. It can then be written to a hard disk. Video scaling is done by fetching the video data from off-screen memory, then scaling and writing the data into the on-screen portion of the frame buffer in actual display size. The CRTC can then fetch the video data to the DAC by the YUV-to-RGB converter if necessary. Finally, the DAC converts the video data to the analog RGB signal for direct connection to the monitor.

3.3.5 Playback by the Host Bus

Another alternative to playback video data is using the host bus on the CL-GD546X. To use this alternative, video data must be written to the off-screen frame buffer area. After the video data is in the off-screen portion of the frame buffer, it is used in exactly the same manner as data gathered by the V-Port bus.

3.3.6 I^2C Port Access (DDC/External Device Control)

The I^2C port implemented in the CL-GD546X is a generic data line and clock line connected to register bits. The data and clock are controlled by software changes to the register contents, which change the outputs. By using the correct software driver, the I^2C port can be used to send or receive any single-bit data format. VESA DDC level 2B signalling is supported with the CL-GD546X BIOS. To communicate to other devices, such as multistandard decoder, special drivers can be written to work with the I^2C port.

3.3.7 BIOS Read

For compliance with the PCI single load specification, the BIOS access must be buffered and accessed with address and data pins. The BIOS ROM is read once during the computer boot process and shadowed in system memory. Once this is complete, the general-purpose I/O port can be used.

The VESA VL-Bus is not supported by the CL-GD546X.

3.4 Performance Notes

The CL-GD546X is designed with the following performance-enhancing features:

- A 64-bit 2D graphics engine with three-operand BitBLT, color expansion for 8-, 16-, 24-, and 32-bpp modes, stretch BLT, transparent BLT, and linedraw acceleration.
- The CL-GD5464 contains a 3D graphics engine capable of rendering triangles with texture mapping, Gouraud shading, alpha blending, and Z-buffering.
- BitBLT operations stored in frame buffer display list and triggerable on command or following any scanline of screen refresh.
- Video playback acceleration with bi-linear interpolated scaling, up to three occluded video windows simultaneously, and YUV-to-RGB conversion. Frame rate conversion is done automatically by Laguna™ hardware.
- Integrated 230-MHz (170 MHz on CL-GD5462) palette DAC, clock synthesizer, and hardware cursor, supporting non-interlaced resolutions up to 1600 × 1200.
- Rambus® memory architecture allowing up to 600 Mbytes/second bandwidth and a frame buffer up to 8 Mbytes at increments of 1 Mbyte.
- 32-bit configurable host interface compliant with PCI v2.1 standards.
- Memory-Mapped registers, linear addressable frame buffer, bi-endian data format support, and 5- or 3.3-V host interface.
- Enhanced V-Port™ bus and general-purpose I/O port support for multimedia expansion.
- VESA® DDC level 2B-compliant monitor signalling.
- Green PC support with VESA® DPMS and system power down.

3.5 Compatibility

The CL-GD5462 includes all registers and data paths required for VGA controllers, and supports extensions to VGA, including resolutions up to 1024 × 768 × 16.8 million colors non-interlaced. The CL-GD546X displays true-color images at up to 1024 × 768 resolution, and 256-color modes can reach a maximum of 1600 × 1200 resolution.

3.6 Board Testability

The CL-GD546X device is testable, even when installed on a printed circuit board. By using the pin-scan testing, any IC signal pin not connected to the board or shorted to a neighboring pin or trace, is detected. The signature generator allows the entire system, including the display memory, to be tested at operating speed.