

---

# *Contents*

---



## Table of Contents

<b>1.</b>	<b>INTRODUCTION .....</b>	<b>1-2</b>
1.1	Scope of Document .....	1-2
1.2	Device Types Covered .....	1-2
1.3	Intended Audience .....	1-2
1.4	Conventions .....	1-3
1.4.1	Numeric Naming .....	1-5
<b>2.</b>	<b>OVERVIEW .....</b>	<b>2-2</b>
2.1	Features .....	2-2
2.2	Chip Architecture .....	2-4
2.2.1	Introduction .....	2-4
2.2.2	Host Interface.....	2-5
2.2.3	2D/3D Graphics Engine .....	2-6
2.2.4	Rambus® Interface .....	2-9
2.2.5	VGA Core and Extended I/O.....	2-10
2.2.6	Display Pipeline and Display FIFO .....	2-11
2.2.7	Enhanced V-Port™.....	2-11
2.2.8	Palette DAC .....	2-11
2.2.9	Programmable Synthesizers.....	2-12
2.2.10	CRT Controller .....	2-13
2.2.11	I <sup>2</sup> C (Serial) Port.....	2-13
2.2.12	General-Purpose I/O Port (PCI Configuration) .....	2-14
2.3	Hardware/Software Compatibility .....	2-14
2.4	Graphics Subsystem Architecture .....	2-15
<b>3.</b>	<b>VGA CORE REGISTERS .....</b>	<b>3-2</b>
3.1	MISC: Miscellaneous Output Register .....	3-5
3.2	FC: Feature Control Register .....	3-7
3.3	FEAT: Input Status Register 0 .....	3-8
3.4	STAT: Input Status Register 1 .....	3-9
3.5	Pixel Mask Register .....	3-10
3.6	Palette Address Register (Read Mode, Write Only) .....	3-11
3.7	DAC State Register (Read Only) .....	3-12
3.8	Palette Address Register (Write Mode, Write Only) .....	3-13
3.9	Pixel Data Register .....	3-14
3.10	SRX: Sequencer Index Register .....	3-15
3.11	SR0: Sequencer Reset Register .....	3-16
3.12	SR1: Sequencer Clocking Mode Register .....	3-17
3.13	SR2: Sequencer Plane Mask Register .....	3-18
3.14	SR3: Sequencer Character Map Select Register .....	3-19
3.15	SR4: Sequencer Memory Mode Register .....	3-21
3.16	CRX: CRTC Index Register .....	3-22
3.17	CR0: CRTC Horizontal Total Register .....	3-25

3.18	CR1: CRTC Horizontal Display End Register .....	3-26
3.19	CR2: CRTC Horizontal Blanking Start Register .....	3-27
3.20	CR3: CRTC Horizontal Blanking End Register .....	3-28
3.21	CR4: CRTC Horizontal Sync Start Register .....	3-29
3.22	CR5: CRTC Horizontal Sync End Register .....	3-30
3.23	CR6: CRTC Vertical Total Register .....	3-31
3.24	CR7: CRTC Overflow Register .....	3-32
3.25	CR8: CRTC Screen A Preset Row-Scan Register .....	3-33
3.26	CR9: CRTC Character Cell Height Register .....	3-34
3.27	CRA: CRTC Text Cursor Start Register .....	3-35
3.28	CRB: CRTC Text Cursor End Register .....	3-36
3.29	CRC: CRTC Screen Start Address High Register .....	3-37
3.30	CRD: CRTC Screen Start Address Low Register .....	3-38
3.31	CRE: CRTC Text Cursor Location High Register .....	3-39
3.32	CRF: CRTC Text Cursor Location Low Register .....	3-40
3.33	CR10: CRTC Vertical Sync Start Register .....	3-41
3.34	CR11: CRTC Vertical Sync End Register .....	3-42
3.35	CR12: CRTC Vertical Display End Register .....	3-43
3.36	CR13: CRTC Offset Register .....	3-44
3.37	CR14: CRTC Underline Row Scanline Register .....	3-45
3.38	CR15: CRTC Vertical Blank Start Register .....	3-46
3.39	CR16: CRTC Vertical Blank End Register .....	3-47
3.40	CR17: CRTC Mode Control Register .....	3-48
3.41	CR18: CRTC Line Compare Register .....	3-50
3.42	CR22: Graphics Data Latches Readback Register .....	3-51
3.43	CR24: Attribute Controller Toggle Readback Register .....	3-52
3.44	CR26: Attribute Controller Index Readback Register .....	3-53
3.45	GRX: Graphics Controller Index Register .....	3-54
3.46	GR0: Graphics Controller Set/Reset Register .....	3-55
3.47	GR1: Graphics Controller Set/Reset Enable Register .....	3-56
3.48	GR2: Graphics Controller Color Compare Register .....	3-57
3.49	GR3: Graphics Controller Data Rotate Register .....	3-58
3.50	GR4: Graphics Controller Read Map Select Register .....	3-59
3.51	GR5: Graphics Controller Mode Register .....	3-60
3.52	GR6: Graphics Controller Miscellaneous Register .....	3-62
3.53	GR7: Graphics Controller Color Don't Care Register .....	3-63
3.54	GR8: Graphics Controller Bit Mask Register .....	3-64
3.55	ARX: Attribute Controller Index Register .....	3-65
3.56	AR0-ARF: Attribute Controller Palette Registers .....	3-66
3.57	AR10: Attribute Controller Mode Register .....	3-67
3.58	AR11: Overscan (Border) Color Register .....	3-69
3.59	AR12: Color Plane Enable Register .....	3-70

3.60	AR13: Pixel Panning Register .....	3-71
3.61	AR14: Color Select Register .....	3-72
<b>4.</b>	<b>EXTENDED I/O REGISTERS .....</b>	<b>4-2</b>
4.1	PCI00: PCI Vendor ID Register .....	4-4
4.2	PCI02: PCI Device ID Register .....	4-5
4.3	PCI04: PCI Command Register .....	4-6
4.4	PCI06: PCI Status Register .....	4-8
4.5	PCI08: PCI Revision ID Register .....	4-9
4.6	PCI09: PCI Class Code Register .....	4-10
4.7	PCI0D: PCI Master Latency Timer Register (CL-GD5464 only) .....	4-11
4.8	PCI0E: PCI Header Type Register .....	4-12
4.9	PCI10: PCI MMI/O Base Address Register .....	4-13
4.10	PCI14: PCI Frame Buffer Base Address Register .....	4-14
4.11	PCI2C: PCI Subsystem Vendor ID Register .....	4-15
4.12	PCI2E: PCI Subsystem ID Register .....	4-16
4.13	PCI30: PCI Expansion ROM Base Address Enable Register .....	4-17
4.14	PCI3C: PCI Interrupt Line Register .....	4-18
4.15	PCI3D: PCI Interrupt Pin Register .....	4-19
4.16	PCIF8: PCI VGA Shadow Register .....	4-20
4.17	PCIFC: PCI Vendor Specific Control Register .....	4-21
4.18	SR6: Unlock I/O Extensions Register .....	4-24
4.19	SR7: Extended Sequencer Mode Register .....	4-25
4.20	SR9, SRA, SR14, SR15: Scratch Pad 0, 1, 2, 3 Registers .....	4-26
4.21	SR0B, SR0C, SR0D, SR0E: Denominator and Post-Scalar Registers .....	4-27
4.22	SR18: Signature Generator Control Register .....	4-28
4.23	SR19, SR1A: Signature Generator Result Registers .....	4-30
4.24	SR1B, SR1C, SR1D, SR1E: VCLK 0, 1, 2, 3 Numerator Registers .....	4-31
4.25	GR9: Offset Register 0 .....	4-32
4.26	GRA: Offset Register 1 .....	4-33
4.27	GRB: Graphics Controller Mode Extensions Register .....	4-34
4.28	CR19: CRTIC Interlace End Register .....	4-35
4.29	CR1A: CRTIC Miscellaneous Control Register .....	4-36
4.30	CR1B: CRTIC Extended Display Control Register .....	4-37
4.31	CR1D: CRTIC Screen Start A Extension Register .....	4-39
4.32	CR1E: CRTIC Timing Overflow Register .....	4-40
4.33	CSL: Current Scanline Register (CL-GD5464 Only) .....	4-41
4.34	CSLC: Current Scanline Comparison Register (CL-GD5464 Only) .....	4-42
4.35	SSA: Secondary Start Address Register (CL-GD5464 Only) .....	4-43
4.36	Multi-Buffering Control Register (CL-GD5464 Only) .....	4-44
4.37	TLUT_LOAD Register (CL-GD5464 Only) .....	4-45
<b>5.</b>	<b>VIDEO PIPELINE REGISTERS .....</b>	<b>5-2</b>
5.1	Palette State Register .....	5-3
5.2	External Overlay Control Register .....	5-5

5.3	Color Key Register .....	5-6
5.4	Color Key Mask Register .....	5-7
5.5	Graphics/Video Format Register .....	5-8
5.6	START_BLT_3 Register .....	5-11
5.7	STOP_BLT_3 Register .....	5-12
5.8	X_START_2 Register .....	5-13
5.9	Y_START_2 Register .....	5-14
5.10	X_END_2 Register .....	5-15
5.11	Y_END_2 Register .....	5-16
5.12	START_BLT_2 Register .....	5-17
5.13	STOP_BLT_2 Register .....	5-18
5.14	START_BLT_1 Register .....	5-19
5.15	STOP_BLT_1 Register .....	5-20
5.16	CURSOR_X Register .....	5-21
5.17	CURSOR_Y Register .....	5-22
5.18	Cursor_Preset Register .....	5-23
5.19	Miscellaneous_Control Register .....	5-24
5.20	Cursor_Address Register .....	5-25
5.21	Display Threshold and Tiling Control Register .....	5-26
5.22	Miscellaneous Test Register .....	5-27
5.23	Test Horizontal Counter Register .....	5-29
5.24	Test Vertical Counter Register .....	5-30
<b>6.</b>	<b>ENHANCED V-PORT™ REGISTERS .....</b>	<b>6-2</b>
6.1	Buffer 0 X Address Register .....	6-3
6.2	Buffer 1 X Address Register .....	6-4
6.3	Buffer 0 Y Address Register .....	6-5
6.4	Buffer 1 Y Address Register .....	6-6
6.5	Capture X Start Register .....	6-7
6.6	Capture X Stop Register .....	6-8
6.7	Capture Y Start Register .....	6-9
6.8	Capture Y Stop Register .....	6-10
6.9	V-Port™ Control Register (CL-GD5462 Only) .....	6-11
6.10	V-Port™ Mode Register (CL-GD5464 Only) .....	6-14
6.11	Video Y Start Register (CL-GD5464 Only) .....	6-19
6.12	Test Output Register (CL-GD5464 Only) .....	6-20
<b>7.</b>	<b>RAMBUS® REGISTERS .....</b>	<b>7-2</b>
7.1	RIF Control Register .....	7-3
7.2	RAC Control Register .....	7-5
7.3	Rambus® Transaction Register .....	7-7
7.4	Rambus® Data Register .....	7-8
<b>8.</b>	<b>2D GRAPHICS ACCELERATOR REGISTERS .....</b>	<b>8-2</b>
8.1	ALPHA_{A,B} Register .....	8-4
8.2	BITMASK Register .....	8-5

8.3	BLTDEF Register .....	8-6
8.4	BLTEXT_EX, BLTEXT_XEX Registers .....	8-9
8.5	BLTEXTFF_EX, BLTEXTFF_XEX Registers .....	8-10
8.6	BLTEXTR_EX, BLTEXTR_XEX Registers .....	8-11
8.7	CHROMA_CNTL Register .....	8-12
8.8	CHROMA_LOWER Register .....	8-14
8.9	CHROMA_UPPER Register .....	8-15
8.10	COMMAND Register .....	8-16
8.11	CONTROL Register .....	8-17
8.12	DRAWDEF Register .....	8-19
8.13	HOST_DATA_PORT Register .....	8-20
8.14	LNCNTL Register .....	8-21
8.15	MAJ{X,Y}, MIN{X,Y}, ACCUM{X,Y} Registers .....	8-23
8.16	MBLTEXT_EX, MBLTEXT_XEX Registers .....	8-24
8.17	MBLTEXTR_EX, MBLTEXTR_XEX Registers .....	8-25
8.18	MONOQW Register .....	8-26
8.19	OFFSET_2D Register .....	8-27
8.20	OP_opBGCOLOR Register .....	8-28
8.21	OP_opFGCOLOR Register .....	8-29
8.22	OP{0-2}_opMRDRAM Registers .....	8-30
8.23	OP{1-2}_opMSRAM Registers .....	8-31
8.24	OP{0-2}_opRDRAM Registers .....	8-32
8.25	OP{0-2}_opSRAM Registers .....	8-33
8.26	PATOFF Register .....	8-34
8.27	QFREE Register .....	8-35
8.28	RESIZE{A-C}_opRDRAM Registers .....	8-36
8.29	SHRINKINC Register .....	8-37
8.30	SRCX Register .....	8-38
8.31	STATUS Register .....	8-39
8.32	STRETCH_CNTL Register .....	8-40
8.33	TAG_MASK Register .....	8-44
8.34	TILE_CTRL Register .....	8-45
8.35	TIMEOUT Register .....	8-46
<b>9.</b>	<b>3D GRAPHICS ACCELERATOR REGISTERS .....</b>	<b>9-2</b>
9.1	3D Drawing Registers .....	9-3
9.1.1	X_3D Register.....	9-5
9.1.2	Y_3D Register.....	9-6
9.1.3	R_3D Register .....	9-7
9.1.4	G_3D Register .....	9-8
9.1.5	B_3D Register.....	9-9
9.1.6	DX_MAIN_3D Register.....	9-10
9.1.7	Y_COUNT_3D Register.....	9-11

9.1.8	WIDTH1_3D Register .....	9-12
9.1.9	WIDTH2_3D Register .....	9-13
9.1.10	DWIDTH1_3D Register.....	9-14
9.1.11	DWIDTH2_3D/DY_MAIN_3D Register .....	9-15
9.1.12	DR_MAIN_3D Register.....	9-16
9.1.13	DG_MAIN_3D Register.....	9-17
9.1.14	DB_MAIN_3D Register.....	9-18
9.1.15	DR_ORTHO_3D Register.....	9-19
9.1.16	DG_ORTHO_3D Register.....	9-20
9.1.17	DB_ORTHO_3D Register.....	9-21
9.1.18	Z_3D Register.....	9-22
9.1.19	DZ_MAIN_3D Register .....	9-23
9.1.20	DZ_ORTHO_3D Register .....	9-24
9.1.21	V_3D Register.....	9-25
9.1.22	U_3D Register .....	9-26
9.1.23	DV_MAIN_3D Register.....	9-27
9.1.24	DU_MAIN_3D Register.....	9-28
9.1.25	DV_ORTHO_3D Register .....	9-29
9.1.26	DU_ORTHO_3D Register.....	9-30
9.1.27	D2V_MAIN_3D Register .....	9-31
9.1.28	D2U_MAIN_3D Register.....	9-32
9.1.29	D2V_ORTHO_3D Register .....	9-33
9.1.30	D2U_ORTHO_3D Register.....	9-34
9.1.31	DV_ORTHO_ADD_3D Register .....	9-35
9.1.32	DU_ORTHO_ADD_3D Register .....	9-36
9.1.33	A_3D Register.....	9-37
9.1.34	DA_MAIN_3D Register.....	9-38
9.1.35	DA_ORTHO_3D Register.....	9-40
9.1.36	OPCODE_3D Register .....	9-42
9.2	3D Engine Control Registers .....	9-43
9.2.1	CONTROL_MASK_3D Register .....	9-44
9.2.2	CONTROL0_3D Register .....	9-47
9.2.3	COLOR_MIN_BOUNDS_3D Register .....	9-52
9.2.4	COLOR_MAX_BOUNDS_3D Register .....	9-55
9.2.5	CONTROL1_3D Register .....	9-56
9.2.6	BASE0_ADDR_3D Register .....	9-57
9.2.7	BASE1_ADDR_3D Register .....	9-59
9.2.8	TX_CTL0_3D Register.....	9-60
9.2.9	TX_XYBASE_3D Register.....	9-67
9.2.10	TX_CTL1_3D Register.....	9-68
9.2.11	TX_CTL2_3D Register.....	9-69
9.2.12	COLOR_REG0_3D Register .....	9-70
9.2.13	COLOR_REG1_3D Register .....	9-71
9.2.14	Z_COLLIDE_3D Register .....	9-72
9.2.15	STATUS0_3D Register.....	9-73

9.2.16	X_CLIP_3D Register.....	9-74
9.2.17	Y_CLIP_3D Register.....	9-75
9.2.18	TEX_SRAM_CTL_3D Register.....	9-76
9.3	Pattern RAM Registers .....	9-77
9.3.1	PATTERN_RAM_0_3D Register .....	9-81
9.3.2	PATTERN_RAM_1_3D Register .....	9-83
9.3.3	PATTERN_RAM_2_3D Register .....	9-84
9.3.4	PATTERN_RAM_3_3D Register .....	9-85
9.3.5	PATTERN_RAM_4_3D Register .....	9-86
9.3.6	PATTERN_RAM_5_3D Register .....	9-87
9.3.7	PATTERN_RAM_6_3D Register .....	9-88
9.3.8	PATTERN_RAM_7_3D Register .....	9-89
9.4	HostXY Unit Registers .....	9-90
9.4.1	HXY_BASE0_ADDRESS_PTR_3D Register .....	9-91
9.4.2	HXY_BASE0_START_3D Register .....	9-92
9.4.3	HXY_BASE0_EXTENT_3D Register.....	9-93
9.4.4	HXY_BASE1_ADDRESS_PTR_3D Register .....	9-94
9.4.5	HXY_BASE1_OFFSET0_3D Register.....	9-95
9.4.6	HXY_BASE1_OFFSET1_3D Register.....	9-96
9.4.7	HXY_BASE1_LENGTH_3D Register .....	9-97
9.4.8	HXY_HOST_CTRL_3D Register .....	9-98
9.5	Mailbox Registers .....	9-100
9.5.1	MAILBOX0_3D Register .....	9-101
9.5.2	MAILBOX1_3D Register .....	9-102
9.5.3	MAILBOX2_3D Register .....	9-103
9.5.4	MAILBOX3_3D Register .....	9-104
9.6	Prefetch Unit Registers .....	9-105
9.6.1	PF_BASE_ADDR_3D Register.....	9-106
9.6.2	PF_CTL_3D Register.....	9-107
9.6.3	PF_DEST_ADDR_3D Register.....	9-109
9.6.4	PF_FB_SEG_3D Register .....	9-110
9.6.5	PF_INST_ADDR_3D Register .....	9-111
9.6.6	PF_STATUS_3D Register .....	9-112
9.6.7	HOST_MASTER_CTL_3D Register .....	9-114
9.6.8	PF_INST_3D Register .....	9-117
9.7	Host Address Registers .....	9-118
9.7.1	HOST_3D_DATA_PORT Register .....	9-119
9.7.2	HOST_TEXTURE_DATA_PORT Register .....	9-120
<b>10.</b>	<b>MISCELLANEOUS REGISTERS .....</b>	<b>10-2</b>
10.1	BCLK Multiplier Register .....	10-3
10.2	GPIO Timing Register .....	10-4
10.3	GPIO Data Register .....	10-6
10.4	GPIO Configuration Register .....	10-7
10.5	Serial Bus (I <sup>2</sup> C) Register .....	10-9

## Appendixes

<b>A1</b>	<b>CONNECTOR PINS .....</b>	<b>A1-2</b>
<b>B1</b>	<b>LAYOUT GUIDELINES .....</b>	<b>B1-2</b>
	1. INTRODUCTION .....	B1-2
	2. REFERENCE DESIGNS .....	B1-2
	3. PARTS PLACEMENT.....	B1-2
	3.1 PCI Bus Adapter Card .....	B1-2
	3.2 Motherboard .....	B1-3
	4. POWER.....	B1-4
	5. GROUND.....	B1-5
	6. DECOUPLING CAPACITORS .....	B1-6
	7. RGB LINES .....	B1-6
	8. RAMBUS® CHANNELS .....	B1-7
	8.1 Physical Layout .....	B1-7
	8.2 CL-GD546X Layout .....	B1-7
	8.3 Rambus® Channel Clock .....	B1-10
	8.4 RDRAM Array .....	B1-11
	8.5 Expansion Socket .....	B1-11
	8.6 Terminators .....	B1-11
	8.7 VTERM and VREF Generation .....	B1-12
	8.8 Controlled Characteristic Impedance Traces .....	B1-13
	8.9 Board Stacking .....	B1-14
	8.10 PCB Design Rules .....	B1-15
	8.11 PCB Geometry .....	B1-17
	8.11.1 Rambus® Channel Layout .....	B1-17
	8.11.2 Coplanar Waveguide (Serpentine) Clock Trace .....	B1-18
	8.11.3 Component Side Clock Routing.....	B1-20
	8.11.4 External Rambus® Clock Generator Circuit Layout.....	B1-20
	8.11.5 VTERM Layout.....	B1-22
	8.12 Notes .....	B1-23
	8.13 Checklist .....	B1-24
<b>B2</b>	<b>PCI BUS REFERENCE DESIGN .....</b>	<b>B2-2</b>
	1. INTRODUCTION .....	B2-2
	2. PCI BUS INTERFACE.....	B2-2
	2.1 Bus Connections .....	B2-2
	2.2 INTA# Pin .....	B2-3
	2.3 VGA BIOS .....	B2-3
	3. DISPLAY MEMORY INTERFACE.....	B2-3
	3.1 Memory Configurations .....	B2-3
	3.2 Rambus® Access Channel Design .....	B2-3
	4. MONITOR INTERFACE .....	B2-4
	4.1 RGB Lines .....	B2-4
	4.2 Sync Lines .....	B2-4

	4.3	Monitor ID .....	B2-4
	5.	VESA® CONNECTOR .....	B2-5
	5.1	Standard VESA® Interface .....	B2-5
	5.2	Enhanced V-Port™ .....	B2-5
	5.3	I <sup>2</sup> C Interface .....	B2-5
	6.	POWER DISTRIBUTION AND CONDITIONING .....	B2-6
	6.1	Introduction .....	B2-6
	6.2	Dedicated Ground Plane .....	B2-6
	6.3	Dedicated Power Plane .....	B2-6
	6.4	Power Bypassing .....	B2-7
	6.5	Power Conditioning .....	B2-7
	6.6	Configuration Resistors .....	B2-8
	6.7	Synthesizer Reference .....	B2-8
	6.8	Current Reference .....	B2-8
<b>B3</b>		<b>CONFIGURATION NOTES .....</b>	<b>B3-2</b>
	1.	INTRODUCTION .....	B3-2
	2.	CONFIGURATION SUMMARY .....	B3-2
	3.	CONFIGURATION DETAILS .....	B3-3
<b>B4</b>		<b>SIGNATURE GENERATOR .....</b>	<b>B4-2</b>
	1.	INTRODUCTION .....	B4-2
	2.	REGISTER SR18: SIGNATURE GENERATOR CONTROL.....	B4-2
	3.	SAMPLE CODE.....	B4-4
<b>B5</b>		<b>PIN SCAN .....</b>	<b>B5-2</b>
	1.	INTRODUCTION .....	B5-2
	2.	TEST METHOD.....	B5-2
	2.1	Entering Pin-Scan Mode: CL-GD5462 .....	B5-2
	2.2	Exiting Pin-Scan Mode: CL-GD5462 .....	B5-2
	2.3	Entering Pin-Scan Mode: CL-GD5464 .....	B5-2
	2.4	Exiting Pin-Scan Mode: CL-GD5464 .....	B5-2
	3.	PIN SCAN ORDER.....	B5-3
<b>B6</b>		<b>MANUFACTURING TEST .....</b>	<b>B6-2</b>
	1.	MANUFACTURING TEST PROGRAM .....	B6-2
	1.1	Operating Instructions .....	B6-2
	1.2	Installing and Starting MFGTST.EXE .....	B6-2
	1.2.1	Command Line Options .....	B6-3
	1.3	Using the MFGTEST Program .....	B6-4
	1.3.1	Using the Special Keystrokes .....	B6-4
	1.4	Listing the Manufacturing Tests .....	B6-6
	1.4.1	Manufacturing Test Groups .....	B6-8
	1.5	Manufacturing Test Updates .....	B6-19
<b>B7</b>		<b>GENERAL-PURPOSE I/O PORT .....</b>	<b>B7-2</b>
	1.	INTRODUCTION .....	B7-2
	2.	CONFIGURATION .....	B7-2
	3.	PIN DEFINITIONS.....	B7-4
	3.1	GPIO Data Register .....	B7-5

<b>C1</b>	<b>SOFTWARE SUPPORT .....</b>	<b>C1-2</b>
1.	INTRODUCTION .....	C1-2
2.	CL-GD546X SOFTWARE UTILITIES.....	C1-2
2.1	CLMODE — A CL-GD546X Video Mode Configuration Utility .....	C1-2
2.2	RAMBIOS.COM — RAMBIOS Utility .....	C1-2
2.3	MFGTST.EXE — Manufacturing Test Utility .....	C1-3
2.4	REG.EXE — A Register Utility .....	C1-3
2.5	OEMSI (OEM System Integration) Utility .....	C1-4
2.6	WINMODE Utility .....	C1-4
3.	CL-GD546X SOFTWARE DRIVERS.....	C1-5
3.1	Driver Applicability .....	C1-5
<b>C2</b>	<b>VIDEO SUPPORT .....</b>	<b>C2-2</b>
1.	INTRODUCTION .....	C2-2
2.	FUNCTIONAL DESCRIPTION.....	C2-2
2.1	Video Capture .....	C2-3
2.2	Resize BitBLTs and Auto-BitBLTs .....	C2-4
2.3	Windows .....	C2-4
2.4	Mixed Frame Buffer .....	C2-6
2.5	Pixel Reformatting During Stretch BitBLTs .....	C2-6
2.6	Timing Overview .....	C2-8
3.	VIDEO CAPTURE AND OVERLAY PINS.....	C2-10
3.1	Capture Mode .....	C2-11
3.2	Feature Connector Mode .....	C2-12
3.2.1	Feature Connector Output Mode .....	C2-12
3.2.2	Feature Connector Input Mode.....	C2-12
3.2.3	Feature Connector Dynamic Overlay Mode.....	C2-12
4.	REGISTERS.....	C2-12
4.1	Introduction .....	C2-12
4.2	Video Pipeline Registers .....	C2-12
4.2.1	Overlay Control Register.....	C2-13
4.2.2	Color Key and Color Key Mask Registers.....	C2-13
4.2.3	Graphics/Video Format Register.....	C2-14
4.2.4	Window 2 Descriptor Registers (X,Y_START,END_2).....	C2-14
4.2.5	Auto-BitBLT Enable Registers (START,STOP_BLT_1,2,3).....	C2-15
4.3	Enhanced V-Port™ Registers .....	C2-16
4.3.1	V-Port™ Control .....	C2-16
4.3.2	Capture Buffer Start.....	C2-16
4.3.3	Capture Buffer Size.....	C2-17
4.4	Graphics Accelerator Registers .....	C2-17
4.4.1	RSIZE{A-C}_opRDRAM.....	C2-17
4.5	Auto-BitBLT Header .....	C2-18
<b>C3</b>	<b>CIRRUS LOGIC BBS, FTP, WWW .....</b>	<b>C3-2</b>
1.	BULLETIN BOARD SERVICE (BBS) .....	C3-2
1.1	Introduction .....	C3-2

	1.2 Telephone Number and Communication Parameters .....	C3-2
	1.3 First-Time Logon .....	C3-2
	1.4 Upgraded Access .....	C3-3
	1.5 Organization of the BBS .....	C3-3
	2. ANONYMOUS FTP SITE .....	C3-4
	3. WWW PAGE .....	C3-4
<b>D1</b>	<b>DATA BOOK .....</b>	<b>D1-ii</b>
<b>E1</b>	<b>GLOSSARY .....</b>	<b>E1-2</b>
	<b>BIBLIOGRAPHY .....</b>	<b>E1-12</b>

**Indexes**

	<b>REGISTER INDEX .....</b>	<b>F-2</b>
	<b>INDEX .....</b>	<b>F-7</b>

