3D Graphics Accelerator Registers

9. 3D GRAPHICS ACCELERATOR REGISTERS

This register interface is used to program the CL-GD5464 as either a programmed I/O device (registers are written followed by commands), or to set up an Instruction Fetch (Display List) mode. In Instruction Fetch mode, the prefetch engine is programmed to point to a region of host system memory that contains a stream of commands (register loads, flow control, and drawing operations). The CL-GD5464 uses the PCI Bus-Mastering mode of operation to retrieve and execute the instruction stream.

Idle/Coprocessor mode 2D and 3D registers are written to program the device to perform indicated 2D and 3D drawing operations.

Instruction Fetch/ or Display List mode System memory-based packets are read by the CL-GD5464 to load its internal registers, and perform indicated 2D and 3D drawing operations.

The 2D Graphics Accelerator register set resides at the top of a 4-Kbyte aperture of memory set by the BASE_ADDRESS_REGISTER_0 in the PCI configuration space. This aperture is 16 Kbytes in length to provide for four different bi-endian data swapping modes. The 3D register set begins at the next 16 Kbytes above the 2D register set (for a total of 32 Kbytes) and is organized as shown in Table 9-1.

Table 9-1. CL-GD5464 Register Apertures

MMI/O Offset	Contents	Format
3D Register Set		
7000h	CL-GD5464 4-Kbyte register aperture	Bytes swapped within dword (byte 0 -> byte 3; byte 1 -> byte 2; byte 2 -> byte 1; byte 3 -> byte 0)
6000h	CL-GD5464 4-Kbyte register aperture	Bytes swapped within dword (same as above)
5000h	CL-GD5464 4-Kbyte register aperture	Bytes swapped within words
4000h[a]	CL-GD5464 4-Kbyte register aperture	No swapping (default)
2D Register Set		
3000h	CL-GD5462 4-Kbyte aperture	Bytes swapped within dword (byte 0-> byte 3; byte 1->byte 2; byte 2-> byte 1; byte 3-> byte 0)
2000h	CL-GD5462 4-Kbyte aperture	Bytes swapped within dword (same as above)
1000h	CL-GD5462 4-Kbyte aperture	Bytes swapped within words
0000h	CL-GD5462 4-Kbyte aperture	No swapping

[a] In this section, the 4000h aperture is used generically to represent 3D register locations.

9.1 3D Drawing Registers

The 3D Drawing registers are listed in Table 9-2 in MMI/O offset order. A detailed register description is also provided in offset order.

Refer to the *Laguna VisualMedia™ Accelerators Family — CL-GD546X Volume II (Software Reference Manual, Second Edition, September 1996)*, "3D Programmer's Guide" chapter for Draw Instruction register parameter tables.

Naming convention: 'D' prefix means the register value is used in a DDA engine at each step of the engine.

Table 9-2. 3D Drawing Registers

Register Name	Description	Format[a]	MMI/O Offset	Page
X_3D	Initial X value (X at base point) plus control bits	11.16	4000h	9-5
Y_3D	Initial Y value (Y at base point) plus control bits	11.16	4004h	9-6
R_3D	Initial Red color component value	8.16	4008h	9-7
G_3D	Initial Green color component value	8.16	400Ch	9-8
B_3D	Initial Blue color component value	8.16	4010h	9-9
DX_MAIN_3D	X_Main delta value	12.16	4014h	9-10
Y_COUNT_3D	Y Count2: Y Count1 concatenated	x.11.x.11	4018h	9-11
WIDTH1_3D	Initial width for drawing Area1 of a polygon	11.16	401Ch	9-12
WIDTH2_3D	Initial width for drawing Area2 of a polygon	11.16	4020h	9-13
DWIDTH1_3D	Area1 width delta value	s.12.16	4024h	9-14
DWIDTH2_3D/ DY_MAIN_3D	Area2 width delta value for polygons, Y_Main delta value for lines	s.12.16/ 1.16	4028h	9-15
DR_MAIN_3D	R_Main delta value	s.9.16	402Ch	9-16
DG_MAIN_3D	G_Main delta value	s.9.16	4030h	9-17
DB_MAIN_3D	B_Main delta value	s.9.16	4034h	9-18
DR_ORTHO_3D	R_Ortho delta value	s.9.16	4038h	9-19
DG_ORTHO_3D	G_Ortho delta value	s.9.16	403Ch	9-20
DB_ORTHO_3D	B_Ortho delta value	s.9.16	4040h	9-21
Z_3D	Initial Z value (depth at base point)	16.16	4044h	9-22
DZ_MAIN_3D	Z_Main delta value	s.16.16	4048h	9-23
DZ_ORTHO_3D	Z_Ortho value	s.16.16	404Ch	9-24
V_3D	Initial V value (V at texture base point)	9.16	4050h	9-25
U_3D	Initial U value (U at texture base point)	9.16	4054h	9-26

Table 9-2. 3D Drawing Registers *(cont.)*

Register Name	Description	Format[a]	MMI/O Offset	Page
DV_MAIN_3D	V_Main delta value	s.10.16	4058h	9-27
DU_MAIN_3D	U_Main delta value	s.10.16	405Ch	9-28
DV_ORTHO_3D	V_Ortho delta value	s.10.16	4060h	9-28
DU_ORTHO_3D	U_Ortho delta value	s.10.16	4064h	9-30
D2V_MAIN_3D	V2_Main delta value	s.10.16	4068h	9-31
D2U_MAIN_3D	U2_Main delta value	s.10.16	406Ch	9-32
D2V_ORTHO_3D	V2_Ortho delta value	s.10.16	4070h	9-33
D2U_ORTHO_3D	U2_Ortho delta value	s.10.16	4074h	9-34
DV_ORTHO_ADD_3D	DV_Ortho_Add value	s.10.16	4078h	9-35
DU_ORTHO_ADD_3D	DU_Ortho_Add value	s.10.16	407Ch	9-36
A_3D	Initial A value (alpha at base point)	8.8	40C0h	9-37
DA_MAIN_3D	A_Main delta value plus constant A bits	s.9.8	40C4h	9-38
DA_ORTHO_3D	A_Ortho delta value plus constant A bits	s.9.8	40C8h	9-40
OPCODE_3D	Opcode for execution/polygon engine	32	40FCh	9-42

[a] In format column, a '11.16' value indicates integer (value before the decimal) and fraction (value after the decimal) portion of the register.
An 'x' indicates reserved, and an 's' indicates a Sign bit that can be included in the integer value.

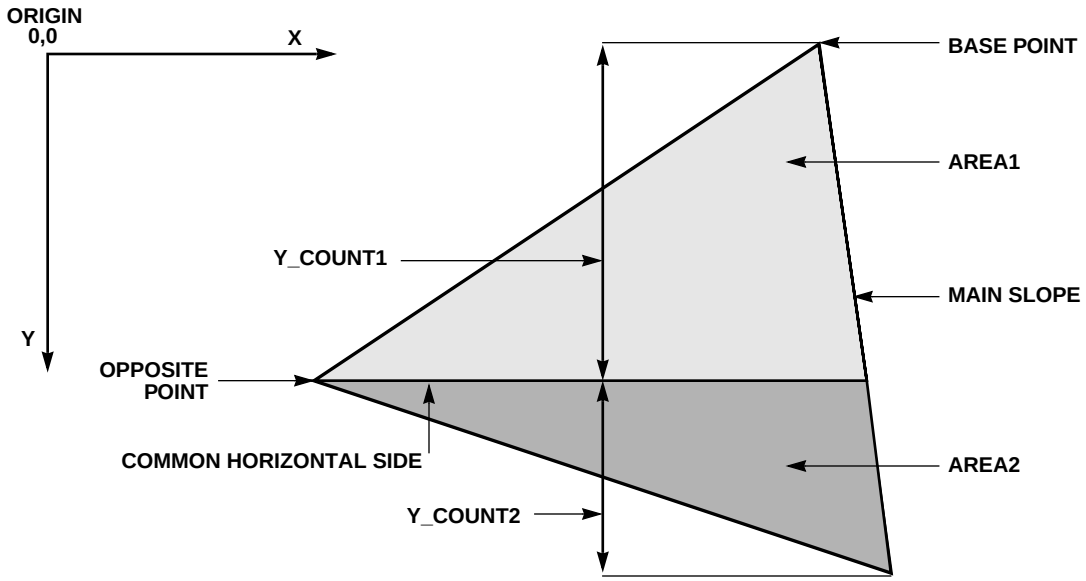


Figure 9-1. CL-GD5464 General Terminology and Definitions for Triangles

9.1.1 X_3D Register

Size (bits):	32
MMI/O Offset	4000h
Access Type	Read/Write

Bit	Description
31	X Direction
30	Left Edge Disable
29	Right Edge Disable
28:27	Reserved
26:16	X_Int
15:0	X_Frac

This register specifies the X value of the initial pixel coordinate or base point for drawing points, lines, and polygons. That is, the X_Main accumulator initial value. This register also controls the direction of drawing from the main slope and controls drawing of the leftmost and rightmost pixels in a span. For polygons, the base point represents the (upper) leftmost or rightmost pixel of the first span, depending on the X Direction bit (bit 31). It is the first point drawn in a line or polygon.

Bit	Description
31	**X Direction:** This bit sets the direction of span drawing. If this bit is set to '1', spans of a polygon are drawn in decreasing values of X from the main slope. If this bit is set to '0', spans are drawn in increasing values of X.
30	**Left Edge Disable:** If this bit is set to '1', the leftmost (least X valued) pixel of each span in X is not drawn. If this bit is set to '0', the leftmost pixel of each span is drawn. This bit only affects drawing of polygons.
29	**Right Edge Disable:** If this bit is set to '1', the rightmost (greatest X valued) pixel of each span in X is not drawn. If this bit is set to '0', the rightmost pixel of each span is drawn. This bit only affects drawing of polygons.
28:27	**Reserved**
26:16	**X_Int:** These bits set the integer portion of X value at the base point. Integer is in the range of 0 to 2047.
15:0	**X_Frac:** These bits set the fractional portion of X value at the base point.

9.1.2 Y_3D Register

Size (bits):	32
MMI/O Offset	4004h
Access Type	Read/Write

Bit	Description
31	Reserved
30	Top Edge Disable
29	Bottom Edge Disable
28:27	Reserved
26:16	Y_Int
15:0	Y_Frac

This register specifies the Y value of the initial pixel coordinate or base point for drawing points or lines and drawing polygons. For polygons, the base point represents the (upper) leftmost or rightmost pixel of the first span, depending on the X Direction bit (bit 31) in the X_3D register. It is the first point drawn in a line or polygon.

Bit	Description
31	**Reserved**
30	**Top Edge Disable:** If this bit is set to '1', the topmost (least Y valued) pixel of a line or polygon is not drawn. If this bit is set to '0', the topmost pixel is drawn.
29	**Bottom Edge Disable:** If this bit is set to '1', the bottommost (greatest Y valued) pixel of a line or polygon is not drawn. If this bit is set to '0', the bottommost pixel is drawn.
28:27	**Reserved**
26:16	**Y_Int:** These bits set the integer portion of Y value at the base point. Integer is in the range of 0 to 2047.
15:0	**Y_Frac:** These bits set the fractional portion of Y value at the base point.

9.1.3 R_3D Register

Size (bits):	32
MMI/O Offset	4008h
Access Type	Read/Write

Bit	Description
31:24	Reserved
23:16	R_Int
15:0	R_Frac

This register specifies the red color or red lighting value at the base point. That is, the R_Main accumulator initial value. The R_Main accumulator represents a mapped color when in 8-bpp mode. The R_Main accumulator is used for lighting when the polygon engine is selected by the Light_Src_Sel field (bits 26:25) of the CONTROL0_3D register.

Bit	Description
31:24	**Reserved:** These bits are always ‘0h’.
23:16	**R_Int:** These bits set the integer portion of red color value at the base point. Integer is in the range of 0 to 255.
15:0	**R_Frac:** These bits set the fractional portion of red color value at the base point.

9.1.4 G_3D Register

Size (bits):	32
MMI/O Offset	400Ch
Access Type	Read/Write

Bit	Description
31:23	Reserved
23:16	G_Int
15:0	G_Frac

This register specifies the green color or green lighting value at the base point (not loaded when in 8-bpp mode). That is, the G_Main accumulator initial value. The G_Main accumulator is used for lighting when the polygon engine is selected by the Light_Src_Sel field (bits 26:25) of the CONTROL0_3D register.

Bit	Description
31:24	**Reserved:** These bits are always ‘0h’.
23:16	**G_Int:** These bits set the integer portion of green color value at the base point. Integer is in the range of 0 to 255.
15:0	**G_Frac:** These bits set the fractional portion of green color value at the base point.

9.1.5 B_3D Register

Size (bits):	32
MMI/O Offset	4010h
Access Type	Read/Write

Bit	Description
31:24	Reserved
23:16	B_Int
15:0	B_Frac

This register specifies the blue color or blue lighting value at the base point (not loaded when in 8-bpp mode). That is, the B_Main accumulator initial value. The B_Main accumulator is used for lighting when polygon engine is selected by the Light_Src_Sel field (bits 26:25) of the CONTROL0_3D register.

Refer to Draw Instruction Register Parameter tables to see when this register is needed.

Bit	Description
31:24	**Reserved:** These bits are always ‘0h’.
23:16	**B_Int:** These bits set the integer portion of blue color value at the base point. Integer is in the range of 0 to 255.
15:0	**B_Frac:** These bits set the fractional portion of blue color value at the base point.

9.1.6 DX_MAIN_3D Register

Size (bits):	32
MMI/O Offset	4014h
Access Type	Read/Write

Bit	Description
31:16	DX_Int
15:0	DX_Frac

This register specifies the change in the X value along the main slope of a polygon or along the line. That is, the X_Main accumulator delta value.

For X-major lines, this register should be loaded with a value of +1.0 or –1.0 (10000h or FFFF0000h), and the DWIDTH2_3D/DY_MAIN_3D register loaded with a value between 0.0 and 1.0 (that is, between 0h and 10000h).

For polygons, this register is the amount by which the X position start value for each span in X is adjusted on each step in Y.

Bit	Description
31:16	**DX_Int:** These bits set the signed integer portion of the X_Main delta value. Integer is in the range of –2048 to 2047 (12 bits). Bit 27 is sign-extended to bit 31.
15:0	**DX_Frac:** These bits set the fractional portion of the X_Main delta value.

9.1.7 Y_COUNT_3D Register

Size (bits):	32
MMI/O Offset	4018h
Access Type	Read/Write

Bit	Description
31:27	Reserved
26:16	Y_Count1
15:11	Reserved
10:0	Y_Count2

This register specifies the count in Y for the two possible areas of the polygon. The total height of the polygon is (Y_Count1 + 1 + Y_Count2).

Bit	Description
31:27	**Reserved**
26:16	**Y_COUNT1:** This field represents the number of steps in Y for the first portion (Area1) of a drawn polygon. The number of steps taken is one more than the value programmed. This field is programmed with a value in the range of 0 to 2047.
15:11	**Reserved**
10:0	**Y_COUNT2:** This field specifies the number of steps in Y for the second portion (Area2) of a drawn polygon. If programmed to '0', only Area1 is drawn. This field is programmed with a value in the range of 0 to 2047**.**

9.1.8 WIDTH1_3D Register

Size (bits):	32
MMI/O Offset	401Ch
Access Type	Read/Write

Bit	Description
31:27	Reserved
26:16	Width1_Int
15:0	Width1_Frac

This register specifies the width of the first span in X for the upper portion (Area1) of a polygon. It is the width of the polygon at the base point. That is, the Width1 accumulator initial value.

Bit	Description
31:27	**Reserved**
26:16	**Width1_Int:** These bits set the integer portion of span width at the base point. Value is in the range of 0 to 2047.
15:0	**Width1_Frac:** These bits set the fractional portion of span width at the base point.

9.1.9 WIDTH2_3D Register

Size (bits):	32
MMI/O Offset	4020h
Access Type	Read/Write

Bit	Description
31:27	Reserved
26:16	Width2_Int
15:0	Width2_Frac

This register specifies the width of the first span in X of the lower portion (Area2) of a polygon. It is the width of the polygon at the opposite point. That is, the Width2 accumulator initial value.

Bit	Description
31:27	**Reserved**
26:16	**Width2_Int:** These bits set the integer portion of span width value at the opposite point. Value is in the range of 0 to 2047.
15:0	**Width2_Frac:** These bits set the fractional portion of span width value at the opposite point.

9.1.10 DWIDTH1_3D Register

Size (bits):	32
MMI/O Offset	4024h
Access Type	Read/Write

Bit	Description
31:16	DWidth1_Int
15:0	DWidth1_Frac

This register specifies the change in width along the main slope for the first portion (Area1) of a polygon. That is, the Width1 accumulator delta value.

Refer to Draw Instruction Register Parameter tables to see when this register is needed.

Bit	Description
31:16	**DWidth1_Int:** These bits set the signed integer portion of span width delta value for Area1. Value is in the range of –2048 to 2047 (12 bits). Bit 27 is sign-extended to bit 31.
15:0	**DWidth1_Frac:** These bits set the fractional portion of span width delta value for Area1.

9.1.11 DWIDTH2_3D/DY_MAIN_3D Register

Size (bits):	32
MMI/O Offset	4028h
Access Type	Read/Write

For Drawing Polygons

Bit	Description
31:16	DWidth2_Int
15:0	DWidth2_Frac

For Drawing Lines

Bit	Description
31:17	Reserved
16	DY_Main_Int
15:0	DY_Main_Frac

For polygons, this register specifies the change in width along the main slope for the second portion (Area2) of a polygon. That is, the Width2 accumulator delta value.

For lines, this register specifies the change in Y value for each step in X along the line. For X-major lines, the value should be in the range of 0.0 to 1.0 (0 to 10000h) inclusive with ± 1.0 programmed in the DX_MAIN_3D register. For Y major lines, this register should be programmed to 1.0 (10000h), and a value in the range of 0.0 to ± 1.0 programmed in the DX_MAIN_3D register. Lines (and polygons) are only drawn for increasing values of Y.

For Drawing Polygons

Bit	Description
31:16	**DWidth2_Int:** These bits set the signed integer portion of span width delta value for Area2 of a polygon. Value is in the range of –2048 to 2047 (12 bits). Bit 27 is sign-extended to bit 31.
15:0	**DWidth2_Frac:** These bits set the fractional portion of span width delta value for Area2 of a polygon.

For Drawing Lines

Bit	Description
31:17	**Reserved:** Program these bits to ‘0h’.
16:	**DY_Main_Int:** These bits set the integer portion of change in Y value for each unit step in X along the line. For X-major lines, this bit should be set ‘0’. If this bit is set to ‘1’, the fractional field, the DY_Main_Frac should be programmed to ‘0000h’.
15:0	**DY_Main_Frac:** These bits set the fractional portion of change in Y value for each step in X along the line. For Y-major lines, these bits should be set to ‘0000h’.

9.1.12 DR_MAIN_3D Register

Size (bits):	32
MMI/O Offset	402Ch
Access Type	Read/Write

Bit	Description
31:16	DR_Main_Int
15:0	DR_Main_Frac

This register specifies the change in the red color or red lighting component along the main slope. That is, the R_Main accumulator delta value. This value is the amount by which the red component start value for each span in X is adjusted on each step in Y for the polygon.

The value by which the red component changes for each span step in X is given by the DR_ORTHO_3D register value.

The R_Main accumulator is used for lighting when the polygon engine is selected by the Light_Src_Sel field (bits 26:25) of the CONTROL0_3D register.

Bit	Description
31:16	**DR_Main_Int:** These bits set the signed integer portion of the R_Main delta value. Value is in the range of –256 to 255 (9 bits). Bit 24 is sign-extended to bit 31.
15:0	**DR_Main_Frac:** These bits set the fractional portion of the R_Main delta value.

9.1.13 DG_MAIN_3D Register

Size (bits):	32
MMI/O Offset	4030h
Access Type	Read/Write

Bit	Description
31:16	DG_Main_Int
15:0	DG_Main_Frac

This register specifies the change in the green color or green lighting component along the main slope. That is, the G_Main accumulator delta value. This value is the amount by which the green component start value for each span in X is adjusted on each step in Y for the polygon.

The value by which the green component changes for each span step in X is given by the DG_ORTHO_3D register value.

The G_Main accumulator is used for lighting when the polygon engine is selected by the Light_Src_Sel field (bits 26:25) of the CONTROL0_3D register.

Bit	Description
31:16	**DG_Main_Int:** These bits set the signed integer portion of the G_Main delta value. Value is in the range of –255 to 255 (9 bits). Bit 24 is sign-extended to bit 31.
15:0	**DG_Main_Frac:** These bits set the fractional portion of the G_Main delta value.

9.1.14 DB_MAIN_3D Register

Size (bits):	32
MMI/O Offset	4034h
Access Type	Read/Write

Bit	Description
31:16	DB_Main_Int
15:0	DB_Main_Frac

This register specifies the change in the blue color or blue lighting component along the main slope. That is, the B_Main accumulator delta value. This value is the amount by which the blue component start value for each span in X is adjusted on each step in Y for the polygon.

The value by which the blue component changes for each span step in X is given by the DB_ORTHO_3D register value.

The B_Main accumulator is used for lighting when the polygon engine is selected by the Light_Src_Sel field (bits 26:25) of the CONTROL0_3D register.

Refer to Draw Instruction Register Parameter tables to see when this register is needed.

Bit	Description
31:16	**DB_Main_Int:** These bits set the signed integer portion of the B_Main delta value. Value is in the range of –256 to 255 (9 bits). Bit 24 is sign-extended to bit 31.
15:0	**DB_Main_Frac:** These bits set the fractional portion of the B_Main delta value.

9.1.15 DR_ORTHO_3D Register

Size (bits):	32
MMI/O Offset	4038h
Access Type	Read/Write

Bit	Description
31:16	DR_Ortho_Int
15:0	DR_Ortho_Frac

This register specifies the change in the red color or red lighting component along a span in X that is, the R_Ortho accumulator delta value. This value is the amount by which the red component is adjusted on each step along the X span for the polygon.

The initial value for the span is determined by the R_3D register value and the accumulation of the DR_MAIN_3D register value for each step in Y.

The R_Ortho accumulator is used for lighting when the polygon engine is selected by the Light_Src_Sel field (bits 26:25) of the CONTROL0_3D register.

Bit	Description
31:16	**DR_Ortho_Int:** The 9-bit signed integer portion of R_Ortho delta value. These bits set the signed integer portion of R_Ortho delta value. Value is in the range of –256 to 255 (9 bits). Bit 24 is sign-extended to bit 31.
15:0	**DR_Ortho_Frac:** Fractional portion of R_Ortho delta value. These bits set the fractional portion of R_Ortho delta value.

9.1.16 DG_ORTHO_3D Register

Size (bits):	32
MMI/O Offset	403Ch
Access Type	Read/Write

Bit	Description
31:16	DG_Ortho_Int
15:0	DG_Ortho_Frac

This register specifies the change in the green color or green lighting component along the span in X that is, the G_Ortho accumulator delta value. This value is the amount by which the green component is adjusted on each step along the X span for the polygon.

The initial value for the span is determined by the G_3D register value and the accumulation of the DG_MAIN_3D register value for each step in Y.

The G_Ortho accumulator is used for lighting when the polygon engine is selected by the Light_Src_Sel field (bits 26:25) of the CONTROL0_3D register.

Bit	Description
31:16	**DG_Ortho_Int:** These bits set the signed integer portion of the G_Ortho value. Value is in the range of –256 to 255 (9 bits). Bit 24 is sign-extended to bit 31.
15:0	**DG_Ortho_Frac:** These bits set the fractional portion of the G_Ortho delta value.

9.1.17 DB_ORTHO_3D Register

Size (bits):	32
MMI/O Offset	4040h
Access Type	Read/Write

Bit	Description
31:16	DB_Ortho_Int
15:0	DB_Ortho_Frac

This register specifies the change in the blue color or blue lighting component along a span in X. That is, the B_Ortho accumulator delta value. This value is the amount by which the blue component is adjusted on each step along the X span for the polygon.

The initial value for the span is determined by the B_3D register value and the accumulation of the DB_MAIN_3D register value for each step in Y.

The B_Ortho accumulator is used for lighting when the polygon engine is selected by the Light_Src_Sel field (bits 26:25) of theCONTROL0_3D register.

Bit	Description
31:16	**DB_Ortho_Int:** These bits set the signed integer portion of the B_Ortho delta value. Value is in the range of –256 to 255 (9 bits). Bit 24 is sign-extended to bit 31.
15:0	**DB_Ortho_Frac:** These bits set the fractional portion of the B_Ortho delta value.

9.1.18 Z_3D Register

Size (bits):	32
MMI/O Offset	4044h
Access Type	Read/Write

Bit	Description
31:16	Z_Int
15:0	Z_Frac

This register specifies the Z value at the base point (not loaded when Z buffering is disabled). That is, the Z_Main accumulator initial value.

Bit	Description
31:16	**Z_Int:** These bits set the 16-bit unsigned integer portion of the Z value at the base point. Value is in the range of 0 to 65535. When in 8-bit Z mode (Z_Stride_Control bit of CONTROL0_3D register is set to ‘1’), the values are in the same range, but only bits 31:24 are used to compare with and store into the Z buffer.
15:0	**Z_Frac:** These bits set the fractional portion of the Z value at the base point.

9.1.19 DZ_MAIN_3D Register

Size (bits):	32
MMI/O Offset	4048h
Access Type	Read/Write

Bit	Description
31:16	DZ_Main_Int
15:0	DZ_Main_Frac

This register specifies the change in Z along the main slope. That is, the Z_Main accumulator delta value. This value is the amount by which the Z-start value for each span in X is adjusted on each step in Y for the polygon.

The value by which the Z changes for each span step in X is given by the DZ_ORTHO_3D register value.

Bit	Description
31:16	**DZ_Main_Int:** These bits set the 16-bit signed integer portion of the Z_Main delta value. Value is in the range of −32768 to 32767. When in 8-bit Z mode (Z_Stride_Control bit of CONTROL0_3D register is set to '1'), the values are in the same range, but only bits 31:24 are used to compare with and store into the Z buffer.
15:0	**DZ_Main_Frac:** These bits set the fractional portion of the Z_Main delta value.

9.1.20 DZ_ORTHO_3D Register

Size (bits):	32
MMI/O Offset	404Ch
Access Type	Read/Write

Bit	Description
31:16	DZ_Ortho_Int
15:0	DZ_Ortho_Frac

This register specifies the change in Z along a span in X that is, the Z_Ortho accumulator delta value. This value is the amount by which Z is adjusted on each step along the X span for the polygon.

The initial value for the span is determined by the Z_3D register value and the accumulation of the DZ_MAIN_3D register value for each step in Y.

Bit	Description
31:16	**DZ_Ortho_Int:** These bits set the 16-bit signed integer portion of the Z_Ortho delta value. Value is in the range of –32768 to 32767. When in 8-bit Z mode (Z_Stride_Control bit of CONTROL0_3D register is set to '1'), the values are in the same range, but only bits 31:24 are used to compare with and store into the Z buffer.
15:0	**DZ_Ortho_Frac:** These bits set the fractional portion of the Z_Ortho delta value.

9.1.21 V_3D Register

Size (bits):	32
MMI/O Offset	4050h
Access Type	Read/Write

Bit	Description
31:25	Reserved
24:16	V_Int
15:0	V_Frac

This register specifies the V value for the initial texture coordinate corresponding to the polygon base point that is, the V_Main accumulator initial value. The initial texture coordinate is also called the texture base point.

Bit	Description
31:25	**Reserved**
24:16	**V_Int:** These bits set the integer portion of the V value of texture base point. Value is in the range of 0 to 511.
15:0	**V_Frac:** These bits set the fractional portion of the V value of texture base point.

9.1.22 U_3D Register

Size (bits):	32
MMI/O Offset	4054h
Access Type	Read/Write

Bit	Description
31:25	Reserved
24:16	U_Int
15:0	U_Frac

This register specifies the U value for the initial texture coordinate corresponding to the polygon base point that is, the U_Main accumulator initial value. The initial texture coordinate is also called the texture base point.

Bit	Description
31:25	**Reserved**
24:16	**U_Int:** These bits set the integer portion of the U value of texture base point. Value is in the range of 0 to 511.
15:0	**U_Frac:** These bits set the fractional portion of the U value of texture base point.

9.1.23 DV_MAIN_3D Register

Size (bits):	32
MMI/O Offset	4058h
Access Type	Read/Write

Bit	Description
31:16	DV_Main_Int
15:0	DV_Main_Frac

This register specifies the first-order change in the V value of the texture coordinate along the main slope. That is, the V_Main accumulator first-order delta value.

Bit	Description
31:16	**DV_Main_Int:** These bits set the signed integer portion of the V_Main first-order delta value. Value is in the range of –512 to 511 (10 bits). Bit 25 is sign-extended to bit 31.
15:0	**DV_Main_Frac:** These bits set the fraction portion of the V_Main first-order delta value.

9.1.24 DU_MAIN_3D Register

Size (bits):	32
MMI/O Offset	405Ch
Access Type	Read/Write

Bit	Description
31:16	DU_Main_Int
15:0	DU_Main_Frac

This register specifies the first-order change in the U value of the texture coordinate along the main slope. That is, the U_Main accumulator first-order delta value.

Bit	Description
31:16	**DU_Main_Int:** These bits set the signed integer portion of the U_Main first-order delta value. Value is in the range of –512 to 511 (10 bits). Bit 25 is sign-extended to bit 31.
15:0	**DU_Main_Frac:** These bits set the fractional portion of the U_Main first-order delta value.

9.1.25 DV_ORTHO_3D Register

Size (bits):	32
MMI/O Offset	4060h
Access Type	Read/Write

Bit	Description
31:16	DV_Ortho_Int
15:0	DV_Ortho_Frac

This register specifies the first-order change in the V value of the texture coordinate along a span in X. That is, the V_Ortho accumulator first-order delta value.

Bit	Description
31:16	**DV_Ortho_Int:** These bits set the signed integer portion of the V_Ortho value first-order delta. Value is in the range of –512 to 511 (10 bits). Bit 25 is sign-extended to bit 31.
15:0	**DV_Ortho_Frac:** These bits set the fractional portion of the V_Ortho first-order delta value.

9.1.26 DU_ORTHO_3D Register

Size (bits):	32
MMI/O Offset	4064h
Access Type	Read/Write

Bit	Description
31:16	DU_Ortho_Int
15:0	DU_Ortho_Frac

This register specifies the first-order change in the U value of the texture coordinate along a span in X. That is, the U_Ortho accumulator first-order delta value.

Bit	Description
31:16	**DU_Ortho_Int:** These bits set the signed integer portion of the U_Ortho first-order delta value. Value is in the range of –512 to 511 (10 bits). Bit 25 is sign-extended to bit 31.
15:0	**DU_Ortho_Frac:** These bits set the fractional portion of the U_Ortho first-order delta value.

9.1.27 D2V_MAIN_3D Register

Size (bits):	32
MMI/O Offset	4068h
Access Type	Read/Write

Bit	Description
31:16	D2V_Main_Int
15:0	D2V_Main_Frac

This register specifies the second-order change in the V value of the texture coordinate along the main slope. That is, the V_Main accumulator second-order delta value. This value is only used for perspective-corrected texture maps.

Bit	Description
31:16	**D2V_Main_Int:** These bits set the signed integer portion of the V_Main second-order delta value. Value is in the range of –512 to 511 (10 bits). Bit 25 is sign-extended to bit 31.
15:0	**D2V_Main_Frac:** These bits set the fractional portion of the V_Main second-order delta value.

9.1.28 D2U_MAIN_3D Register

Size (bits):	32
MMI/O Offset	406Ch
Access Type	Read/Write

Bit	Description
31:16	D2U_Main_Int
15:0	D2U_Main_Frac

This register specifies the second-order change in the U value of the texture coordinate along the main slope. That is, the U_Main accumulator second-order delta value. This value is only used for perspective-corrected texture maps.

Bit	Description
31:16	**D2U_Main_Int:** These bits set the signed integer portion of the U_Main second-order delta value. Value is in the range of –512 to 511 (10 bits). Bit 25 is sign-extended to bit 31.
15:0	**D2U_Main_Frac:** These bits set the fractional portion of the U_Main second-order delta value.

9.1.29 D2V_ORTHO_3D Register

Size (bits):	32
MMI/O Offset	4070h
Access Type	Read/Write

Bit	Description
31:16	D2V_Ortho_Int
15:0	D2V_Ortho_Frac

This register specifies the second-order change in the V value of the texture coordinate along a span in X. That is, the V_Ortho accumulator second-order delta value. This value is only used for perspective-corrected texture maps.

Bit	Description
31:16	**D2V_Ortho_Int:** These bits set the signed integer portion of the V_Ortho second-order delta value. Value is in the range of –512 to 511 (10 bits). Bit 25 is sign-extended to bit 31.
15:0	**D2V_Ortho_Frac:** These bits set the fractional portion of the V_Ortho second-order delta value.

9.1.30 D2U_ORTHO_3D Register

Size (bits):	32
MMI/O Offset	4074h
Access Type	Read/Write

Bit	Description
31:16	D2U_Ortho_Int
15:0	D2U_Ortho_Frac

This register specifies the second-order change in the U value of the texture coordinate along a span in X. That is, the U_Ortho accumulator second-order delta value. This value is only used for perspective-corrected texture maps.

Bit	Description
31:16	**D2U_Ortho_Int:** These bits set the signed integer portion of the U_Ortho second-order delta value. Value is in the range of –512 to 511 (10 bits). Bit 25 is sign-extended to bit 31.
15:0	**D2U_Ortho_Frac:** These bits set the fractional portion of the U_Ortho second-order delta value**.**

9.1.31 DV_ORTHO_ADD_3D Register

Size (bits):	32
MMI/O Offset	4078h
Access Type	Read/Write

Bit	Description
31:16	DV_Ortho_Add_Int
15:0	DV_Ortho_Add_Frac

This register specifies the value to be used as the change in the V value of the texture coordinate along a span in X. That is, the V_Ortho accumulator value. This value is only used for perspective-corrected texture maps.

Bit	Description
31:16	**DV_Ortho_Add_Int:** These bits set the signed integer portion of the V_Ortho value. Value is in the range of –512 to 511 (10 bits). Bit 25 is sign-extended to bit 31.
15:0	**DV_Ortho_Add_Frac:** These bits set the fractional portion of the V_Ortho value**.**

9.1.32 DU_ORTHO_ADD_3D Register

Size (bits):	32
MMI/O Offset	407Ch
Access Type	Read/Write

Bit	Description
31:16	DU_Ortho_Add_Int
15:0	DU_Ortho_Add_Frac

This register specifies the value to be used as the change in the U value of the texture coordinate along a span in X. That is, the U_Ortho accumulator value. This value is only used for perspective-corrected texture maps.

Bit	Description
31:16	**DU_Ortho_Add_Int:** These bits set the signed integer portion of U_Ortho. Value is in the range of –512 to 511 (10 bits). Bit 25 is sign-extended to bit 31.
15:0	**DU_Ortho_Add_Frac:** These bits set the fractional portion of the U constant.

9.1.33 A_3D Register

Size (bits):	32
MMI/O Offset	40C0h
Access Type	Read/Write

Bit	Description
31:24	Reserved
23:16	A_Int
15:8	A_Frac
7:0	Reserved

This register specifies the alpha value or lighting value at the base point. That is, the A_Main accumulator initial value.

Bit	Description
31:24	**Reserved:** Program these bits to ‘0h’.
23:16	**A_Int:** These bits set the 8-bit unsigned integer portion of alpha or lighting value at the base point. Value is in the range of 0 to 255.
15:8	**A_Frac:** These bits set the fractional portion of alpha or lighting value at the base point.
7:0	**Reserved:** Program these bits to ‘0h’.

9.1.34 DA_MAIN_3D Register

Size (bits):	32
MMI/O Offset	40C4h
Access Type	Read/Write

Fixed Alpha Modes

Bit	Description
31:25	Reserved
24:16	A_Src_Const
15:0	Reserved

a:8:8:8 Mode

Bit	Description
31:16	A_Main_Int
15:8	A_Main_Frac
7:0	Reserved

When Fixed Alpha mode is selected, this register specifies the source alpha blend constant for the polygon.

When in a:8:8:8 mode or when used for interpolated lighting, this register specifies the change in alpha/lighting value along the main slope. That is, the A_Main accumulator delta value. This value is the amount by which the alpha/lighting start value for each span in X is adjusted on each step in Y for the polygon. The value by which alpha/lighting changes for each span step in X is given by the DA_ORTHO_3D register value.

Fixed Alpha Mode

Bit 31:25 — **Reserved:** Program these bits to ‘0h’.

Bit 24:16 — **A_Src_Const:** The percentage of the source pixel to be blended with the destination pixel to determine the resultant pixel value.

Bits 24:16	Combination percentage
000000000	0 × source pixel (no contribution)
000000001	1 ÷ 256 × source pixel
000000010	2 ÷ 256 × source pixel
000000011	3 ÷ 256 × source pixel
. . .	
011111110	254 ÷ 256 × source pixel
011111111	255 ÷ 256 × source pixel
1xxxxxxxx	1 × source pixel

Bit 15:0 — **Reserved:** Program these bits to ‘0h’.

9.1.34 DA_MAIN_3D Register *(cont.)*

a:8:8:8 Mode or Interpolated Lighting

Bit	Description
31:16	**A_Main_Int:** These bits set the signed integer portion of the A_Main delta value. Value is in the range of –255 to 255 (9 bits). Bit 24 is sign-extended to bit 31.
15:8	**A_Main_Frac:** These bits set the fractional portion of the A_Main delta value.
7:0	**Reserved:** Program these bits to ‘0h’.

9.1.35 DA_ORTHO_3D Register

Size (bits):	32
MMI/O Offset	40C8h
Access Type	Read/Write

Fixed Alpha Modes

Bit	Description
31:25	Reserved
24:16	A_Dest_Const
15:0	Reserved

a:8:8:8 Mode

Bit	Description
31:16	A_Ortho_Int
15:8	A_Ortho_Frac
7:0	Reserved.

When Fixed Alpha mode is selected, this register specifies the destination alpha constant for the polygon.

When a:8:8:8 mode is selected, this register specifies the change in alpha along a span in X. That is, the A_Ortho accumulator delta value. This value is the amount by which alpha is adjusted on each step along the X span for the polygon. The initial value for the span is determined by the A_3D register value and the accumulation of the DA_MAIN_3D register value for each step in Y.

Fixed Alpha Mode

Bit 31:25 — **Reserved:** Program these bits to ‘0h’.

Bit 24:16 — **A_Dest_Const:** The percentage of the destination pixel to be blended with the source pixel to determine the resultant pixel value.

Bits 24:16	Combination percentage
000000000	0 × destination pixel (no contribution)
000000001	1 ÷ 256 × destination pixel
000000010	2 ÷ 256 × destination pixel
000000011	3 ÷ 256 × destination pixel
. . .	
011111110	254 ÷ 256 × destination pixel
011111111	255 ÷ 256 × destination pixel
1xxxxxxxx	1 × destination pixel

Bit 15:0 — **Reserved:** Program these bits to ‘0h’.

9.1.35 DA_ORTHO_3D Register *(cont.)*

a:8:8:8 Mode or Interpolated Lighting

Bit	Description
31:16	**A_Ortho_Int:** These bits set the signed integer portion of the A_Main delta value. Value is in the range of –255 to 255 (9 bits). Bit 24 is sign-extended to bit 31.
15:8	**A_Ortho_Frac:** These bits set the fractional portion of the A_Main delta value.
7:0	**Reserved:** Program these bits to ‘0h’.

9.1.36 OPCODE_3D Register

Size (bits):	32
MMI/O Offset	40FCh
Access Type	Read/Write

Bit	Description
31:0	Opcode

This register specifies the opcode for the 3D execution engine. It is used in the coprocessor direct method of programming.

Bit	Description
31:0	**Opcode:** Only the following opcodes and associated parameters should be written to this register using the coprocessor-direct method. DRAW_POINT DRAW_LINE DRAW_POLY WRITE_REGISTER NOP CLEAR

9.2 3D Engine Control Registers

The 3D Engine Control registers are listed in Table 9-3 in MMI/O offset order. A detailed register description is also provided in offset order.

Table 9-3. 3D Engine Control Registers

Register Name	Description	Format	MMI/O Offset	Page
CONTROL_MASK_3D	Execution/polygon engine control mask bits	??	4100h	9-44
CONTROL0_3D	3D Engine Control 0	??	4104h	9-47
COLOR_MIN_BOUNDS_3D	Color saturation and compare minimum bounds	8.24	4108h	9-52
COLOR_MAX_BOUNDS_3D	Color saturation and compare maximum bounds	8.24	410Ch	9-55
CONTROL1_3D	3D Engine Control 1	32	4110h	9-56
BASE0_ADDR_3D	Base offset address 0	32	4114h	9-57
BASE1_ADDR_3D	Base offset address 1	32	4118h	9-59
Reserved				
TX_CTL0_3D	Texture Control 0	32	4120h	9-60
TX_XYBASE_3D	Texture XY Base Address	32	4124h	9-67
TX_CTL1_3D	Texture Control 1	32	4128h	9-68
TX_CTL2_3D	Texture Control 2	32	412Ch	9-69
COLOR_REG0_3D	Color 0 (used for patterned polygons or fixed alpha)	x.24	4130h	9-70
COLOR_REG1_3D	Color 1 (used for patterned polygons or fixed lighting)	x.24	4134h	9-71
Z_COLLIDE_3D	Z-Collision Detect	x.16	4138h	9-72
STATUS0_3D	Status 0	32	413Ch	9-73
PATTERN_RAM see Section 9.3 on page 9-77			4140h–415Ch	
X_CLIP_3D	Enables and X coordinates of clipping rectangle for drawing	32	4160h	9-74
Y_CLIP_3D	Enables and Y coordinates of clipping rectangle for drawing	32	4164h	9-75
TEX_SRAM_CTL_3D	Texture SRAM Control	??	4168h	9-76

9.2.1 CONTROL_MASK_3D Register

Size (bits):	32
MMI/O Offset	4100h
Access Type	Read/Write

Bit	Description	Reset Value
31	CONTROL_MASK_3D [31]	0
30:29	Reserved	
28	CONTROL_MASK_3D [28:24]	0
23	Reserved	0
22	CONTROL_MASK_3D [22:13]	0
12	Reserved	0
11	CONTROL_MASK_3D [11:3]	0
2:1	Reserved	0
0	CONTROL_MASK_3D [0]	0

This register contains bits that mask write accesses to various fields or single bits in the control registers used by the 3D engine. This mask field is most effective in (Processor mode) for setting a single bit or bit-field value using a mask rather than a read modify write sequence.

NOTE: The register field is write-protected (masked) if set to '1', and writable if set to '0'.

Bit	Description
31	**CONTROL_MASK_3D [31]:** This bit controls bit 31 in the X_CLIP_3D and Y_CLIP_3D registers.
30:29	**Reserved**
28	**CONTROL_MASK_3D [28]:** This bit controls bits 30:28 in the CONTROL0_3D register and bits 31:28 in the TX_CTL0_3D register.
27	**CONTROL_MASK_3D [27]:** This bit controls bit 27 in the TX_CTL1_3D register.
26	**CONTROL_MASK_3D [26]:** This bit controls bit 26 in the TX_CTL1_3D register.
25	**CONTROL_MASK_3D [25]:** This bit controls bits 26:25 in the CONTROL0_3D register and bit 25 in the TX_CTL1_3D register.
24	**CONTROL_MASK_3D [24]:** This bit controls the following bits in the respective registers: Bit 24 in the CONTROL0_3D register; bits 31:24 in the COLOR_MIN_BOUNDS_3D register; bits 31:24 in the COLOR_MAX_BOUNDS_3D register; bits 31:24 in the CONTROL1_3D register; bits 27:24 in the BASE0_ADDR_3D register; bits 25:24 in the TX_CTL0_3D register; and bit 24 in the TX_CTL1_3D register.
23	**Reserved**
22	**CONTROL_MASK_3D [22]:** This bit controls bit 22 in the TX_CTL0_3D register.
21	**CONTROL_MASK_3D [21]:** This bit controls bit 21 in the TX_CTL0_3D register.

9.2.1 CONTROL_MASK_3D Register *(cont.)*

Bit	Description
20	**CONTROL_MASK_3D [20]:** This bit controls bits 23:20 in the CONTROL0_3D register and bit 20 in the TX_CTL0_3D register.
19:17	**CONTROL_MASK_3D [19:17]:** These bits control bits 19:17 in the TX_CTL0_3D register.
16	**CONTROL_MASK_3D [16]:** This bit controls the following bits in the respective registers: Bit 16 in the CONTROL0_3D register; bits 19:16 in the BASE0_ADDR_3D register; bits 28:21 in the BASE1_ADDR_3D register; bit 16 in the TX_CTL0_3D register; bits 28:20 in the TX_XYBASE_3D register; bits 26:16 in the X_CLIP_3D register; and bits 26:16 in the Y_CLIP_3D register.
15	**CONTROL_MASK_3D [15]:** This bit controls the following bits in the respective registers: Bit 15 in the CONTROL0_3D register; bit 15 in the BASE0_ADDR_3D register; bit 15 in the X_CLIP_3D register; and bit 15 in the Y_CLIP_3D register.
14	**CONTROL_MASK_3D [14]:** This bit controls bit 14 in the BASE0_ADDR_3D register.
13	**CONTROL_MASK_3D [13]:** This bit controls bits 14:13 in the CONTROL0_3D register and bit 13 in the BASE0_ADDR_3D register.
12	**Reserved**
11	**CONTROL_MASK_3D [11]:** This bit controls bits 12:11 in the CONTROL0_3D register.
10:9	**CONTROL_MASK_3D [10:9]:** This bit controls bits 10:9 in the CONTROL0_3D register.
8	**CONTROL_MASK_3D [8]:** This bit controls bit 8 in the CONTROL0_3D register and bits 10:8 in the TX_CTL0_3D register.
7	**CONTROL_MASK_3D [7]:** This bit controls bit 7 in the CONTROL0_3D register and bit 7 in the TX_CTL0_3D register.
6	**CONTROL_MASK_3D [6]:** This bit controls bit 6 in the CONTROL0_3D register.
5	**CONTROL_MASK_3D [5]:** This bit controls bit 5 in the CONTROL0_3D register.
4	**CONTROL_MASK_3D [4]:** This bit controls the following bits in the respective registers: Bit 4 in the CONTROL0_3D register; bits 6:4 in the TX_CTL0_3D register; and bits 6:4 in the TEX_SRAM_CTL_3D register.

9.2.1 CONTROL_MASK_3D Register *(cont.)*

Bit	Description
3	**CONTROL_MASK_3D [3]:** This bit controls bit 5 in the TX_CTL0_3D register
2:1	**Reserved**
0	**CONTROL_MASK_3D [0]:** This bit controls the following bits in the respective registers: Bits 2:0 in the CONTROL0_3D register; bits 23:0 in the COLOR_MIN_BOUNDS_3D register; bits 23:0 in the COLOR_MAX_BOUNDS_3D register bits 7:0 in the CONTROL1_3D register bits 12:6 in the BASE0_ADDR_3D register; bits 12:5 in the BASE1_ADDR_3D register; bits 2:0 in the TX_CTL0_3D register; bits 12:5 in the TX_XYBASE_3D register; bits 23:0 in the TX_CTL1_3D register; bits 23:0 in the TX_CTL2_3D register; bits 23:0 in the COLOR_REG0_3D register; bits 23:0 in the COLOR_REG1_3D register; bits 15:0 in the Z_COLLIDE_3D register; bits 10:0 in the X_CLIP_3D register; and bits 10:0 in the Y_CLIP_3D register.

9.2.2 CONTROL0_3D Register

Size (bits):	32
MMI/O Offset	4104h
Access Type	Read/Write

Bit	Description	Mask	Reset Value
31	Reserved		0
30:28	Z_Mode	CONTROL_MASK_3D [28]	0
27	Reserved		0
26:25	Light_Src_Sel	CONTROL_MASK_3D [25]	0
24	Z_Collision_Detect_En	CONTROL_MASK_3D [24]	0
23:20	Z_Compare_Mode	CONTROL_MASK_3D [20]	0
19:17	Reserved		0
16	Z_Stride_Control	CONTROL_MASK_3D [16]	0
15	Alpha_Blending_En	CONTROL_MASK_3D [15]	0
14:13	Alpha_Dest_Color_Select	CONTROL_MASK_3D [13]	0
12:11	Alpha_Mode	CONTROL_MASK_3D [11]	0
10	Color_Compare_Mode	CONTROL_MASK_3D [10]	0
9	Blue_Color_Compare_En	CONTROL_MASK_3D [9]	0
8	Green_Color_Compare_En	CONTROL_MASK_3D [8]	0
7	Red_Color_Compare_en	CONTROL_MASK_3D [7]	0
6	Color_Saturate_En	CONTROL_MASK_3D [6]	0
5	Pixel_Mask_Polarity	CONTROL_MASK_3D [5]	0
4	Pixel_Mask_En	CONTROL_MASK_3D [4]	0
3	Reserved		0
2:0	Pixel_Mode	CONTROL_MASK_3D [0]	0

This register specifies some fundamental operating parameters of the 3D engine. All bits can be protected from write accesses by programming the corresponding bits of CONTROL_MASK_3D register to ‘1’. This allows individual bits or fields to be altered without read-modify-write operations. Note that control registers and bit fields should not be programmed while the drawing engine is busy.

Bit	Description
31	**Reserved:** Always set this bit to ‘0’.

9.2.2 CONTROL0_3D Register *(cont.)*

Bit **Description**

30:28 **Z_Mode:** Controls the Z and color update method during drawing.

Bits 30:28	Z Format	Z Update Method	Color Update Method	Description
111–101	Reserved			Reserved
100	Z_Hit	No update	No update	Sets Z collision flag and records Z hit destination. Uses Z mask field in 4110h to select precision of collision compare.
011	Z_Only	Z_Compare_Mode	No update	Z depth buffer update based on Z_Compare_Mode field of CONTROL0_3D register. Color not written to frame buffer.
010	Z_Always	Always	Always	Z depth always written, color always written to frame buffer regardless of Z compare result.
001	Z_Mask	No update	Z_Compare_ Mode	Z depth read for compare, but not written. Color is written based on Z_Compare_Mode field of CONTROL0_3D register.
000	Z_Normal	Z_Compare_Mode	Z_Compare_ Mode	Normal operating mode. Z_Compare_Mode field of CONTROL0_3D register determines Z and color buffer update policy.

Writes to this field are masked by CONTROL_MASK_3D bit (bit 28).

27 **Reserved:** Always set this bit to ‘0’.

26:25 **Light_Src_Sel**: Selects the lighting source multiplier input, LIGHT_RGB, to the lighting stage.
11 Reserved
10 COLOR_REG1_3D
01 Alpha interpolator (A_Main and A_Ortho accumulators)
00 Polygon engine (with shading, patterning, stipple, or dithering)
Writes to this field are masked by CONTROL_MASK_3D bit (bit 25).
The lighting stage performs the following function when enabled by the Lighting Instruction Modifier bit (bit 18 of the instruction):
LIT_RGB = SOURCE_RGB × LIGHT_RGB

9.2.2 CONTROL0_3D Register *(cont.)*

Bit	Description
24	**Z_Collision_Detect_En:** This bit allows setting a flag based on Z compare equal. When this bit is set to '1', it enables Z collision detection logic. When this bit is set to '0', it disables the Z collision detection logic. Writes to this field are masked by CONTROL_MASK_3D bit (bit 24).
23:20	**Z_Compare_Mode:** These bits control the Z compare function. 1111–0110Reserved 0101 Compare is true if new value == old 0100 Compare is true if new value != old 0011 Compare is true if new value < old 0010 Compare is true if new value ≤ old 0001 Compare is true if new value > old 0000 Compare is true if new value ≥ old Writes to this field are masked by CONTROL_MASK_3D bit (bit 20).
19:17	**Reserved:** Program to '0h'.
16	**Z_Stride_Control:** This bit controls the Z buffer precision. If this bit is set to '1', 8-bit depth values are stored and compared to the Z interpolators. This allows 256 levels of overlay in Z:8:8:8 modes. If this bit is set to '0', 16-bit depth values are stored and compared to the Z interpolators. Writes to this field are masked by CONTROL_MASK_3D bit (bit 16).
15	**Alpha_Blending_En:** If this bit is set to '1', alpha blending is enabled. If this bit is set to '0', alpha blending is disabled. Writes to this field are masked by CONTROL_MASK_3D bit (bit 15).
14:13	**Alpha_Dest_Color_Select:** These bits select the DEST_RGB input to the alpha stage. 11 Reserved 10 Polygon engine (with shading, patterning, stipple, or dither applied as selected) 01 COLOR_REG0_3D 00 Destination data (existing frame buffer data) (when the Fetch_Color Instruction Modifier bit (bit 23) is set) Writes to this field are masked by CONTROL_MASK_3D bit (bit 13)

9.2.2 CONTROL0_3D Register *(cont.)*

Bit	Description
12:11	**Alpha_Mode:** These bits select the Alpha Blending mode when enabled by the Alpha_Blending_En bit (bit 15) of this register. Alpha_Mode selects the SRC_ALPHA and DEST_ALPHA inputs to the alpha blending stage. 11 SRC_ALPHA input is alpha read from the color buffer DEST_ALPHA input is 256 minus alpha read from the color buffer 10 SRC_ALPHA input is from the alpha interpolator DEST_ALPHA input is 256 minus the alpha interpolator 01 Reserved 00 SRC_ALPHA input is A_Src_Const from DA_MAIN_3D register DEST_ALPHA input is A_Dest_Const from DA_ORTHO_3D register Writes to this field are masked by CONTROL_MASK_3D bit (bit 11). The alpha blending stage performs the following function: RGB_OUT = (SRC_ALPHA × LIT_RGB) + (DEST_ALPHA × DEST_RGB) **NOTES:** 1) The alpha interpolator can be used for lighting or for alpha, but not for both. 2) For Alpha_Mode is '00' and SRC_ALPHA is '100h', the RGB_OUT output of the alpha stage is the value of the LIT_RGB input. 3) For Alpha_Mode is '00' and DEST_ALPHA is '100h', the RGB_OUT output is the value of the DEST_RGB input.
10	**Color_Compare_Mode:** This bit controls the Destination Color Compare mode. If this bit is set to '1', the mask is inclusive to bounds. If this bit is set to '0', the mask is exclusive of bounds. Writes to this field are masked by CONTROL_MASK_3D bit (bit 10).
9	**Blue_Color_Compare_En:** This bit controls the enable for the destination color compare of the blue color component. If this bit is set to '1', it enables compares to bounds. If this bit is set to '0', it disables compare to bounds. Writes to this field are masked by CONTROL_MASK_3D bit (bit 9).
8	**Green_Color_Compare_En:** This bit controls the enable for the destination color compare of the green color component. If this bit is set to '1', it enables compare to bounds. If this bit is set to '0', it disables compare to bounds. Writes to this field are masked by CONTROL_MASK_3D bit (bit 8).
7	**Red_Color_Compare_En:** This bit controls the enable for the destination color compare of the red color component. If this bit is set to '1', it enables compare to bounds. If this bit is set to '0', it disables compare to bounds. Writes to this field are masked by CONTROL_MASK_3D bit (bit 7).
6	**Color_Saturate_En:** This bit enables the saturate to color MAX and MIN bounds for 8-bpp Mapped mode. If this bit is set to '1', it enables color saturate to bounds. If this bit is set to '0', it disables color saturate to bounds. Writes to this field are masked by CONTROL_MASK_3D bit (bit 6).

9.2.2 CONTROL0_3D Register *(cont.)*

Bit | **Description**

5 — **Pixel_Mask_Polarity:** This bit only has an effect when enabled by the Pixel_Mask_Enable bit (bit 4) of this register, and when the Fetch_Color Instruction Modifier bit is set and in Pixel_Modes of a:5:5:5 or a:8:8:8. That is, modes which include a bit mask in the pixel. The mask bit for these two modes is either bit 31 in a:8:8:8 mode, or bit 15 in a:5:5:5 mode. If the Pixel_Mask_Polarity bit does not equal the mask bit in the destination data, the pixel does not write to the frame buffer (that is, masked). If these bits are equal, the frame buffer can be updated.

That is, If this bit is '1', the frame buffer pixels with a mask bit of '0' are preserved. Pixels with a mask bit of '1' can be overwritten. If this bit is '0' the frame buffer pixels with a mask bit of '1' are preserved. Pixels with a mask bit of '0' can be overwritten. Writes to this bit are controlled by the CONTROL_MASK_3D bit (bit 5).

4 — **Pixel_Mask_En:** This bit enables operations that use the mask bit of a pixel in the frame buffer. Only applicable for Pixel_Modes that have a mask bit in the pixel. That is, bit in a:8:8:8 mode or a:5:5:5 mode. The destination pixel masking operation depends on the Pixel_Mask_Polarity bit (bit 5).
If this bit is '1', it enables pixel masking when the Fetch_Color Instruction Modifier bit is set. If this bit is '0', it disables pixel masking. The frame buffer data can be overwritten by the 3D engine.
Writes to this bit are controlled by the CONTROL_MASK_3D bit (bit 4).

3 — **Reserved:** Set this bit to '0'.

2:0 — **Pixel_Mode:** Color Frame Buffer Drawing mode.

Bits 2:0	Pixel Data		
	Size (bits)	Format	Description
000	8	Mapped	8-bpp mapped (uses red interpolater)
001	8	3:3:2	8-bpp RGB (3:3:2)
010	16	5:6:5	16-bpp RGB (5:6:5)
011	16	a:5:5:5	16-bpp RGB (5:5:5); bit 15 can be used as a mask
100	32	a:8:8:8	24-bpp RGB (8:8:8) with upper 8 bits unused; bit 31 can be used as a mask
101	32	Z:8:8:8	24-bpp RGB (8:8:8) with 8-bpp Z
110	Reserved		
111	Reserved		

Writes to this field are controlled by CONTROL_MASK_3D bit (bit 0).

9.2.3 COLOR_MIN_BOUNDS_3D Register

Size (bits):	32
MMI/O Offset	4108h
Access Type	Read/Write

Bit	Description	Mask	Reset Value
31:24	Color_Saturate_Min	CONTROL_MASK_3D [24]	0
23:16	Color_Compare_Min (Red)	CONTROL_MASK_3D [0]	0
15:8	Color_Compare_Min (Green)	CONTROL_MASK_3D [0]	0
7:0	Color_Compare_Min (Blue)	CONTROL_MASK_3D [0]	0

This register specifies the minimum bounds for the color saturate and color compare functions.

Bit	Description
31:24	**Color_Saturate_Min (8-bpp modes only):** These bits control the minimum bound value used in color saturate for 8-bpp modes only. See also the enable bit, Color_Saturate_En bit in the CONTROL0_3D register on page 9-47. Writes to this field are controlled by the CONTROL_MASK_3D bit (bit 24).
23:16	**Color_Compare_Min (Red Component):** Since color compares operate at a full 8-bits per component, some bits from 5- and 3-bit red components must be replicated in this field. The following table gives the method for this replication.

Table 9-4. Red Component Color Compare Mapping

Pixel_Mode	Color Compare Value (Red Component)			
	23:21	20:19	18	17:16
24-bpp, a:8:8:8 mode	Bits 23:16 of 32-bit pixel			
16-bpp, 5:6:5 mode	Bits 15:11 of 16-bit pixel		Bits 15:13 of 16-bit pixel	
16-bpp, a:5:5:5 mode	Bits 14:10 of 16-bit pixel		Bits 14:12 of 16-bit pixel	
8-bpp, 3:3:2 mode	Bits 7:5 of 8-bit pixel	Bits 7:5 of 8-bit pixel		Bits 7:6 of 8-bit pixel
8-bpp mapped	Bits 7:0 of 8-bit pixel			

In 24-bpp modes, the 8-bit red component compare value is written to this field. In a:5:5:5 and 5:6:5 16-bit-per-pixel modes, the 5-bit red component compare value should be placed in bits 23:19 and then duplicated in the next three bits. In 8-bpp mode, the upper three bits of the 3:3:2 pixel (the red component) are duplicated through the 8-bit component of this register. This imitates the color unpacking logic. Writes to this field are controlled by the CONTROL_MASK_3D bit (bit 0).

9.2.3 COLOR_MIN_BOUNDS_3D Register *(cont.)*

Bit	Description
15:8	**Color_Compare_Min (Green Component):** Since color compares operate at a full 8-bits per component, some bits from 6-, 5- and 3-bit green components must be replicated in this field. The following table gives the method for this replication.

Table 9-5. Green Component Color Compare Mapping

Pixel_Mode	Color Compare Value (Green Component)			
	15:13	**12:11**	**10**	**9:8**
24-bpp, a:8:8:8 mode	Bits 15:8 of 32-bit pixel			
16-bpp, 5:6:5 mode	Bits 10:5 of 16-bit pixel			Bits 10:9 of 16-bit pixel
16-bpp, a:5:5:5 mode	Bits 9:5 of 16-bit pixel		Bits 9:7 of 16-bit pixel	
8-bpp, 3:3:2 mode	Bits 4:2 of 8-bit pixel	Bits 4:2 of 8-bit pixel		Bits 4:3 of 8-bit pixel
8-bpp mapped	Must be disabled			

In 24-bit-per-pixel modes, the 8-bit green component compare value is written to this field. In a:5:5:5 (or 5:6:5) 16-bit-per-pixel modes, the 5-bit (or 6) green component compare value should be placed in the upper five (or 6) bits and then duplicated in the lower three (or 2) bits. In 8-bpp mode, the middle three bits or the 3:3:2 pixel (the green component) are duplicated through the 8-bit component of this register. This imitates the color unpacking logic.
Writes to this field are controlled by the CONTROL_MASK_3D bit (bit 0).

9.2.3 COLOR_MIN_BOUNDS_3D Register *(cont.)*

Bit	Description
7:0	**Color_Compare_Min (Blue Component):** Since color compares operate at a full 8-bits per component, some bits from 5- and 2-bit blue components must be replicated in this field. The following table gives the method for this replication.

Table 9-6. Blue Component Color Compare Mapping

Pixel_Mode	Color Compare Value (Blue Component)				
	7:6	5:4	3	2	1:0
24-bpp, a:8:8:8 mode	Bits 7:0 of 32-bit pixel				
16-bpp, 5:5:5 and 5:6:5 modes	Bits 4:0 of 16-bit pixel			Bits 4:2 of 16-bit pixel	
8-bpp, 3:3:2 mode	Bits 1:0 of 8-bit pixel	Bits 1:0 of 8-bit pixel	Bits 1:0 of 8 bit pixel		Bits 1:0 of 8-bit pixel
8-bpp mapped	Must be disabled				

In 24-bit-per-pixel modes, the 8-bit blue component compare value is written to this field. In a:5:5:5 and 5:6:5 16-bit-per-pixel modes, the 5-bit blue component compare value should be placed in the upper five bits of this field, and the then duplicated in the lower three bits. In 8-bpp mode, the lower two bits of the 3:3:2 pixel (the blue component) are duplicated through the 8-bit component of this register. This imitates the color unpacking logic.
Writes to this field are controlled by CONTROL_MASK_3D bit (bit 0).

9.2.4 COLOR_MAX_BOUNDS_3D Register

Size (bits):	32
MMI/O Offset	410Ch
Access Type	Read/Write

Bit	Description	Mask	Reset Value
31:24	Color_Saturate_Max	CONTROL_MASK_3D [24]	0
23:16	Color_Compare_Max (Red)	CONTROL_MASK_3D [0]	0
15:8	Color_Compare_Max (Green)	CONTROL_MASK_3D [0]	0
7:0	Color_Compare_Max (Blue)	CONTROL_MASK_3D [0]	0

This register specifies the maximum bounds for the color saturate and color compare functions.

Bit	Description
31:24	**Color_Saturate_Max (8-bpp modes only):** This 8-bit field sets the maximum bound value used in color saturate for 8-bpp modes only. See the Color_Saturate_En bit in the CONTROL0_3D register on page 9-47. Writes to this field are controlled by the CONTROL_MASK_3D bit (bit 24).
23:16	**Color_Compare_Max (Red Component):** See the Color_Compare_Min (Red field) of COLOR_MIN_BOUNDS_3D register on page 9-52 for details of usage. Writes to this field are controlled by the CONTROL_MASK_3D bit (bit 0).
15:8	**Color_Compare_Max (Green Component):** See the Color_Compare_Min (Green field) of COLOR_MIN_BOUNDS_3D register on page 9-52 for details of usage. Writes to this field are controlled by the CONTROL_MASK_3D bit (bit 0).
7:0	**Color_Compare_Max (Blue Component):** See the Color_Compare_Min (Blue field) of COLOR_MIN_BOUNDS_3D register on page 9-52 for details of usage. Writes to this field are controlled by the CONTROL_MASK_3D bit (bit 0).

9.2.5 CONTROL1_3D Register

Size (bits):	32
MMI/O Offset	4110h
Access Type	Read/Write

Bit	Description	Mask	Reset Value
31:24	Z_Hit_ Object_Mask	CONTROL_MASK_3D [24]	0
23:8	Reserved		0
7:0	Z_Hit_Precision_Mask	CONTROL_MASK_3D [0]	0

This register specifies the collision-detection function of the 3D engine.

Bit	Description
31:24	**Z_Hit_Object_Mask:** These bits are used only when the Z_ON and Z_COLLISION modes are selected. On a bit level, this field masks the upper eight bits of the Z-compare operation, and is used to reserve upper bits of the Z-buffer contents to hold 'object' indices. If two bits are masked, up to four objects can be represented by the upper two bits of the Z value. If three bits are masked, up to eight objects can be represented and so on. Each bit in this field has the following meaning: If this bit is set to '1', it masks the bit from Z-collision compare. If the bit is set to '0', it uses the bit for Z-collision compare (normal compare). Writes to this field are controlled by CONTROL_MASK_3D bit (bit 24).
23:8	**Reserved:** Program these bits to '0'.
7:0	**Z_Hit_Precision_Mask:** These bits are used only when the Z_ON and Z_COLLISION modes are selected. On a bit level, this field masks the lower eight bits of the Z-compare operation for collision detection. Masking of these lower eight bits can be used to select the precision of the Z-collision compare operation. Thus, Z-collision events can occur at a coarser granularity than the Z-buffer bit width. If this bit is set to '1', it masks the bit from Z-collision compare. If this bit is set to '0', it uses the bit for Z-collision compare (normal compare). Writes to this field are controlled by CONTROL_MASK_3D bit (bit 0).

9.2.6 BASE0_ADDR_3D Register

Size (bits):	32
MMI/O Offset	4114h
Access Type	Read/Write

Bit	Description	Mask	Reset Value
31:28	Reserved		
27:24	Pattern_X_Offset	CONTROL_MASK_3D [24]	0
23:20	Reserved		0
19:16	Pattern_Y_Offset	CONTROL_MASK_3D [16]	0
15	Texture_Location	CONTROL_MASK_3D [15]	0
14	Z_Buffer_Location	CONTROL_MASK_3D [14]	0
13	Color_Buffer_Location	CONTROL_MASK_3D [13]	0
12:6	Color_Buffer_X_Offset [12:6]	CONTROL_MASK_3D [0]	0
5:0	Reserved		0

This register specifies the Pattern_RAM offsets and X address offsets to base addresses and texture, and to the Z and color location controls.

Bit	Description
31:28	**Reserved:** Program these bits to ‘0h’.
27:24	**Pattern_X_Offset:** These bits control the pattern lookup offset for X address. This offset is used with the interpolated X value from the 3D Engine, X_{interp} to determine the X location, X_{pat} in the Pattern RAM. X_{pat} values wrap within the pattern. That is, $X_{pat} = (X_{interp} + Pattern\_X\_Offset) \text{ MOD } Pat\_Size$ where Pat_Size is 16 for XY color or XY stipple patterning or 8 for XY dither patterning. Writes to this field are controlled by the CONTROL_MASK_3D bit 16.
23:20	**Reserved:** Program these bits to ‘0h’.
19:16	**Pattern_Y_Offset:** These bits control the pattern lookup offset for Y address. This offset is used with the interpolated Y value from the 3D engine, Y_{interp} to determine the Y location, Y_{pat} in the Pattern RAM. The Y_{pat} values wrap within the pattern. That is, $Y_{pat} = (Y_{interp} + Pattern\_Y\_Offset) \text{ MOD } Pat\_Size$ where Pat_Size is 16 for XY color or XY stipple patterning or 8 for XY dither patterning. Writes to this field are controlled by the CONTROL_MASK_3D bit (bit 16).
15	**Texture_Location:** This bit controls the location of texture maps for subsequent drawing operations. Texels within a map are always accessed in an XY format. When this bit is set to ‘1’, it fetches from host memory (tiled format). When this bit is set to ‘0’, it is fetched from RDRAM memory (UV format). Writes to this field are controlled by the CONTROL_MASK_3D bit (bit 15).

9.2.6 BASE0_ADDR_3D Register *(cont.)*

Bit	Description
14	**Z_Buffer_Location:** This bit controls the location of the depth buffer for subsequent drawing operations. Depth data are always accessed in an XY format. When this bit is set to '1', it is stored in host processor memory. When this bit is set to '0', it is stored in RDRAM memory. Writes to this field are controlled by the CONTROL_MASK_3D bit (bit 14).
13	**Color_Buffer_Location:** This bit controls the location of the color buffer for subsequent drawing operations. Pixels are always accessed in an XY format. When this bit is set to '1', it is stored in host processor memory. When this bit is set to '0', it is stored in RDRAM memory. Writes to this field are controlled by the CONTROL_MASK_3D bit (bit 13).
12:6	**Color_Buffer_X_Offset [12:6]:** This bit controls the offset to color buffer X address. The offset is in 64-byte blocks. Writes to this field are controlled by the CONTROL_MASK_3D bit (bit 0).
5:0	**Reserved:** These bits should always be set to '0h'.

Computing X Address of Color Buffer

Source/Result	12:11	10:6	5:0
Source 1: X address of pixel (Interpolated by the 3D engine)		X address (bits 10:0)	
Source 2: color space X base address	Color_Buffer_X_Offset (BASE0_ADDR_3D bits 12:6)		000000
Resulting X address of color buffer	Sum of these two sources		

9.2.7 BASE1_ADDR_3D Register

Size (bits):	32
MMI/O Offset	4118h
Access Type	Read/Write

Bit	Description	Mask	Reset Value
31:29	Reserved		0
28:21	Z_Buffer_Y_Offset [12:5]	CONTROL_MASK_3D [16]	0
20:16	Reserved		0
15:13	Reserved		0
12:5	Color_Buffer_Y_Offset [12:5]	CONTROL_MASK_3D [0]	0
4:0	Reserved		0

This register specifies the offset addresses for the RDRAM Z buffer and color buffer Y address translation.

Bit **Description**

31:29 **Reserved:** Program these bits to ‘0h’.

28:21 **Z_Buffer_Y_Offset [12:5]:** These bits control the Y offset of the Z buffer from the color space Y base address. The offset is in 32-line blocks. Writes to this field are controlled by the CONTROL_MASK_3D bit (bit 16).

Source/Result	12:11	10:5	4:0
Source 1: Y address of pixel (interpolated by the 3D engine)	00	Y address (bits 10:0)	
Source 2: Z buffer Y base address	Z_Buffer_Y_Offset (BASE1_ADDR_3D bits 28:21)		00000
Resulting Y address of Z buffer	Sum of these two sources		

20:16 **Reserved:** Program these bits to ‘0h’.

15:13 **Reserved:** Program these bits to ‘0h’.

12:5 **Color_Buffer_Y_Offset [12:5]:** These bits control the Y offset of the color buffer from the color space Y base address. The offset is in 32-line blocks. Writes to this field are controlled by the CONTROL_MASK_3D bit (bit 0).

Source/Result	12:11	10:5	4:0
Source 1: Y address of pixel (interpolated by the 3D engine)	00	Y address (bits 10:0)	
Source 2: color buffer Y offset (this field)	Color_Buffer_Y_Offset (BASE1_ADDR_3D bits 12:5)		00000
Resulting Y address of color buffer	Sum of these two sources		

4:0 **Reserved:** Program these bits to ‘0h’.

9.2.8 TX_CTL0_3D Register

Size (bits):	32
MMI/O Offset	4120h
Access Type	Read/Write

Bit	Description	Mask	Reset Value
31:28	Texture Lookup Offset	CONTROL_MASK_3D [28]	0
27:26	Reserved		0
25:24	Texel UV Address Multiplexer Select	CONTROL_MASK_3D [24]	0
23	Reserved		0
22	Tex_Mask_Function	CONTROL_MASK_3D [22]	0
21	Tex_Mask_Enable	CONTROL_MASK_3D [21]	0
20	Tex_Mask_Polarity	CONTROL_MASK_3D [20]	0
19	Reserved	CONTROL_MASK_3D [19]	0
18	Fil_Tex_En	CONTROL_MASK_3D [18]	0
17	Tex_as_Src	CONTROL_MASK_3D [17]	0
16	Texel_Lookup_En	CONTROL_MASK_3D [16]	0
15:11	Reserved		0
10:8	Texel_Mode	CONTROL_MASK_3D [8]	0
7	Tex_V_Ovf_Sat_En	CONTROL_MASK_3D [7]	0
6:4	Tex_V_Address_Mask	CONTROL_MASK_3D [4]	0
3	Tex_U_Ovf_Sat_En	CONTROL_MASK_3D [3]	0
2:0	Tex_U_Address_Mask	CONTROL_MASK_3D [0]	0

This register controls the texture mapping functions of the CL-GD5464. A write to this register invalidates all entries in the texture cache.

Bit	Description
31:28	**Texture Lookup Offset:** An offset for lookup of texel color value in the TLUT (texture lookup table). Enabled by bit 16 of this register and used only in 4-bpp Mapped or 8-bpp Mapped Texel modes. Addresses in the TLUT are formed as following: 4-bpp Mapped Texel mode: TLUT address = texel (4:0) + ((Texture_Lookup_Offset (3:0) << 4) + 0x0000) 8-bpp Mapped Texel mode: TLUT address = texel (8:0) + ((Texture_Lookup_Offset (3:0) << 4) + 0x0000)
27:26	**Reserved:** Program these bits to ‘0h’.

9.2.8 TX_CTL0_3D Register *(cont.)*

Bit	Description
25:24	**Texel UV Address Multiplexer Select:** These bits map the upper V address bits into U space. This allows better packing of texture maps into unused fragments of RDRAM. Writes to this field are controlled by CONTROL_MASK_3D bit (bit 24).

Table 9-7. UV Address Multiplex Select

Register Bits		Address Bits		
25	**24**	**U6**	**U5**	**U4–U0**
0	0	U6	U5	U4–U0
0	1	U5	V7	U4–U0
1	0	V7	U5	U4–U0
1	1	V8	V7	U4–U0

23	**Reserved:** Set this bit to ‘0’.
22	**Tex_Mask_Function:** This bit, in concert with other Texture Control register bits, Instruction Modifier bits, and possibly the mask bit within the texel, selects either interpolated color from the RGB interpolators, host generated texels (provided as filtered texels from host memory), or regular texels (from a texture map) as the SOURCE_RGB (input) term to the lighting stage. See the table and description of Tex_Mask_En bit (bit 21). The Tex_Mask_Function bit only has an effect for Texel_Modes that have a mask bit in a texel. That is, in Texel_Modes of 4-bpp mapped, 8-bpp mapped, a:5:5:5, or a:8:8:8. If this bit is set to ‘1’, the texture masking source is selected. If this bit is set to ‘0’, the write mask is selected. Writes to this field are controlled by CONTROL_MASK_3D bit (bit 22).

9.2.8 TX_CTL0_3D Register *(cont.)*

Bit **Description**

21 **Tex_Mask_Enable:** This bit enables operations that use the mask bit in the texel. Only applicable for Texel_Modes that have a mask bit in the texel. That is, in Texel_Modes of 4-bpp mapped, 8-bpp mapped, a:5:5:5, or a:8:8:8. A '1' enables and '0' disables this bit.
Writes to this field are controlled by CONTROL_MASK_3D bit (bit 21).

Tex On	Tex Mask En	Tex Mask Fn	Tex as Src	Tex Mask Po	Texel Mask bit	SOURCE_RGB
0	0	X	0	X	X	Interpolated color (patterned, stippled, or dithered as selected by Instruction Modifier bits). This is the normal color configuration.
0	0	X	1	X	X	Host generated texels with masking disabled
0	1	X	1	X	X	Host generated texels with masking enabled
1	0	X	0	X	X	Regular texels from a texture map. This is the normal texture map configuration.
1	0	X	1	X	X	Interpolated color. This configuration is not normally used during texture mapping.
1	1	0	0	X	X	Regular texels. This configuration uses the Texel Mask bit to control update of the color buffer.
1	1	0	1	X	X	Interpolated color. This configuration uses the Texel Mask bit to control update of the color buffer.
1	1	1	X	0	0	Regular texels
1	1	1	X	0	1	Interpolated color
1	1	1	X	1	0	Interpolated color
1	1	1	X	1	1	Regular texels

For the above table, the column definitions are:
Tex On: Texture_Eng_On Instruction Modifier bit 17.
Tex Mask En: Tex_Mask_En bit (bit 21) of TX_CTL0_3D register.
Tex Mask Fn: Tex_Mask_Function bit (bit 22) of TX_CTL0_3D register.
Tex as Src: Tex_as_Src bit (bit 17) of TX_CTL0_3D register.
Tex Mask Pol: Tex_Mask_Polarity bit (bit 20) of TX_CTL0_3D register.
Texel Mask Bit: The mask bit within the texel, that is, Texture Lookup bit (bit 0) in 4-bpp mapped; CLUT bit (bit 0) in 8-bpp mapped; bit 15 in a:5:5:5 Texel_Mode; or bit 31 in a:8:8:8 Texel_Mode.
The 'X' in the body of the table indicates a don't care setting of the bit.

9.2.8 TX_CTL0_3D Register *(cont.)*

Bit **Description**

20 **Tex_Mask_Polarity:** This bit only has an effect when enabled by the Texel_Mask_En bit (bit 21) of this register. This bit allows programmers to inhibit texel writes within a textured polygon when in Texel_Mode, which includes a mask bit. If Tex_Mask_Polarity does not equal the mask bit in the texture data, the texel can not be written to the frame buffer (that is, masked). If Tex_Mask_Polarity equals the mask bit in the texture data, the frame buffer can be updated. For texture map filtering enabled by the Fil_Tex_En bit (bit 18 of this register), see the following table.

If this bit is '1', texels with a value of '0' in their mask bit cannot be written to the frame buffer (masked). Texels with a value of '1' can be written to the frame buffer.

If this bit is '0', the texels with a value of '1' in their mask bit cannot be written to the frame buffer (masked). Texels with a value of '0' can be written to the frame buffer.

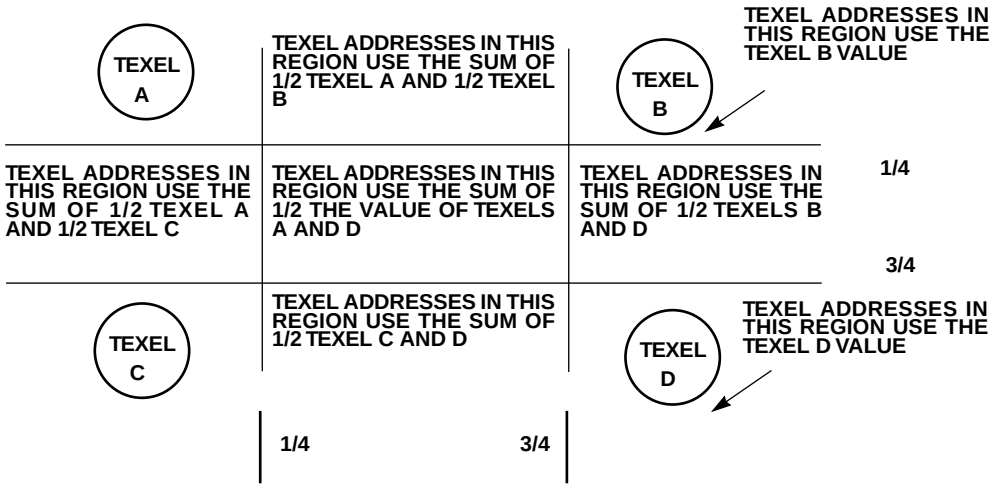
Tex_Mask_ Polarity	Texel1's Mask Bit	Texel2's Mask Bit	Texture Mask Function for Filtered Texture Maps
0	0	0	Write to frame buffer
0	0	1	Write to frame buffer
0	1	0	Write to frame buffer
0	1	1	Mask (does not write to frame buffer)
1	0	0	Mask (does not write to frame buffer)
1	0	1	Write to frame buffer
1	1	0	Write to frame buffer
1	1	1	Write to frame buffer

Writes to this field are controlled by CONTROL_MASK_3D bit (bit 24).

19 **Reserved:** Set this bit to '0'.

9.2.8 TX_CTL0_3D Register *(cont.)*

Bit	Description
18	**Fil_Tex_En:** This bit controls whether texture filtering is performed in full-color texel modes. For example, for the texels A, B, C, and D at (0,0), (0,1), (1,0), and (1,1) sub-texel addresses in the range $0.25 \le U < 0.75$ and sub-texels addresses in the range $0.25 \le U < 0.75$ and sub-texels in the range $0.25 \le V < 0.75$ are treated as a merge of the surrounding texels according to the drawing below. Write to this field is controlled by CONTROL_MASK_3D bit (bit 18).



	'1' enables texture filtering, and '0' disables it.
17	**Tex_as_Src:** This bit specifies the source data for lighting. This bit in concert with other texture control register bits, Instruction Modifier bits, and possibly the mask bit within the texel, selects either iterpolated color, host generated texels, or regular texels (from a texture map) as the SOURCE_RGB (input) term to the lighting stage. See the description of bit 21, Tex_Mask_En bit. Writes to this field are controlled by CONTROL_MASK_3D bit (bit 17). When this bit is '1', the polygon engine is the lighting source. When this bit is '0', the texture data is the lighting source.
16	**Texel_Lookup_En:** This bit enables the use of texel data as lookup address into the TLUT (either 4- or 8-bpp modes). Write to this field is controlled by CONTROL_MASK_3D bit (bit 16). When this bit is '1', the lookup is enabled. When this bit is '0', the lookup is disabled.
15:11	**Reserved:** Program these bits to '0h'.

9.2.8 TX_CTL0_3D Register *(cont.)*

Bit **Description**

10:8 **Texel_Mode:** This three-bit field stores the texel size. Writes to this field are controlled by CONTROL_MASK_3D bit (bit 8).

Bits 10:8	Texel Data	
	Size (bits)	Format
0 0 0	4	Mapped (by TLUT); bit 0 from TLUT can be used as a mask
0 0 1	n/a	Reserved
0 1 0	8	Mapped (by TLUT); bit 0 from TLUT can be used as a mask
0 1 1	8	3:3:2
1 0 0	16	5:6:5
1 0 1	16	a:5:5:5; bit 15 can be used as a mask
1 1 0	32	a:8:8:8; bit 31 can be used as a mask
1 1 1	n/a	Reserved

7 **Tex_V_Ovf_Sat_En:** This bit controls whether the V component of the texture coordinate is allowed to wrapped at its extents (0 to MAX value), or is clipped at either 0 or the MAX value.

When this bit is '1', saturate V to 0 or MAX is enabled. When this bit is '0', the wrap is disabled.

Writes to this field are controlled by CONTROL_MASK_3D bit (bit 7).

6:4 **Texel_V_Address_Mask:** This field defines the height of V space. Writes to this field are controlled by CONTROL_MASK_3D bit (bit 4).

110–111 Reserved
101 512
100 256
011 128
010 64
001 32
000 16

9.2.8 TX_CTL0_3D Register *(cont.)*

Bit	Description
3	**Tex_U_Ovf_Sat_En:** This bit controls whether the U component of the texture coordinate is allowed to wrapped at it's extents (0-to-MAX value), or is clipped at either 0 or the max value. When this bit is '1', saturate U-to-0 or MAX is enabled. When this bit is '0', the wrap is disabled. Writes to this field are controlled by CONTROL_MASK_3D bit (bit 3).
2:0	**Texel_U_Address_Mask:** This field defines the width of the U space. Writes to this field are controlled by CONTROL_MASK_3D bit (bit 0). 110–111 Reserved 101 512 100 256 011 128 010 64 001 32 000 16

9.2.9 TX_XYBASE_3D Register

Size (bits):	32
MMI/O Offset	4124h
Access Type	Read/Write

Bit	Description	Mask	Reset Value
31:29	Reserved		0
28:20	Tex_Y_Base_Addr [12:4]	CONTROL_MASK_3D [16]	0
19:13	Reserved		0
12:5	Tex_X_Base_Addr [12:5]	CONTROL_MASK_3D [0]	0
4:0	Reserved		0

This register specifies texture XY base address. A write to this register invalidates all entries in the texture cache.

Bit **Description**

31:29 **Reserved:** Program these bits to ‘0h’.

28:20 **Tex_Y_Base_Addr [12:4]:** This field defines Y scanline offset address in 16 blocks within RDRAM (frame buffer) memory. Writes to this field are controlled by CONTROL_MASK_3D bit (bit 16).

Source/Result	12:9	8:4	3:0
Source 1: V address of texel	0000	V address (bits 8:0)	
Source 2: Y base address	Texture Y base address (bits 28:20)		0000
Resulting X address of texel at V	Sum of these two sources		

19:13 **Reserved:** Program these bits to ‘0h’.

12:5 **Tex_X_Base_Addr [12:5]:** This field defines X byte offset address within RDRAM (frame buffer) memory. (Textures are aligned on 32-byte boundaries.) Writes to this field are controlled by CONTROL_MASK_3D bit (bit 0).

Source/Result	12:8	7:5	4:0
Source 1: U address of texel	0000	U address (bits 7:0)	
Source 2: X base address	Texture X base address (bits 12:5)		00000
Resulting X address of texel at U	Sum of the above two sources		

4:0 **Reserved:** Program these bits to ‘0h’.

9.2.10 TX_CTL1_3D Register

Size (bits):	32
MMI/O Offset	4128h
Access Type	Read/Write

Bit	Description	Mask	Reset Value
31:28	Reserved		0
27	Tex_Color_Compare_Mode	CONTROL_MASK_3D [27]	0
26	Tex_Blue_Color_Compare	CONTROL_MASK_3D [26]	0
25	Tex_Green_Color_Compare	CONTROL_MASK_3D [25]	0
24	Tex_Red_Color_Compare	CONTROL_MASK_3D [24]	0
23:16	Tex_Min (Red)	CONTROL_MASK_3D [0]	0
15:8	Tex_Min (Green)	CONTROL_MASK_3D [0]	0
7:0	Tex_Min (Blue)	CONTROL_MASK_3D [0]	0

This register specifies Texture Control 1. A write to this register invalidates all entries in the texture cache.

Bit	Description
31:28	**Reserved:** Program these bits to ‘0h’.
27	**Tex_Color_Compare_Mode:** This bit determines if the texture compare color compare is exclusive or inclusive (for transparent texture effects). Writes to this field are controlled by CONTROL_MASK_3D bit (bit 24). If this bit is ‘1’, the color compare is inclusive. If this bit is ‘0’, the color compare is exclusive.
26	**Tex_Blue_Color_Compare:** This bit is the mask used prior to texture compare (for transparent texture effects). Writes to this field are controlled by CONTROL_MASK_3D bit (bit 27). This bit is enabled by ‘1’, and disabled by ‘0’.
25	**Tex_Green_Color_Compare:** This bit is the mask used prior to texture compare (for transparent texture effects). Writes to this field are controlled by CONTROL_MASK_3D bit (bit 26). This bit is enabled by ‘1’, and disabled by ‘0’.
24	**Tex_Red_Color_Compare:** This bit is the mask used prior to texture compare (for transparent texture effects). Writes to this field are controlled by CONTROL_MASK_3D bit (bit 25). This bit is enabled by ‘1’, and disabled by ‘0’.
23:16	**Tex_Min (Red Component):** This field stores the texel mask minimum bounds. Writes to this field are controlled by CONTROL_MASK_3D bit (bit 0).
15:8	**Tex_Min (Green Component):** This field stores the texel mask minimum bounds. Writes to this field are controlled by CONTROL_MASK_3D bit (bit 0).
7:0	**Tex_Min (Blue Component):** This field stores the texel mask minimum bounds. Writes to this field are controlled by CONTROL_MASK_3D bit (bit 0).

9.2.11 TX_CTL2_3D Register

Size (bits):	32
MMI/O Offset	412Ch
Access Type	Read/Write

Bit	Description	Mask	Reset Value
31:24	Reserved		0
23:16	Tex_Max (Red)	CONTROL_MASK_3D [0]	0
15:8	Tex_Max (Green)	CONTROL_MASK_3D [0]	0
7:0	Tex_Max (Blue)	CONTROL_MASK_3D [0]	0

This register specifies Texture Control 2. A write to this register invalidates all entries in the texture cache.

Bit	Description
31:24	**Reserved:** Program these bits to ‘0h’.
23:16	**Tex_Max (Red Component):** This field stores the texel mask maximum bounds. Writes to this field are controlled by CONTROL_MASK_3D bit (bit 0).
15:8	**Tex_Max (Green Component):** This field stores the texel mask maximum bounds. Writes to this field are controlled by CONTROL_MASK_3D bit (bit 0).
7:0	**Tex_Max (Blue Component):** This field stores the texel mask maximum bounds. Writes to this field are controlled by CONTROL_MASK_3D bit (bit 0).

9.2.12 COLOR_REG0_3D Register

Size (bits):	32
MMI/O Offset	4130h
Access Type	Read/Write

Bit	Description	Mask	Reset Value
31:24	Reserved		0
23:16	Color0 (Red)	CONTROL_MASK_3D [0]	0
15:8	Color0 (Green)	CONTROL_MASK_3D [0]	0
8:0	Color0 (Blue)	CONTROL_MASK_3D [0]	0

This register specifies a constant value for color patterning or alpha blending.

Bit	Description
31:24	**Reserved:** Program these bits to ‘0h’.
23:0	**Color0:** This 24-bit field stores the constant value used in patterned polygons or Non-Indexed mode fixed-alpha blending. For patterned polygons, the Pattern_RAM registers select either this field or the Color1 field of the COLOR_REG1_3D register (on page 9-71) as the pair of colors used to fill the polygon. For Non-Indexed mode alpha blending, this field is multiplied by the DEST_ALPHA value when selected as the DEST_RGB value by Alpha_Dest_Color_Select field (bits 14:13) of CONTROL0_3D register. Note that all eight bits of each component are used in the multiplication regardless of the pixel mode. Writes to this field are controlled by CONTROL_MASK_3D bit (bit 0). 23:16 Red component 15:8 Green component 7:0 Blue component

9.2.13 COLOR_REG1_3D Register

Size (bits):	32
MMI/O Offset	4134h
Access Type	Read/Write

Bit	Description	Mask	Reset Value
31:24	Reserved		0
23:16	Color1 (Red)	CONTROL_MASK_3D [0]	0
15:8	Color1 (Green)	CONTROL_MASK_3D [0]	0
7:0	Color1 (Blue)	CONTROL_MASK_3D [0]	0

This register specifies a constant value for color patterning or fixed lighting.

Bit	Description
31:24	**Reserved:** Program these bits to ‘0h’.
23:0	**Color1:** Constant value used in patterned polygons or Non-Indexed mode fixed lighting. For patterned polygons, the Pattern_RAM registers select either this field or the Color0 field of the COLOR_REG0_3D register (on page 9-70) as a pair of colors used to fill the polygon. For Non-Indexed mode lighting, this field is multiplied by the SOURCE_RGB value when selected as the LIGHT_RGB value by the Light_Src_Sel field (bits 26:25) of the CONTROL0_3D register. Note that all eight bits of each component are used in the multiplication regardless of the pixel mode. Writes to this field are controlled by CONTROL_MASK_3D bit (bit 0). 23:16 Red component 15:8 Green component 7:0 Blue component

9.2.14 Z_COLLIDE_3D Register

Size (bits):	32
MMI/O Offset	4138h
Access Type	Read/Write

Bit	Description	Mask	Reset Value
31:16	Reserved		0
15:0	Z_Collision	CONTROL_MASK_3D [0]	0

This register is normally read only and determines the Z value at a Z hit or collision. This register should only be written during manufacturing tests.

Bit	Description
31:16	**Reserved:** These bits always read as ‘0’s.
15:0	**Z_Collision:** This field stores the Z value read from the Z buffer when a Z collision occurs. The values range from 0 to 65535.

9.2.15 STATUS0_3D Register

Size (bits):	32
MMI/O Offset	413Ch
Access Type	Read only

Bit	Description	Reset Value
31:2	Reserved	0
1	3D-Engine Busy	0
0	Z_COLLISION Event Status	0

This register specifies the 3D engine status.

Bit	Description
31:2	**Reserved:** These bits always read as ‘0’s.
1	**3D-Engine Busy:** This bit reflects the status of the 3D engine. If this bit is ‘1’, the 3D engine is busy. If this bit is ‘0’, the 3D engine is not busy.
0	**Z_COLLISION Event Status:** This bit generates an interrupt if the Z_COLLISION interrupt is enabled. If this bit is ‘1’, a Z collision event occured since the last read of this register. This bit is only set if the Z_COLLISION bit is enabled. If this bit is ‘0’, no Z collision event has occured since the last read. A read clears this bit.

9.2.16 X_CLIP_3D Register

Size (bits):	32
MMI/O Offset	4160h
Access Type	Read/Write

Bit	Description	Mask	Reset Value
31	XMax_Clip_Enable	CONTROL_MASK_3D [31]	0
30:27	Reserved		0
26:16	XMax_Clip	CONTROL_MASK_3D [16]	0
15	XMin_Clip_Enable	CONTROL_MASK_3D [15]	0
14:11	Reserved		0
10:0	XMin_Clip	CONTROL_MASK_3D [0]	0

This register controls the X coordinates of the clipping rectangle for drawing. A pixel P at (P_x,P_y) is drawn under the following conditions:

- When both YMin_Clip_Enable and YMax_Clip_Enable are set to '0' (disabled), or
- When YMin_Clip ≤ P_Y and YMin_Clip_Enable is set to '1', and YMax_Clip_Enable is set to '0', or
- When P_Y ≤YMax_Clip and YMax_Clip_Enable is set to '1' and YMin_Clip_Enable is set to '0', or
- When YMin_Clip ≤ P_Y ≤ YMax_Clip and both YMax_Clip_Enable and YMin_Clip_Enable are set to '1' (enabled).

The case XMax_Clip < XMin_Clip should not be programmed when both limits are enabled.

Bit	Description
31	**XMax_Clip_Enable:** If this bit is set to '1', it enables clipping operation to the XMax_Clip value. If this bit is set to '0', it disables clipping to the XMax_Clip value. Writes to this bit are controlled by CONTROL_MASK_3D bit (bit 31).
30:27	**Reserved:** Program these bits to '0h'.
26:16	**XMax_Clip:** This field stores the maximum X coordinate of the clipping rectangle in the range of 0 to 2047. Writes to this field are controlled by CONTROL_MASK_3D bit (bit 16).
15	**XMin_Clip_Enable:** If this bit is set to '1', it enables clipping operation to the XMin_Clip value. If this bit is set to '0', it disables clipping to the XMin_Clip value. Writes to this bit are controlled by CONTROL_MASK_3D bit (bit 15).
14:11	**Reserved:** Program these bits to '0h'.
10:0	**XMin_Clip:** This field stores the minimum X coordinate of the clipping rectangle in the range of 0 to 2047. Writes to this field are controlled by CONTROL_MASK_3D bit (bit 0).

9.2.17 Y_CLIP_3D Register

Size (bits):	32
MMI/O Offset	4164h
Access Type	Read/Write

Bit	Description	Mask	Reset Value
31	YMax_Clip_Enable	CONTROL_MASK_3D [31]	0
30:27	Reserved		0
26:16	YMax_Clip	CONTROL_MASK_3D [16]	0
15	YMin_Clip_Enable	CONTROL_MASK_3D [15]	0
14:11	Reserved		0
10:0	YMin_Clip	CONTROL_MASK_3D [0]	0

This register controls the Y coordinates of the clipping rectangle for drawing. A pixel P at (P_x,P_y) is drawn under the following conditions:

- When both YMin_Clip_Enable and YMax_Clip_Enable are set to '0' (disabled), or
- When YMin_Clip ≤ P_Y and YMin_Clip_Enable is set to '1' and YMax_Clip_Enable is set to '0', or
- When P_Y ≤ YMax_Clip and YMax_Clip_Enable is set to '1' and YMin_Clip_Enable is set to '0', or
- When YMin_Clip ≤ P_Y ≤ YMax_Clip and both YMax_Clip_Enable and YMin_Clip_Enable are set to '1' (enabled).

The case YMax_Clip < YMin_Clip should not be programmed when both limits are enabled.

Bit	Description
31	**YMax_Clip_Enable:** If this bit is set to '1', it enables the clipping operation to the YMax_Clip value. If this bit is set to '0', it disables clipping to the YMax_Clip value. Writes to this bit are controlled by CONTROL_MASK_3D bit (bit 31).
30:27	**Reserved:** Program these bits to '0h'.
26:16	**YMax_Clip:** This field stores the maximum Y coordinate of the clipping rectangle in the range of 0 to 2047. Writes to this field are controlled by CONTROL_MASK_3D bit (bit 16).
15	**YMin_Clip_Enable:** If this bit is set to '1', it enables the clipping operation to the YMin_Clip value. If this bit is set to '0', it disables clipping to the YMin_Clip value. Writes to this bit are controlled by CONTROL_MASK_3D bit (bit 15).
14:11	**Reserved:** Program these bits to '0h'.
10:0	**YMin_Clip:** This field stores the minimum Y coordinate of the clipping rectangle in the range of 0 to 2047. Writes to this field are controlled by CONTROL_MASK_3D bit (bit 0).

9.2.18 TEX_SRAM_CTL_3D Register

Size (bits):	32
MMI/O Offset	4168h
Access Type	Read/Write

Bit	Description	Mask	Reset Value
31:7	Reserved		0
6:4	2D_SRAM_Sel	CONTROL_MASK_3D [4]	0
3:0	Reserved		0

This register specifies a constant value for color patterning or alpha blending.

Bit	Description
31:7	**Reserved:** Program these bits to ‘0h’.
6:4	**2D_SRAM_Select:** This field selects a 128-byte region of the 1-Kbyte texture SRAM cache for use by the BitBLT engine for 2D operations.
3:0	**Reserved:** Program these bits to ‘0h’.

9.3 Pattern RAM Registers

The Pattern RAM registers have an XY color pattern, an XY stipple pattern, an XY dither pattern, or a line mask pattern organization summarized in Table 9-8 through Table 9-13, listed in MMI/O offset order. The detailed register description is also provided in MMI/O offset order.

Table 9-8. XY Color Pattern and XY Stipple Pattern Formats (One-Pattern RAM Register, Bit Per Pixel)

Register Name	Description	Format	MMI/O Offset	Page
PATTERN_RAM_0_3D	Rows 0 and 1 of a 16 × 16 color or stipple pattern	16.16	4140h	9-81
PATTERN_RAM_1_3D	Rows 2 and 3 of a 16 × 16 color or stipple pattern	16.16	4144h	9-83
PATTERN_RAM_2_3D	Rows 4 and 5 of a 16 × 16 color or stipple pattern	16.16	4148h	9-84
PATTERN_RAM_3_3D	Rows 6 and 7 of a 16 × 16 color or stipple pattern	16.16	414Ch	9-85
PATTERN_RAM_4_3D	Rows 8 and 9 of a 16 × 16 color or stipple pattern	16.16	4150h	9-86
PATTERN_RAM_5_3D	Rows 10 and 11 of a 16 × 16 color or stipple pattern	16.16	4154h	9-87
PATTERN_RAM_6_3D	Rows 12 and 13 of a 16 × 16 color or stipple pattern	16.16	4158h	9-88
PATTERN_RAM_7_3D	Rows 14 and 15 of a 16 × 16 color or stipple pattern	16.16	415Ch	9-89

Table 9-9. XY Dither Pattern Format (Four-Pattern RAM Register, Bits Per Pixel)

Register Name	Description	Format	MMI/O Offset	Page
PATTERN_RAM_0_3D	Row 0 (8 pixels) of an 8 × 8 dither pattern	4.4.4.4.4.4.4.4	4140h	9-81
PATTERN_RAM_1_3D	Row 1 (8 pixels) of an 8 × 8 dither pattern	4.4.4.4.4.4.4.4	4144h	9-83
PATTERN_RAM_2_3D	Row 2 (8 pixels) of an 8 × 8 dither pattern	4.4.4.4.4.4.4.4	4148h	9-84
PATTERN_RAM_3_3D	Row 3 (8 pixels) of an 8 × 8 dither pattern	4.4.4.4.4.4.4.4	414Ch	9-85
PATTERN_RAM_4_3D	Row 4 (8 pixels) of an 8 × 8 dither pattern	4.4.4.4.4.4.4.4	4150h	9-86
PATTERN_RAM_5_3D	Row 5 (8 pixels) of an 8 × 8 dither pattern	4.4.4.4.4.4.4.4	4154h	9-87
PATTERN_RAM_6_3D	Row 6 (8 pixels) of an 8 × 8 dither pattern	4.4.4.4.4.4.4.4	4158h	9-88
PATTERN_RAM_7_3D	Row 7 (8 pixels) of an 8 × 8 dither pattern	4.4.4.4.4.4.4.4	415Ch	9-89

Table 9-10. Line Mask Pattern Format (One-Pattern Register, Bit Per Pixel)

Register Name	Description	Format	MMI/O Offset	Page
PATTERN_RAM_0_3D	Register 0 (32 pixels) of line mask pattern	1.1.1 ... 1.1.1	4140h	9-81
PATTERN_RAM_1_3D	Register 1 (32 pixels) of line mask pattern	1.1.1 ... 1.1.1	4144h	9-83
PATTERN_RAM_2_3D	Register 2 (32 pixels) of line mask pattern	1.1.1 ... 1.1.1	4148h	9-84
PATTERN_RAM_3_3D	Register 3 (32 pixels) of line mask pattern	1.1.1 ... 1.1.1	414Ch	9-85
PATTERN_RAM_4_3D	Register 4 (32 pixels) of line mask pattern	1.1.1 ... 1.1.1	4150h	9-86
PATTERN_RAM_5_3D	Register 5 (32 pixels) of line mask pattern	1.1.1 ... 1.1.1	4154h	9-87
PATTERN_RAM_6_3D	Register 6 (32 pixels) of line mask pattern	1.1.1 ... 1.1.1	4158h	9-88
PATTERN_RAM_7_3D	Register 7 (32 pixels) of line mask pattern	1.1.1 ... 1.1.1	415Ch	9-89

Table 9-11 gives the relationship between the PATTERN_RAM register bits and the XY location on the destination bitmap for stipple patterns.

Table 9-11. Stipple Pattern XY Location

Y[3:0] Value (Lower Four Bits of Y)	0	X[3:0] Value (Lower Four Bits of X)	15
0	0	PATTERN_RAM_0_3D	15
1	16	PATTERN_RAM_0_3D	31
2	0	PATTERN_RAM_1_3D	15
3	16	PATTERN_RAM_1_3D	31
4	0	PATTERN_RAM_2_3D	15
5	16	PATTERN_RAM_2_3D	31
6	0	PATTERN_RAM_3_3D	15
7	16	PATTERN_RAM_3_3D	31
8	0	PATTERN_RAM_4_3D	15
9	16	PATTERN_RAM_4_3D	31
10	0	PATTERN_RAM_5_3D	15
11	16	PATTERN_RAM_5_3D	31
12	0	PATTERN_RAM_6_3D	15
13	16	PATTERN_RAM_6_3D	31
14	0	PATTERN_RAM_7_3D	15
15	16	PATTERN_RAM_7_3D	31

Table 9-12 indicates the relationship between the PATTERN_RAM register bits and the XY location on the destination bitmap for dither patterns.

Table 9-12. Dither Pattern XY Location

Y[2:0] Value (Lower Three Bits of Y)	X[2:0] Value (Lower Three bits of X)								PATTERN_RAM Register
0	3:0	7:4	11:8	15:12	19:16	23:20	27:24	31:28	PATTERN_RAM_0_3D
1	3:0	7:4	11:8	15:12	19:16	23:20	27:24	31:28	PATTERN_RAM_1_3D
2	3:0	7:4	11:8	15:12	19:16	23:20	27:24	31:28	PATTERN_RAM_2_3D
3	3:0	7:4	11:8	15:12	19:16	23:20	27:24	31:28	PATTERN_RAM_3_3D
4	3:0	7:4	11:8	15:12	19:16	23:20	27:24	31:28	PATTERN_RAM_4_3D
5	3:0	7:4	11:8	15:12	19:16	23:20	27:24	31:28	PATTERN_RAM_5_3D
6	3:0	7:4	11:8	15:12	19:16	23:20	27:24	31:28	PATTERN_RAM_6_3D
7	3:0	7:4	11:8	15:12	19:16	23:20	27:24	31:28	PATTERN_RAM_7_3D

Table 9-13 indicates the relationship between PATTERN_RAM register bits and pixel location within a line bitmap for line mask patterns when the PATTERN_RAM_0_3D register is selected by the Pattern_Y_Offset field of BASE0_ADDR_3D.

Table 9-13. PATTERN_RAM Register Bits and Pixel Location

Pixel Number Along the Line (in the direction of drawing)									PATTERN_RAM Register
0	**1st**	**2nd**	**...**	**31st**	**32nd**	**33rd**	**34th**	**...**	
0	1	2	...	31	0	1	2	...	PATTERN_RAM_0_3D

9.3.1 PATTERN_RAM_0_3D Register

Size (bits):	32
MMI/O Offset	4140h
Access Type	Read/Write

XY Color Patterning Selected by Instruction Modifier

Bit	Description	Reset Value
31:16	Row1_Color_Data	0
15:0	Row0_Color_Data	0

XY Stipple Patterning Selected by Instruction Modifier

Bit	Description	Reset Value
31:16	Row1_Stipple_Data	0
15:0	Row0_Stipple_Data	0

XY Dither Patterning Selected by Instruction Modifier

Bit	Description	Reset Value
31:28	Row0_Col7_Dither_Data	0
27:24	Row0_Col6_Dither_Data	0
23:20	Row0_Col5_Dither_Data	0
19:16	Row0_Col4_Dither_Data	0
15:12	Row0_Col3_Dither_Data	0
11:8	Row0_Col2_Dither_Data	0
7:4	Row0_Col1_Dither_Data	0
3:0	Row0_Col0_Dither_Data	0

Line Masking Selected by Instruction Modifier

Bit	Description	Reset Value
31:0	Line_Mask_Data	0

This register specifies either two rows of a 16 × 16 XY color pattern or XY stipple pattern, or a row of an 8 × 8 XY dither pattern or line mask pattern organization.

XY Color Patterning

Bit	Description
31:16	**Row1_Color_Data:** This 16-bit field stores the larger Y valued row of single-bit color data.
15:0	**Row0_Color_Data:** This 16-bit field stores the first (top) row of single-bit color data. Where, if single-bit color data is '1', use the color value in COLOR_REG1_3D register; if single-bit color data is '0', use the color value in COLOR_REG0_3D register, and where the least-significant bit of each 16-bit field is at the least-significant X position and the most-significant bit of each field is at X position (X = 15) of 16 × 16 pattern.

9.3.1 PATTERN_RAM_0_3D Register *(cont.)*

XY Stipple Patterning

Bit	Description
31:16	**Row1_Stipple_Data:** This 16-bit field stores one row (larger Y value of pair) of single-bit mask data.
15:0	**Row0_Stipple_Data:** This 16-bit field stores the first (top) row of single-bit mask data. Where, if this field is '1', mask (do not draw) the pixel; if this field is '0', draw the pixel, and where the least-significant bit of each 16-bit field is at the least-significant X position and most-significant bit is at X position (X = 15).

XY Dither Patterning

Bit	Description
31:28	**Row0_Col7_Dither_Data:** This field stores the four-bit dither data at the most significant X position (X_{pat} = 7) of 8 × 8 pattern.
27:24	**Row0_Col6_Dither_Data:** This field stores the dither data at X_{pat} = 6.
23:20	**Row0_Col5_Dither_Data:** This field stores the dither data at X_{pat} = 5.
19:16	**Row0_Col4_Dither_Data:** This field stores the dither data at X_{pat} = 4.
15:12	**Row0_Col3_Dither_Data:** This field stores the dither data at X_{pat} = 3.
11:8	**Row0_Col2_Dither_Data:** This field stores the dither data at X_{pat} = 2.
7:4	**Row0_Col1_Dither_Data:** This field stores the dither data at X_{pat} = 1.
3:0	**Row0_Col0_Dither_Data:** This field stores the dither data at least-significant X position (X_{pat} = 0).

Line Masking

Bit	Description
31:0	**Line_Mask_Data:** This is the 32-bit field of single-bit mask data, where bit 0 corresponds to the base point of the line and each subsquent pixel uses the next highest bit from this field for mask data. When bit 31 is reached, the next mask is taken from bit 0. Where, if this field is '1', mask (do not draw) the pixel; if this field is '0', draw the pixel.

9.3.2 PATTERN_RAM_1_3D Register

Size (bits):	32
MMI/O Offset	4144h
Access Type	Read/Write

XY Color Patterning Selected by Instruction Modifier

Bit	Description	Reset Value
31:16	Row3_Color_Data	0
15:0	Row2_Color_Data	0

XY Stipple Patterning Selected by Instruction Modifier

Bit	Description	Reset Value
31:16	Row3_Stipple_Data	0
15:0	Row2_Stipple_Data	0

XY Dither Patterning Selected by Instruction Modifier

Bit	Description	Reset Value
31:28	Row1_Col7_Dither_Data	0
27:24	Row1_Col6_Dither_Data	0
23:20	Row1_Col5_Dither_Data	0
19:16	Row1_Col4_Dither_Data	0
15:12	Row1_Col3_Dither_Data	0
11:8	Row1_Col2_Dither_Data	0
7:4	Row1_Col1_Dither_Data	0
3:0	Row1_Col0_Dither_Data	0

Line Masking Selected by Instruction Modifier

Bit	Description	Reset Value
31:0	Line_Mask_Data	0

This register specifies either two rows of a 16×16 XY color pattern or XY stipple pattern, one row of an 8×8 XY dither pattern, or line mask pattern organization.

9.3.3 PATTERN_RAM_2_3D Register

Size (bits):	32
MMI/O Offset	4148h
Access Type	Read/Write

XY Color Patterning Selected by Instruction Modifier

Bit	Description	Reset Value
31:16	Row5_Color_Data	0
15:0	Row4_Color_Data	0

XY Stipple Patterning Selected by Instruction Modifier

Bit	Description	Reset Value
31:16	Row5_Stipple_Data	0
15:0	Row4_Stipple_Data	0

XY Dither Patterning Selected by Instruction Modifier

Bit	Description	Reset Value
31:28	Row2_Col7_Dither_Data	0
27:24	Row2_Col6_Dither_Data	0
23:20	Row2_Col5_Dither_Data	0
19:16	Row2_Col4_Dither_Data	0
15:12	Row2_Col3_Dither_Data	0
11:8	Row2_Col2_Dither_Data	0
7:4	Row2_Col1_Dither_Data	0
3:0	Row2_Col0_Dither_Data	0

Line Masking Selected by Instruction Modifier

Bit	Description	Reset Value
31:0	Line_Mask_Data	0

This register specifies either two rows of a 16×16 XY color pattern or XY stipple pattern, one row of an 8×8 XY dither pattern, or line mask pattern organization.

9.3.4 PATTERN_RAM_3_3D Register

Size (bits):	32
MMI/O Offset	414Ch
Access Type	Read/Write

XY Color Patterning Selected by Instruction Modifier

Bit	Description	Reset Value
31:16	Row7_Color_Data	0
15:0	Row6_Color_Data	0

XY Stipple Patterning Selected by Instruction Modifier

Bit	Description	Reset Value
31:16	Row7_Stipple_Data	0
15:0	Row6_Stipple_Data	0

XY Dither Patterning Selected by Instruction Modifier

Bit	Description	Reset Value
31:28	Row3_Col7_Dither_Data	0
27:24	Row3_Col6_Dither_Data	0
23:20	Row3_Col5_Dither_Data	0
19:16	Row3_Col4_Dither_Data	0
15:12	Row3_Col3_Dither_Data	0
11:8	Row3_Col2_Dither_Data	0
7:4	Row3_Col1_Dither_Data	0
3:0	Row3_Col0_Dither_Data	0

Line Masking Selected by Instruction Modifier

Bit	Description	Reset Value
31:0	Line_Mask_Data	0

This register specifies either two rows of a 16×16 XY color pattern or XY stipple pattern, one row of an 8×8 XY dither pattern, or line mask pattern organization.

9.3.5 PATTERN_RAM_4_3D Register

Size (bits):	32
MMI/O Offset	4150h
Access Type	Read/Write

XY Color Patterning Selected by Instruction Modifier

Bit	Description	Reset Value
31:16	Row9_Color_Data	0
15:0	Row8_Color_Data	0

XY Stipple Patterning Selected by Instruction Modifier

Bit	Description	Reset Value
31:16	Row9_Stipple_Data	0
15:0	Row8_Stipple_Data	0

XY Dither Patterning Selected by Instruction Modifier

Bit	Description	Reset Value
31:28	Row4_Col7_Dither_Data	0
27:24	Row4_Col6_Dither_Data	0
23:20	Row4_Col5_Dither_Data	0
19:16	Row4_Col4_Dither_Data	0
15:12	Row4_Col3_Dither_Data	0
11:8	Row4_Col2_Dither_Data	0
7:4	Row4_Col1_Dither_Data	0
3:0	Row4_Col0_Dither_Data	0

Line Masking is Selected by Instruction Modifier

Bit	Description	Reset Value
31:0	Line_Mask_Data	0

This register specifies either two rows of a 16×16 XY color pattern or XY stipple pattern, one row of an 8×8 XY dither pattern, or line mask pattern organization.

9.3.6 PATTERN_RAM_5_3D Register

Size (bits):	32
MMI/O Offset	4154h
Access Type	Read/Write

XY Color Patterning Selected by Instruction Modifier

Bit	Description	Reset Value
31:16	Row11_Color_Data	0
15:0	Row10_Color_Data	0

XY Stipple Patterning Selected by Instruction Modifier

Bit	Description	Reset Value
31:16	Row11_Stipple_Data	0
15:0	Row10_Stipple_Data	0

XY Dither Patterning Selected by Instruction Modifier

Bit	Description	Reset Value
31:28	Row5_Col7_Dither_Data	0
27:24	Row5_Col6_Dither_Data	0
23:20	Row5_Col5_Dither_Data	0
19:16	Row5_Col4_Dither_Data	0
15:12	Row5_Col3_Dither_Data	0
11:8	Row5_Col2_Dither_Data	0
7:4	Row5_Col1_Dither_Data	0
3:0	Row5_Col0_Dither_Data	0

Line Masking Selected by Instruction Modifier

Bit	Description	Reset Value
31:0	Line_Mask_Data	0

This register specifies either two rows of a 16×16 XY color pattern or XY stipple pattern, one row of an 8×8 XY dither pattern, or line mask pattern organization.

9.3.7 PATTERN_RAM_6_3D Register

Size (bits):	32
MMI/O Offset	4158h
Access Type	Read/Write

XY Color Patterning Selected by Instruction Modifier

Bit	Description	Reset Value
31:16	Row13_Color_Data	0
15:0	Row12_Color_Data	0

XY Stipple Patterning Selected by Instruction Modifier

Bit	Description	Reset Value
31:16	Row13_Stipple_Data	0
15:0	Row12_Stipple_Data	0

XY Dither Patterning Selected by Instruction Modifier

Bit	Description	Reset Value
31:28	Row6_Col7_Dither_Data	0
27:24	Row6_Col6_Dither_Data	0
23:20	Row6_Col5_Dither_Data	0
19:16	Row6_Col4_Dither_Data	0
15:12	Row6_Col3_Dither_Data	0
11:8	Row6_Col2_Dither_Data	0
7:4	Row6_Col1_Dither_Data	0
3:0	Row6_Col0_Dither_Data	0

Line Masking Selected by Instruction Modifier

Bit	Description	Reset Value
31:0	Line_Mask_Data	0

This register specifies either two rows of a 16×16 XY color pattern or XY stipple pattern, one row of an 8×8 XY dither pattern, or line mask pattern organization.

9.3.8 PATTERN_RAM_7_3D Register

Size (bits):	32
MMI/O Offset	415Ch
Access Type	Read/Write

XY Color Patterning Selected by Instruction Modifier

Bit	Description	Reset Value
31:16	Row15_Color_Data	0
15:0	Row14_Color_Data	0

XY Stipple Patterning Selected by Instruction Modifier

Bit	Description	Reset Value
31:16	Row15_Stipple_Data	0
15:0	Row14_Stipple_Data	0

XY Dither Patterning Selected by Instruction Modifier

Bit	Description	Reset Value
31:28	Row7_Col7_Dither_Data	0
27:24	Row7_Col6_Dither_Data	0
23:20	Row7_Col5_Dither_Data	0
19:16	Row7_Col4_Dither_Data	0
15:12	Row7_Col3_Dither_Data	0
11:8	Row7_Col2_Dither_Data	0
7:4	Row7_Col1_Dither_Data	0
3:0	Row7_Col0_Dither_Data	0

Line Masking Selected by Instruction Modifier

Bit	Description	Reset Value
31:0	Line_Mask_Data	0

This register specifies either two rows of a 16×16 XY color pattern or XY stipple pattern, one row of an 8×8 XY dither pattern, or line mask pattern organization.

9.4 HostXY Unit Registers

The HostXY Unit registers define and control the operation of the HostXY Unit, and are listed in Table 9-14 in MMI/O offset order. They have no effect unless the Bus Master Enable bit of the PCI Command register (bit 2, MMI/O offset 304h) is enabled. The detailed register description is also provided in MMI/O offset order.

Table 9-14. HostXY Unit Registers

Register Name	Description	Format	MMI/O Offset	Page
HXY_BASE0_ADDRESS_PTR_3D	Host memory base address for XY bitmaps in host memory For example, a color buffer or Z buffer in host memory	32	4200h	9-91
HXY_BASE0_START_3D	Start_X and Start_Y for XY bitmaps in host memory	32	4204h	9-92
HXY_BASE0_EXTENT_3D	Extent_X and Extent_Y for XY bitmaps in host memory	32	4208h	9-93
Reserved	–	–	420Ch	–
HXY_BASE1_ADDRESS_PTR_3D	Host memory base address for linear bit-maps in host memory For example, texture maps stored in host memory	32	4210h	9-94
HXY_BASE1_OFFSET0_3D	Offset0 (to HXY_BASE1_ADDRESS_3D) for linear bitmaps in host memory	32	4214h	9-95
HXY_BASE1_OFFSET1_3D	Offset1 (to HXY_BASE1_ADDRESS_3D) for linear bitmaps in host memory	32	4218h	9-96
HXY_BASE1_LENGTH_3D	Length of linear bitmap in host memory (in bytes)		421Ch	9-97
HXY_HOST_CTRL_3D	HOSTXY Control register	32	4240h	9-98

9.4.1 HXY_BASE0_ADDRESS_PTR_3D Register

Size (bits):	32
MMI/O Offset	4200h
Access Type	Read/Write

Bit	Description	Reset Value
31:12	Base0 Address for XY Bitmaps in Host Memory	0
11:2	Physical Range for XY Bitmaps in Host Memory	0
1	Reserved	0
0	Virtual/Physical Control	0

This register specifies the host memory XY bitmap base address and range. This register has no effect unless enabled by the Bus Master Enable bit of the PCI Command register (bit 2, MMI/O offset 304h).

Bit	Description
31:12	**Base0 Address for XY Requests in Host Memory:** This 20-bit field has two meanings depending on the state of bit 0 of this register. It is either bits 31:12 of the physical address corresponding to the origin of the locked physically contiguous host memory area for XY bitmaps, or bits 31:12 of the physical address corresponding to the beginning of a 4-Kbyte locked, virtual-to-physical address translation table in host memory for XY bitmaps. Refer to *Laguna VisualMedia™ Accelerators Family — CL-GD546X, Volume II (Software Reference Manual, Second Edition, September 1996)*, “3D Programmer’s Guide” chapter. The Base0 Address is used: — when drawing to host memory as indicated by the Color_Buffer_Location and Z_Buffer_Location bits (bits 13 and 14) of the BASE0_ADDR_3D register, — when performing 2D BitBLTs with Y15 = 1, or — when performing master I/O XY operations (where the CL-GD5464, as PCI bus master fetches or stores data to/from host memory for the 2D BitBLT engine or the 3D engine).
11:2	**Physical Range for XY Bitmaps in Host Memory:** When bit 0 of this register is ‘0’ and the PCI_Addr_Check_En bit (bit 4) of the HOST_MASTER_CTL_3D register is ‘1’, this field defines the range of valid address accesses starting from the Base0 address. A value of ‘0’ in this field is invalid. Values of 1 through 1023 indicate the number of 4-Kbyte blocks that can be legally accessed from the base address. Invalid accesses cause exceptions.
1	**Reserved:** Set this bit to ‘0’.
0	**Virtual/Physical Control:** This bit controls whether the Base0 address field of this register points to a virtual address translation table, or to a physical address origin. If this bit is ‘1’ (virtual), the Base0 address is the physical address corresponding to the beginning of a 4-Kbyte locked, virtual-to-physical address translation table. If this bit is ‘0’ (physical), Base0 address is the physical address corresponding to the origin of the locked, physically contiguous host memory area for XY bitmaps.

9.4.2 HXY_BASE0_START_3D Register

Size (bits):	32
MMI/O Offset	4204h
Access Type	Read/Write

Bit	Description	Reset Value
31:30	Reserved	0
29:16	Start_Y	0
15:14	Reserved	0
13:0	Start_X	0

This register specifies the starting coordinate for XY operations to host memory. The host memory address first accessed is formed by the sum of the following:

— Base0 address from the HXY_BASE0_ADDRESS_PTR_3D register (or computed address after virtual-to-physical translation table lookup)

— Start_Y multiplied by the YPitch (from the HXY_HOST_CTL_3D register)

— Start_X value

This register has no effect unless enabled by the Bus Master Enable bit of the PCI Command register (bit 2, MMI/O offset 304h).

Bit	Description
31:30	**Reserved**
29:16	**Start_Y:** This field is the starting Y value (or line) of XY bitmap data in host memory.
15:14	**Reserved**
13:0	**Start_X:** This field is the starting X value of XY bitmap data in host memory, in 32-bit dwords.

9.4.3 HXY_BASE0_EXTENT_3D Register

Size (bits):	32
MMI/O Offset	4208h
Access Type	Read/Write

Bit	Description	Reset Value
31	Write_XY	
30:26	Reserved	0
25:16	Extent_Y	0
15:10	Reserved	0
9:0	Extent_X	0

This register specifies the extents of XY bitmaps in host memory. Writes to this register initiate PCI bus master cycles to host memory. Valid values must be programmed to the HXY_BASE0_ADDRESS_PTR_3D and HXY_BASE0_START_3D registers prior to programming this register.

This register has no effect unless enabled by the Bus Master Enable bit of the PCI Command register (bit 2, MMI/O offset 304h), and the HOSTXY Enable bit of the HXY_HOST_CTRL_3D register (bit 0, MMI/O offset 4240h).

Bit	Description
31	**Write_XY:** If this bit is set to '1', the CL-GD5464 as a PCI bus master writes XY bitmap data to host memory at addresses specified by the contents of this register, and the HXY_BASE0_ADDRESS_PTR_3D and HXY_BASE0_START_3D registers. If this bit is set to '0', the PCI bus master reads to host memory occur.
30:26	**Reserved:** Program these bits to '0h'.
25:16	**Extent_Y:** This field is the Y extent (or height in lines) of XY bitmap data in host memory.
15:10	**Reserved:** Program these bits to '0h'.
9:0	**Extent_X:** This field is the X extent in dwords of XY bitmap data in host memory.

9.4.4 HXY_BASE1_ADDRESS_PTR_3D Register

Size (bits):	32
MMI/O Offset	4210h
Access Type	Read/Write

Bit	Description	Reset Value
31:12	Base Address for Linear Bitmaps in Host Memory	0
11:2	Physical Range for Linear Bitmaps in Host Memory	0
1	Reserved	0
0	Virtual/Physical Control	0

This register specifies the host memory base address for linear bitmaps. It has no effect unless enabled by the Bus Master Enable bit of the PCI Command register (bit 2, MMI/O offset 304h).

Bit	Description
31:12	**Base1 Address for Linear Bitmaps in Host Memory:** This 20-bit field has two meanings depending on the value of bit 0 of this register. It is either bits 31:12 of the physical address corresponding to the origin of the locked physically contiguous host memory area for linear bitmaps, or it is bits 31:12 of the physical address corresponding to the beginning of a 4-Kbyte locked virtual-to-physical address translation table in host memory for linear bitmaps. Refer to *Laguna VisualMedia™ Accelerators Family — CL-GD546X, Volume II (Software Reference Manual, Second Edition, September 1996)*, “3D Programmer’s Guide” chapter. This Base1 address is used: — When fetching texture map data from host memory as indicated by the Texture_Location bit (bit 15) of the BASE0_ADDR_3D register. — When performing master I/O linear operations (where the CL-GD5464, as a PCI bus master fetches or stores data to/from host memory for the 2D BitBLT engine or the 3D engine).
11:2	**Physical Range for Linear Bitmaps in Host Memory:** When bit 0 of this register is ‘0’ and the PCI_Addr_Check_En bit (bit 4) of the HOST_MASTER_CTL_3D register is ‘1’, this field defines the range of valid address accesses starting from the Base1 address. A value of ‘0’ in this field is invalid. Values of 1 through 1023 indicate the number of 4-Kbyte blocks that can be legally accessed from the Base1 address. Invalid accesses cause exceptions.
1	**Reserved:** Set this bit to ‘0’.
0	**Virtual/Physical Control:** This bit controls whether the base address field of this register points to a virtual address translation table, or to a physical address origin. If this bit is ‘1’ (virtual), the Base1 address is the physical address corresponding to the beginning of the 4-Kbyte locked, virtual-to-physical address translation table for linear bitmaps in host memory. If this bit is ‘0’ (physical), Base1 address is the physical address corresponding to the origin of the locked, physically contiguous host memory area for linear bitmaps.

9.4.5 HXY_BASE1_OFFSET0_3D Register

Size (bits):	32
MMI/O Offset	4214h
Access Type	Read/Write

Bit	Description	Reset Value
31:22	Reserved	0
21:2	Linear_Offset0 [21:2]	0
1:0	Reserved	0

This register specifies an offset from BASE1_ADDRESS_3D for linear bitmap accesses. For example, for texture maps located in host memory. See also the HXY_BASE1_LENGTH_3D register on page 9-97.

This register has no effect unless enabled by the Bus Master Enable bit of the PCI Command register (bit 2, MMI/O offset 304h).

Bit	Description
31:22	**Reserved:** Program these bits to ‘0h’.
21:2	**Linear_Offset0 [21:2]:** First offset added to BASE1_ADDRESS_3D for linear bitmap addressing into the host memory. For example, this byte address offset (32-bit aligned) is the start of a texture map.
1:0	**Reserved:** Program these bits to ‘0h’ so that writes to bits 21:0 form a 32-bit-aligned byte address.

9.4.6 HXY_BASE1_OFFSET1_3D Register

Size (bits):	32
MMI/O Offset	4218h
Access Type	Read/Write

Bit	Description	Reset Value
31:22	Reserved	0
21:2	Linear_Offset1 [21:2]	0
1:0	Reserved	0

This register specifies another offset from BASE1_ADDRESS_3D for linear bitmap accesses. This register should not be programmed when tiled texture maps are located in host memory. See also the HXY_BASE1_LENGTH_3D register on page 9-97.

This register has no effect unless enabled by the Bus Master Enable bit of the PCI Command register (bit 2, MMI/O offset 304h).

Bit	Description
31:22	**Reserved:** Program these bits to ‘0h’.
21:2	**Linear_Offset1 [21:2]:** This field is the second offset to BASE1_ADDRESS_3D for linear bitmap addressing into host memory. This field is automatically updated by the 3D engine and should not be directly programmed when texture maps are located in host memory. This field should be programmed for master I/O linear accesses to host memory. This is a byte address offset (32-bit aligned).
1:0	**Reserved:** Program these bits to ‘0h’ so that writes to bits 21:0 form a 32-bit-aligned byte address.

9.4.7 HXY_BASE1_LENGTH_3D Register

Size (bits):	32
MMI/O Offset	421Ch
Access Type	Read/Write

Bit	Description	Reset Value
31	Write_Linear	
30	Enable_CPU_Generated_Textures	0
29:21	Reserved	0
20:2	Length_Linear	0
1:0	Reserved	0

This register specifies the length in bytes and type of linear host memory accesses. This register should not be programmed when tiled texture maps are located in host memory.

Writes to this register initiate PCI bus master cycles to host memory. Valid values must be programmed to the HXY_BASE1_ADDRESS_PTR_3D, HXY_BASE1_OFFSET0_3D, and HXY_BASE1_OFFSET1_3D registers prior to programming this register. The sum of these three registers forms the physical PCI address of the initial PCI bus master access. Note that the sum of the Linear_Offset0, Linear_Offset1, and Linear_Length must not be greater than 4 Mbytes.

This register has no effect unless enabled by the Bus Master Enable bit of the PCI Command register (bit 2, MMI/O offset 304h) and the HOSTXY Enable bit of the HXY_HOST_CTRL_3D register (bit 0, MMI/O offset 4240h).

Bit	Description
31	**Write_Linear:** If this bit is set to ‘1’, the CL-GD5464 as a PCI bus master writes linear bitmap data to host memory at addresses specified by the contents of this register, and the HXY_BASE1_ADDRESS_PTR_3D, HXY_BASE1_OFFSET0_3D and HXY_BASE0_OFFSET1_3D registers. If this bit is set to ‘0’, the PCI bus master reads to host memory occur.
30	**Enable_CPU_Generated_Textures:** If this bit is set to ‘1’, it enables CPU generated texture data to be fetched from host memory and is internally sent to the HOST_GEN_TEXT_DATA_3D port. The CPU generated texture is specific to one polygon and is fetched in a linear fashion. If this bit is set to ‘0’, the normal tiled texture data fetch from host memory occurs.
29:21	**Reserved:** Program these bits to ‘0h’.
20:2	**Length_Linear:** This field is the length (in bytes) of linear access. The CL-GD5464 automatically sets this field to 64 bytes for accesses to tiled texture maps located in host memory.
1:0	**Reserved:** Program these bits to ‘0h’ (forces length to be in dword multiples).

9.4.8 HXY_HOST_CTRL_3D Register

Size (bits):	32
MMI/O Offset	4240h
Access Type	Read/Write

Bit	Description	Reset Value
31:14	Reserved	0
13:8	Host YPitch	0
7:1	Reserved	0
0	HostXY Enable	0

This register specifies controls for the HostXY unit.

Bit	Description
31:14	**Reserved:** Program these bits to ‘0h’.
13:8	**Host YPitch:** This field stores the host drawing XY bitmap pitch (encoded in bytes).

Bits						Bitmap Pitch	Bits						Bitmap Pitch	Bits						Bitmap Pitch	Bits						Bitmap Pitch
13	12	11	10	9	8		13	12	11	10	9	8		13	12	11	10	9	8		13	12	11	10	9	8	
0	0	0	0	0	0	n/a	0	1	0	0	0	0	n/a	1	0	0	0	0	0	n/a	1	1	0	0	0	0	n/a
0	0	0	0	0	1	n/a	0	1	0	0	0	1	128	1	0	0	0	0	1	1024	1	1	0	0	0	1	n/a
0	0	0	0	1	0	n/a	0	1	0	0	1	0	n/a	1	0	0	0	1	0	2048	1	1	0	0	1	0	n/a
0	0	0	0	1	1	n/a	0	1	0	0	1	1	n/a	1	0	0	0	1	1	4096	1	1	0	0	1	1	n/a
0	0	0	1	0	0	n/a	0	0	0	1	0	0	n/a	1	0	0	1	0	0	n/a	1	1	0	1	0	0	n/a
0	0	0	1	0	1	n/a	0	1	0	1	0	1	256	1	0	0	1	0	1	1152	1	1	0	1	0	1	n/a
0	0	0	1	1	0	n/a	0	1	0	1	1	0	512	1	0	0	1	1	0	2304	1	1	0	1	1	0	n/a
0	0	0	1	1	1	n/a	0	1	0	1	1	1	n/a	1	0	0	1	1	1	4608	1	1	0	1	1	1	n/a
0	0	1	0	0	0	n/a	0	1	1	0	0	0	n/a	1	0	1	0	0	0	n/a	1	1	1	0	0	0	n/a
0	0	1	0	0	1	n/a	0	1	1	0	0	1	384	1	0	1	0	0	1	1280	1	1	1	0	0	1	n/a
0	0	1	0	1	0	n/a	0	1	1	0	1	0	768	1	0	1	0	1	0	2560	1	1	1	0	1	0	n/a
0	0	1	0	1	1	n/a	0	1	1	0	1	1	n/a	1	0	1	0	1	1	5120	1	1	1	0	1	1	n/a
0	0	1	1	0	0	n/a	0	1	1	1	0	0	n/a	1	0	1	1	0	0	n/a	1	1	1	1	0	0	n/a
0	0	1	1	0	1	n/a	0	1	1	1	0	1	640	1	0	1	1	0	1	1536	1	1	1	1	0	1	n/a
0	0	1	1	1	0	n/a	0	1	1	1	1	0	n/a	1	0	1	1	1	0	3072	1	1	1	1	1	0	n/a
0	0	1	1	1	1	n/a	0	1	1	1	1	1	n/a	1	0	1	1	1	1	6144	1	1	1	1	1	1	n/a

9.4.8 HXY_HOST_CTRL_3D Register *(cont.)*

Bit	Description
7:1	**Reserved**
0	**HOSTXY_Enable:** This bit enables PCI bus master cycles from the HostXY unit due to modification of the HXY_BASE1_LENGTH_3D and HXY_BASE0_EXTENT_3D registers. Modification of these registers can occur by a direct CPU write, a display list instruction write, internal modification by the CL-GD5464 on a (Y15 is '1') BitBLT, or when the color and/or Z buffer is in host memory. If this bit is set to '1', the PCI bus master cycles are enabled. If this bit is set to '0', the PCI bus master cycles are disabled. Writes to the HostXY unit register can still occur, but no action is initiated.

9.5 Mailbox Registers

The Mailbox registers are a set of 32-bit registers for use by software. These registers are typically used to communicate status from display list instruction executing on the CL-GD5464 to the CPU by the WRITE_DEV_REGS and READ_DEV_REGS instructions. These registers are listed in Table 9-15 in MMI/O offset order. The detailed register description is also provided in MMI/O offset order.

Table 9-15. Mailbox Registers

Register Name	Description	Format	MMI/O Offset	Page
MAILBOX0_3D	First mailbox	32	4260h	9-101
MAILBOX1_3D	Second mailbox	32	4264h	9-102
MAILBOX2_3D	Third mailbox	32	4268h	9-103
MAILBOX3_3D	Fourth mailbox	32	426Ch	9-104

9.5.1 MAILBOX0_3D Register

Size (bits):	32
MMI/O Offset	4260h
Access Type	Read/Write

Bit	Description
31:0	Mailbox0

This register is for software use only.

Bit	Description
31:0	**Mailbox0:** This 32-bit field stores the first mailbox.

9.5.2 MAILBOX1_3D Register

Size (bits):	32
MMI/O Offset	4264h
Access Type	Read/Write

Bit	Description
31:0	Mailbox1

This register is for software use only.

Bit	Description
31:0	**Mailbox1:** This 32-bit field stores the second mailbox.

9.5.3 MAILBOX2_3D Register

Size (bits):	32
MMI/O Offset	4268h
Access Type	Read/Write

Bit	Description
31:0	Mailbox2

This register is for software use only.

Bit	Description
31:0	**Mailbox2:** This 32-bit field stores the third mailbox.

9.5.4 MAILBOX3_3D Register

Size (bits):	32
MMI/O Offset	426Ch
Access Type	Read/Write

Bit	Description
31:0	Mailbox3

This register is for software use only.

Bit	Description
31:0	**Mailbox3:** This 32-bit field stores the fourth mailbox.

9.6 Prefetch Unit Registers

The Prefetch Unit registers are listed in Table 9-16 in MMI/O offset order. A detailed register description is also provided in offset order.

Table 9-16. Prefetch Unit Registers

Register Name	Description	Format	MMI/O Offset	Page
PF_BASE_ADDR_3D	Host memory base address for instruction buffer	32	4400h	9-106
PF_CTL_3D	Prefetch control	32	4404h	9-107
PF_DEST_ADDR_3D	Destination address	32	4408h	9-109
PF_FB_SEG_3D	Frame buffer segment (for WRITE_DEV_REGS to frame buffer)	x.11	440Ch	9-110
PF_INST_ADDR_3D	Manufacturing Test register (not normally used, it is the current prefetch instruction address)	32	4420h	9-111
PF_STATUS_3D	Prefetch status	32	4424h	9-112
HOST_MASTER_CTL_3D	–		4440h	9-114
PF_INST_3D	Current prefetch instruction	32	4480h	9-117

9.6.1 PF_BASE_ADDR_3D Register

Size (bits):	32
MMI/O Offset	4400h
Access Type	Read/Write

Bit	Description
31:12	Base Address for Instruction Buffer in Host Memory [31:12]
11:2	Physical Range for Instruction Buffer in Host Memory
1	Reserved
0	Virtual/Physical Control

This register is the host memory base address for the instruction buffer.

Bit	Description
31:12	**Base Address for Instruction Buffer in Host Memory [31:12]:** This 20-bit field has two meanings depending on the value of bit 0 of this register. It is either bits 31:12 of the physical address corresponding to the origin of the locked physically contiguous instruction buffer memory space, or it is the physical address corresponding to the beginning of a 4-Kbyte locked virtual-to-physical address translation table in off-board buffer space. Refer to *Laguna VisualMedia™ Accelerators Family — CL-GD546X, Volume II (Software Reference Manual, Second Edition, September 1996)*, “3D Programmer’s Guide” chapter. This address is used in all cases, as the instruction buffer is always located in host memory.
11:2	**Physical Range for Instruction Buffer in Host Memory:** When bit 0 of this register is ‘0’, and the PCI_Addr_Check_En bit (bit 4) of the HOST_MASTER_CTL_3D register is ‘1’, this field defines the range of valid address accesses starting from the base address. A value of ‘0’ in this field is invalid. Values of 1 through 1023 indicate the number of 4-Kbyte blocks that can be legally accessed from the base address. Invalid accesses cause exceptions.
1	**Reserved:** Set this bit to ‘0’.
0	**Virtual/Physical Control:** This bit controls whether the base address field of this register points to a virtual address translation table, or to a physical address origin. If this bit is set to ‘1’, the (virtual) address is the physical address corresponding to the beginning of a 4-Kbyte locked, virtual-to-physical address translation table for instruction buffer in host memory. If this bit is set to ‘0’, the (physical) address is the physical address corresponding to the origin of the locked, physically contiguous instruction buffer in host memory.

9.6.2 PF_CTL_3D Register

Size (bits):	32
MMI/O Offset	4404h
Access Type	Read/Write

Bit	Description	Reset Value
31:16	Reserved	0
15:8	User Defined Flags	0
7:6	Reserved	0
5	Enable_Interrupts_from_Prefetch_Engine	0
4	3D_Instruction_Tracking_Disable (For Manufacturing Test only)	0
3	Fetch_on_Request	0
2	Reserved	0
1	Pause_Instruction_Fetch	0
0	Enable_Instruction_Fetch	0

This register is for prefetch control.

Bit	Description
31:16	**Reserved**
15:8	**User Defined Flags:** These flags can be written to host memory using the READ_PFSTATUS_REG instruction.
7:6	**Reserved:** Program these bits to ‘0h’.
5	**Enable_Interrupts_from_Prefetch_Engine:** This bit enables interrupt of the host CPU by asserting the PCI INTA# output upon the prefetch engine generating an interrupt. The prefetch engine can generate an interrupt from the IDLE_INT instruction or from various interrupt events as detailed in the PF_STATUS_3D register. If this bit is set to ‘1’, it enables prefetch engine generated interrupts. If this bit is set to ‘0’, it disables prefetch engine generated interrupts.
4	**3D_Instruction_Tracking_Disable (For Manufacturing Test Only):** This bit is for manufacturing test only, and is not normally used. It disables prefetch engine tracking of 3D engine instruction execution. When this bit is disabled, the stalled instructions may not stall at the correct instruction boundary. If this bit is set to ‘1’, it disables draw instruction tracking in HostXY mode. If this bit is set to ‘0’, it enables draw instruction tracking.

9.6.2 PF_CTL_3D Register *(cont.)*

Bit	Description
3	**Fetch_on_Request:** If this bit is set to '1', instructions and parameters are fetched when requested by the execution engine to minimize the number of entries in the transaction queue and command FIFO. This bit must be set to '1' when using HostXY mode. If this bit is set to '0', instructions and parameters are prefetched so as to keep the transaction queue and command FIFO full. This setting is recommended for when not using HostXY mode.
2	**Reserved:** Set this bit to '0'.
1	**Pause_Instruction_Fetch:** If this bit is set to '1', while in Processor mode, instruction fetching pauses at the next instruction boundary at which point the Instruction_Fetch_Paused bit (bit 12) of the PF_STATUS_3D register changes from '0' to '1'. The prefetch engine retains information about the next instruction address. Subsequently, setting this bit to '0' resumes instruction fetching. Note that it is possible for instructions to be in the transaction queue and command FIFO when instruction fetching is paused. Instruction execution does not necessarily immediately halt. The Fetch_Mode bit (bit 11) of the PF_STATUS_3D register remains '1' when instruction fetching is paused. If this bit is set to '0', while in Coprocessor mode, it produces no effect.
0	**Enable_Instruction_Fetch:** If this bit is set to '1', it enables execution of BRANCH, CBRANCH, CBRANCH_NOT, CALL, and RETURN instructions written to the PF_INST_3D register. The BRANCH and CALL instructions when written to the PF_INST_3D register with a valid offset, begin instruction fetching (also known as display list fetching) from host memory. Instruction fetching and execution from host memory is also known as Processor mode. If this bit is set to '0', it disables execution of the BRANCH, CBRANCH, CBRANCH_NOT, CALL, and RETURN instruction when written to the PF_INST_3D register while in Coprocessor mode. Writes to this bit do not cause instruction fetching to begin. If this bit is set to '0', while in Coprocessor mode, it causes instruction fetching to be aborted.

9.6.3 PF_DEST_ADDR_3D Register

Size (bits):	32
MMI/O Offset	4408h
Access Type	Read/Write

Bit	Description
31:22	Reserved
21:2	Destination Address [21:2]
1	Reserved
0	Don't_Increment

This register is the Prefetch Destination Address register, and it provides a virtual address offset for data to be written back to host memory by the READ_DEV_REGS instruction.

This register can be written directly by the CPU or from the display list by the WRITE_DEST_ADDR instruction.

Bit	Description
31:22	**Reserved**
21:2	**Destination Address [21:2]**: This field contains the dword address offset of the start location where data is written by the READ_DEV_REGS instruction. The address used should be entirely within a locked 4-Kbyte page in physical memory that the requesting software controls.
1	**Reserved:** Set this bit to '0'.
0	**Don't_Increment:** If this bit is set to '0', the destination address is incremented after a write to host memory. If this bit is set to '1', the destination address is not incremented.

9.6.4 PF_FB_SEG_3D Register

Size (bits):	32
MMI/O Offset	440Ch
Access Type	Read/Write

Bit	Description
31:11	Reserved
10:0	Frame Buffer Segment

This register is the segment within the frame buffer that is written by a WRITE_DEV_REGS to the frame buffer.

This register can be written directly by the CPU or from the display list by the WRITE_PFCTL_REG instruction.

Bit	Description
31:11	**Reserved:** These bits are always ‘0h’.
10:0	**Frame Buffer Segment:** This 11-bit field is the frame buffer segment, written by a WRITE_DEVE_REGS instruction when addressed to the frame buffer.

9.6.5 PF_INST_ADDR_3D Register

Size (bits):	32
MMI/O Offset	4420h
Access Type	Read only

Bit	Description
31:22	Reserved
21:2	Current Instruction Address Offset [21:2]
1:0	Reserved

This register is the current prefetch instruction address offset.

Bit	Description
31:22	**Reserved:** These bits are always ‘0h’.
21:2	**Current Instruction Address Offset [21:2]:** This field has the current instruction address offset in dwords.
1:0	**Reserved:** These bits are always ‘0h’.

9.6.6 PF_STATUS_3D Register

Size (bits):	32
MMI/O Offset	4424h
Access Type	Read/Write

Bit	Description	Access	Reset Value
31:15	Reserved	Read only	0
14	Prefetch_Interrupt_Flag	Read only	0
13	Illegal_Instruction_Flag	Read only	0
12	Instruction_Fetch_Paused	Read only	0
11	Fetch_Mode	Read only	0
10	Display_List_Switch	Read/Write	0
9	Command_FIFO_Not_Empty_Flag	Read only	
8	BLT_Engine_Busy_Flag	Read only	
7	HostXY_Engine_Busy_Flag	Read only	
6	Execution_Engine_Busy_Flag	Read only	
5	Poly_Engine_Busy_Flag	Read only	
4	Z_Buffer_Compare_Flag	Read only	
3	CRT_Display_Buffer_Switch_Flag	Read only	
2	CRT_Line_Compare_Flag	Read only	
1	CRT_EVSync_Flag	Read only	
0	CRT_VSync_Flag	Read only	

This register is the Prefetch Status register. It is on the PCI side of the transaction queue, and a read only takes three PCI clocks and can occur at any time regardless of the Processor mode or HostXY mode operations in progress.

Bit	Description
31:15	**Reserved:** These bits are always ‘0h’.
14	**Prefetch_Interrupt_Flag:** If this read-only bit is ‘1’, it indicates the prefetch engine has IDLE_INT instruction. This bit is cleared to ‘0’ after a read of this register.
13	**Illegal_Instruction_Flag:** If this read-only bit is ‘1’, it indicates the prefetch engine has detected an illegal instruction since the last clear of this bit. This bit is cleared to ‘0’ after execution of a BRANCH instruction.
12	**Instruction_Fetch_Paused:** If this read-only bit is ‘1’, it indicates instruction fetching has been paused by setting the Pause_Instruction_Fetch bit (bit 1) of the PF_CTL_3D register.
11	**Fetch_Mode:** If this read-only bit is ‘1’, it indicates the prefetch engine is currently executing display list in Processor mode. If this bit is set to ‘0’, it indicates the prefetch engine is idle and the CL-GD5464 is in Coprocessor mode.

9.6.6 PF_STATUS_3D Register *(cont.)*

Bit	Description
10	**Display_List_Switch:** This read/write bit is used in conjunction with the WAIT_AND or WAIT_OR instructions. If this bit is set to '0' when display list executes a 'wait' (for this bit), display list execution pauses until this bit is set to '1' by the system CPU. An example application is the building of long display lists, where the system CPU takes longer to build new display lists than the CL-GD5464 takes to execute them.
9	**Command_FIFO_Not_Empty_Flag:** If this read-only bit is '1', it indicates the command FIFO in the 2D/3D engine has accepted an entry at the moment this register was read.
8	**BLT_Engine_Busy_Flag:** If this read-only bit is '1', it indicates the BitBLT engine was performing an operation at the moment this register was read.
7	**HostXY_Engine_Busy_Flag:** If this read-only bit is '1', it indicates the HostXY engine was performing a draw operation to host memory at the moment this register was read.
6	**Execution_Engine_Busy_Flag:** If this read-only bit is '1', it indicates the execution engine was executing an instruction at the moment this register was read.
5	**Poly_Engine_Busy_Flag:** If this read-only bit is '1', it indicates the polygon engine was drawing at the moment this register was read.
4	**Z_Buffer_Compare_Flag:** If this read-only bit is '1', it indicates the Z-buffer compare logic gave a 'true' result since the last clear of this bit.
3	**CRTC_Display_Buffer_Switch_Flag:** If this read-only bit is '1', it indicates that the CRT controller has been armed for a display buffer switch, but has not yet completed the switch. If this bit is '0', it indicates that either no display buffer switch was initiated, or that a display buffer switch has occurred since the last arming of the display buffer switch by the Multi-Buffer Enable bit in the Multi-Buffer Control register at MMI/O offset 148h.
2	**CRT_Line_Compare_Flag:** If this read-only bit is '1', it indicates the CRT controller issued a line compare 'true' event (that is, the CRT vertical counter is equal to the CRT LINE_COMPARE register) since the last clear of this bit.
1	**CRT_EVSync_Flag:** If this read-only bit is '1', it indicates the CRT controller vertical counter and the END_VERTICAL_SYNC register were equal at the moment this register was read.
0	**CRT_VSync_Flag:** If this read-only bit is '1', it indicates the CRT controller vertical counter and the START_VERTICAL_SYNC register were equal at the moment this register was read.

9.6.7 HOST_MASTER_CTL_3D Register

Size (bits):	32
MMI/O Offset	4440h
Access Type	Read/Write

Bit	Description	Access	Reset Value
31:17	Reserved	Read only	0
16	PCI_Address_Error	Read only	0
15	Slave_Retry_Execution_Eng	Read/Write	0
14	PCI_Greedy	Read/Write	0
13	Force_IRDY_BYTEEN	Read/Write	0
12	Page_Break_Detect_En	Read/Write	0
11	Slave_Retry_Processor_Mode	Read/Write	0
10	Slave_Retry_HostXY	Read/Write	0
9:8	Bi-endian_Aperture_Mode	Read/Write	0
7	PCI_Read_Control	Read/Write	0
6	PCI_Write_Control	Read/Write	0
5	PCI_Restart_Master	Read/Write	0
4	PCI_Addr_Check_En	Read/Write	0
3	Target_Abort_En	Read/Write	0
2	Master_Abort_En	Read/Write	0
1	PCI_Burst_Read_Disable	Read/Write	0
0	PCI_Burst_Write_Disable	Read/Write	0

This register controls the PCI bus behavior of the CL-GD5464. It can be accessed at any time regardless of the HostXY or Processor mode operations in progress.

Bit	Description
31:17	**Reserved:** These bits are always ‘0h’.
16	**PCI_Address_Error:** If this read-only bit is ‘1’, it indicates a PCI address error was detected. This occurs when address checking is enabled by the PCI_Addr_Check_En bit of this register, and the CL-GD5464 as a PCI bus master attempts to access an invalid PCI memory range.
15	**Slave_Retry_Execution_Eng:** If this bit is set to ‘0’, it causes all non-configuration PCI slave accesses to the CL-GD5464 to be retried while in Processor mode. If this bit is set to ‘1’, these PCI slave mode accesses to the CL-GD5464 are not retried.
14	**PCI_Greedy:** If this bit is set to ‘1’, the REQ# output is asserted until the completion of a PCI data phase. If this bit is set to ‘0’, the REQ# is deasserted on the clock after FRAME# is asserted.

9.6.7 HOST_MASTER_CTL_3D Register *(cont.)*

Bit	Description
13	**Force_IRDY_BYTEEN:** If this bit is set to '1', the PCI byte C/BE# pins are driven to 'fh' on a wait state of a burst write, masking all bytes. This is not PCI compliant. When this bit is set to '0', the byte enables from the last data phase carry over into the wait state for the next data phase. This is not PCI compliant, but less likely to be a problem since the byte enables rarely change during write cycles (see PCI specification v2.1 section 3.3.2).
12	**Page_Break_Detect_En:** For non-paged PCI bus master accesses, if this bit is set to '1', page-break detection at 4-Kbyte boundaries are enabled. For non-paged PCI bus master accesses, if this bit is set to '0', page-break detection are disabled. Paged PCI bus master accesses always have 4-Kbyte page-break detection enabled.
11	**Slave_Retry_Processor_Mode:** If this bit is set to '1', it causes all non-configuration PCI slave accesses to the CL-GD5464 to be retried while in Processor mode. If this bit is set to '0', these PCI slave mode accesses to the CL-GD5464 are not retried.
10	**Slave_Retry_HostXY:** If this bit is set to '1', it causes all non-configuration PCI slave accesses to the CL-GD5464 to be retried while texture fetches or drawing to host memory in HostXY mode are in progress. If this bit is set to '0', the PCI slave mode accesses to the CL-GD5464 are not retried.
9:8	**Bi-endian_Aperture_Mode:** This two-bit field selects the byte swapping for all PCI bus master data.
7	**PCI_Read_Control:** If this bit is set to '1', the PCI bus master reads multiple cycles occur (C/BE = 0110). If this bit is set to '0', the normal PCI bus master reads occur (C/BE = 1100).

Bits		Bi-Endian Master Mode	
9	**8**	**Name**	**Bytes in/out**
0	0	No swap	0123 ≥ 0123
0	1	Word swap	0123 ≥ 1032
1	0	Dword swap	0123 ≥ 3210
1	1	Dword swap	0123 ≥ 3210

9.6.7 HOST_MASTER_CTL_3D Register *(cont.)*

Bit	Description
6	**PCI_Write_Control:** If this bit is set to '1', the PCI bus master writes and invalid cycles occur (C/BE is '1111'). If this bit is set to '0', the normal PCI bus master writes occur (C/BE is '0111').
5	**PCI_Restart_Master:** If this bit is set to '1', the CL-GD5464 PCI bus master logic leaves the ABORT/ADDR_ERROR state and goes to an IDLE state. The correct recovery of the device is not guaranteed.
4	**PCI_Addr_Check_En:** For non-paged PCI bus master accesses, if this bit is set to '1', address checking is enabled.The ranges of addresses for non-paged accesses are specified by the Base Address Range fields (bits 11:2) of the PF_BASE_ADDR_3D, HXY_BASE0_ADDR_3D, and HXY_BASE1_ADDR_3D registers. For paged PCI bus master accesses, if this bit is set to '1', it enables checking of the page valid bit in the current page table entry. For either paged or non-paged accesses, if the checking indicates an incorrect valid bit or an out-of-range address (respectively), the PCI bus master cycle does not occur, and an interrupt is generated (PCI bus output pin INTA# is asserted). The PCI_Address_Error bit of this register is changed to '1' and the CL-GD5464 PCI bus master logic is halted (goes to an ABORT/ADDR_ERROR state). If this bit is set to '0', the checking is disabled and illegal PCI bus master accesses are allowed.
3	**Target_Abort_En:** If this bit is set to '1', it enables PCI target-abort detection. If target-abort is detected, it generates an interrupt, the PCI bus master logic is halted, and bit 12 of the PCI Status register (configuration 06h, MMI/O offset 306h) goes to '1'.
2	**Master_Abort_En:** If this bit is set to '1', it enables PCI master-abort detection. If a master-abort is detected, it generates an interrupt, the PCI bus master logic is halted, and bit 13 of the PCI Status register (configuration 06h, MMI/O offset 306h) goes to '1'.
1	**PCI_Burst_Read_Disable:** If this bit is set to '1', all PCI bus master read accesses are single dword transfers. If this bit is set to '0', read accesses of length greater than one are PCI v2.1 burst cycles.
0	**PCI_Burst_Write_Disable:** If this bit is set to '1', all PCI bus master write accesses are single dword transfers. If this bit is set to '0', write accesses of length greater than one are PCI v2.1 burst cycles.

9.6.8 PF_INST_3D Register

Size (bits):	32
MMI/O Offset	4480h
Access Type	Read/Write

Bit	Description
31:0	PF_Instruction

This register is written with prefetch engine instructions only; it is a port to read/write an instruction stream. This register is used to initiate instruction fetching from Coprocessor mode by writing a BRANCH opcode with an offset to the display list from the PF_BASE_ADDR_3D register. A BRANCH instruction causes a transition to Instruction Fetch mode, also known as Processor mode.

Bit	Description
31:0	**PF_Instruction:** Only the following opcodes and associated parameters should be written to this register while in a Coprocessor mode. BRANCH WRITE_DEST_ADDR RETURN (not normally written to this register) CLEAR_INT (not normally written to this register) SET_INT (not normally written to this register) TEST/TEST_AND/TEST_OR (not normally written to this register) NTEST_AND/NTEST_OR (not normally written to this register)

9.7 Host Address Registers

The host addresses for loading instructions and Data registers are listed in Table 9-17 in MMI/O offset order. The detailed register description is also provided in MMI/O offset order.

Table 9-17. Host Address Registers

Register Name	Description	Format	MMI/O Offset	Page
HOST_3D_DATA_PORT	Address range for 3D instructions and parameters; 1 Kbytes	1024 bytes	4800h–4BFFh	9-119
HOST_TEXTURE_DATA_PORT	Address range for host generated texture data; 1 Kbytes	1024 bytes	4C00h–4FFFh	9-120

9.7.1 HOST_3D_DATA_PORT Register

Size (bytes):	1024
MMI/O Offset	4800h–4BFFh
Access Type	Read/Write

Bit	Description
31:0	Coprocessor Mode Indirect Instructions and Parameters

This register specifies an address range for writing 3D instructions and parameters. Each data load to address range 0x4800 through 0x4BFF contains the CL-GD5464 register address in the instruction ‘M’ field and the number of sequential registers to load in the ‘A’ field.

Bit	Description
31:0	**Coprocessor Mode Indirect Instructions and Parameters:** Only the following opcodes and associated parameters should be written to this range of offsets: DRAW_POINT DRAW_LINE DRAW_POLY WRITE_REGISTER NOP CLEAR

9.7.2 HOST_TEXTURE_DATA_PORT Register

Size (bytes):	1024
MMI/O Offset	4C00h–4FFFh
Access Type	Read/Write

Bit	Description
31:0	Texture Data

This register specifies an address range for texture data to be written to the 3D engine.

Bit	Description
31:0	**Texture Data**

