CL-GD5465

Preliminary Data Book

FEATURES

- **64-bit graphics engine with integrated 3D game acceleration**
  - — Perspective textures mapping
  - — FilterJet™ fast bilinear filtering
  - — Lit, copy, decal, and blend textures
  - — Palettized textures (compressed textures)
  - — Mono rasterization (single-pass lighting)
  - — Stipple transparency
  - — Rendering of points, lines, and triangles
  - — 16-bit Z-buffer
  - — Gouraud shading
  - — Alpha blending, fog, and transparency
  - — Display list processing for maximum performance
  - — Texture mirroring and clamping
  - — 3D-clipping support
  - — Texture composition
  - — Full RGB specular lighting
- **High-performance 64-bit GUI accelerator**
  - — Hardware clipping
  - — Three-operand BitBLT (bit boundary block transfer)
  - — Color expansion for 8-, 16-, 24-, and 32-bpp modes
  - — Stretch BitBLT
- **AGP 1.0/PCI v2.1–compliant 66-MHz bus master**
  - — DMA maximizes system performance
  - — Host-rendered/cached texture maps
- **TV output**
  - — Digital output to support next generation of TV encoders
- **Integrated VGA controller**

(cont.)

High-Performance
3D AGP Graphics Accelerator

OVERVIEW

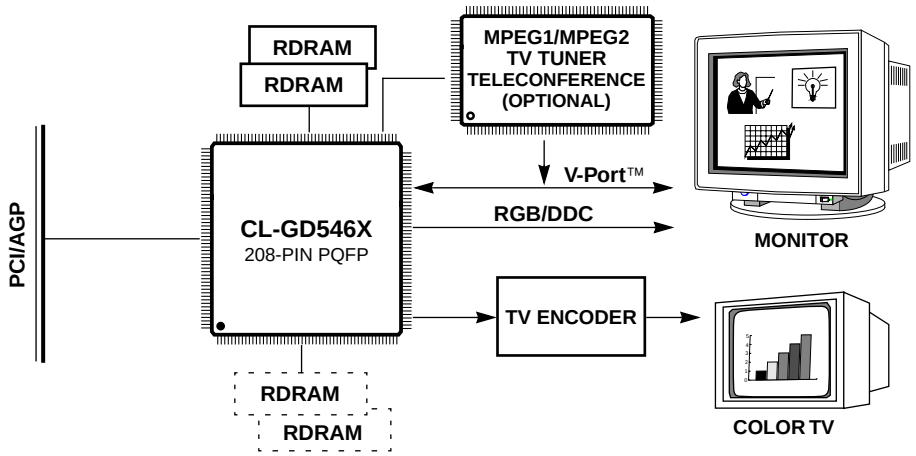
The CL-GD5465 is the third generation of the Laguna™ family of Rambus®-based 2D/3D graphics accelerators. The CL-GD5465 supports Intel® AGP (accelerated graphics port) and Microsoft® Direct3D™, enabling arcade-level 3D game play on desktop computers. In addition to superior 3D capabilities, the CL-GD5465 also offers a high level of 2D performance and video quality.

Based on TextureJet™ technology, the CL-GD5465 offers highly efficient hardware texture-map management. An AGP interface further enhances the texture management by providing high bandwidth between the system memory and the graphics subsystem. The CL-GD5465 is designed to optimize Microsoft Direct3D performance. This device is also compatible with other 3D game APIs on the market.

The CL-GD5465 integrates a 3D engine, a 2D engine, a 24-bpp palette RAMDAC, clock

(cont.)

System Block Diagram



FEATURES (cont.)

- **Video playback acceleration**
  - — Single-pass X, Y interpolated scaling
  - — Hardware occlusion for three video windows
  - — YUV-to-RGB conversion
  - — Color and chroma key
  - — Single overlay window
- **Rambus® memory architecture**
  - — Concurrent and low-latency devices supported
  - — Single memory for color-buffer, video, Z-buffer, and texture store
  - — 600 Mbytes/sec.
- **MPEG-2/DVD acceleration**
  - — DMA bursting
  - — Support for planar YUV 4:2:0 frees CPU of conversion burden
  - — Advanced hardware de-interlacing
- **V-Port™ for peripheral expansion**
  - — MPEG-2 decoder
  - — TV tuner
  - — Teleconferencing
- **Integrated 230-MHz palette DAC and clock synthesizer**
  - — Supports resolutions up to 1600 × 1200 at 85 Hz
  - — True-color operation up to 1024 × 768
  - — Hardware cursor
- **Microsoft® PC 97 and NEC 98–compliant architecture**

OVERVIEW (cont.)

generators, a V-Port™ bus, and digital TV-out circuits in a standard 208-pin HQFP package. The RAMDAC can operate at 230 MHz, allowing 1600 × 1200 resolution at 85-Hz refresh. The 3D engine features single-pass rendering capability, CPU-independent local display list processing, CPU-independent multi-buffer support, and OpenGL™ support. The 2D engine is based on previous Laguna family members and offers performance and feature enhancements.

The V-Port, GPIO, and I^2C bus interfaces provide a glueless connection to external devices to play back disk-based video files (including MPEG-2) and to provide TV-in-a-window, closed captioned, Intercast™, and video conferencing.

The CL-GD5465 is a single-channel device with bandwidth of 600 Mbytes per second. While maintaining the same pin layout, future Laguna family members will use two Rambus channels to increase the bandwidth to 1.3 Gbytes per second.

APPLICATIONS SUPPORT

- **Technical reference manuals and design kit — complete data book, electrical specifications, register set definitions, pin descriptions, reference designs, and applications information.**
- **BIOS and driver release kits — contains user guides, PDR (problem description report) forms, source code license agreement, and quality assurance procedures.**
- **PCI board evaluation kit — adapter card including CL-GD5465, on-board BIOS, and 2-Mbyte RDRAM shipped with complete design package (schematics, Gerber® files) and software drivers.**
- **Electronic information services**
  - — ftp: ftp.cirrus.com
  - — World Wide Web: http://www.cirrus.com/
  - — BBS: (510) 440-9080
  - — Fax-on-demand: (510) 249-4200

LOCALIZATION

- **Simplified Chinese**
- **Traditional Chinese**
- **Czech**
- **Danish**
- **Dutch**
- **Finnish**
- **French**
- **German**
- **Hungarian**
- **Italian**
- **Japanese**
- **Korean**
- **Norwegian**
- **Polish**
- **Brazilian Portuguese**
- **Portuguese**
- **Russian**
- **Latin American Spanish**
- **Spanish**
- **Swedish**
- **Thai**

SOFTWARE DRIVERS SUPPORT

Cirrus Logic provides an extensive and expanding range of software drivers to enhance the resolution and performance of many software packages. The following table lists the Cirrus Logic software drivers for the CL-GD5465.

Software Drivers	Resolution Supported	No. of Colors
Microsoft® Windows®, Microsoft® DCI Provider (display control interface), Microsoft® Windows® 95, Microsoft® DirectDraw™, Microsoft® Direct3D™	640 × 480, 800 × 600, 1024 × 768, 1280 × 1024, 1600 × 1200	256 (8 bit)
	640 × 480, 800 × 600, 1024 × 768, 1280 × 1024	65,536 (16 bit)
	640 × 480, 800 × 600, 1024 × 768	16.8 million (24 bit)
	640 × 480, 800 × 600, 1024 × 768	16.8 million (32 bit)
Microsoft® Windows NT™	640 × 480, 800 × 600, 1024 × 768, 1280 × 1024, 1600 × 1200	256 (8 bit)
	640 × 480, 800 × 600, 1024 × 768, 1280 × 1024	65,536 (16 bit)
	640 × 480, 800 × 600, 1024 × 768	16.8 million (24 bit)
	640 × 480, 800 × 600, 1024 × 768	16.8 million (32 bit)
AutoCAD®, AutoShade® with Renderman™, 3D Studio™, MicroStation®	640 × 480, 800 × 600, 1024 × 768, 1280 × 1024, 1600 × 1200	256 (8 bit)
	640 × 480, 800 × 600, 1024 × 768, 1280 × 1024	65,536 (16 bit)
	640 × 480, 800 × 600, 1024 × 768	16.8 million (24 bit)
OS/2® v3.x, Warp	640 × 480, 800 × 600, 1024 × 768, 1280 × 1024	256 (8 bit)
	640 × 480, 800 × 600, 1024 × 768	65,536 (16 bit)
VPM™ (video port manager)	Resolution-independent	–
Apple™ PowerMAC®	640 × 480, 800 × 600, 1024 × 768, 1280 × 1024	16.8 million

BIOS SUPPORT

- **Fully IBM® VGA-compatible BIOS**
- **VBE (VESA® BIOS Extension) v2.0 support**
- **AGP/PCI support**
- **DPMS (display power management signaling) and DDC2B support in ROM**
- **Plug-and-play support**

UTILITIES

- **Manufacturing test**
- **Video-mode configuration utility: CLMODE**
- **Configured OEM system integration: OEMSI**
- **Resolution switching utility: WINMODE**
- **RAMBIOS utility**
- **Screen centering utility**
- **Register editor and viewer**

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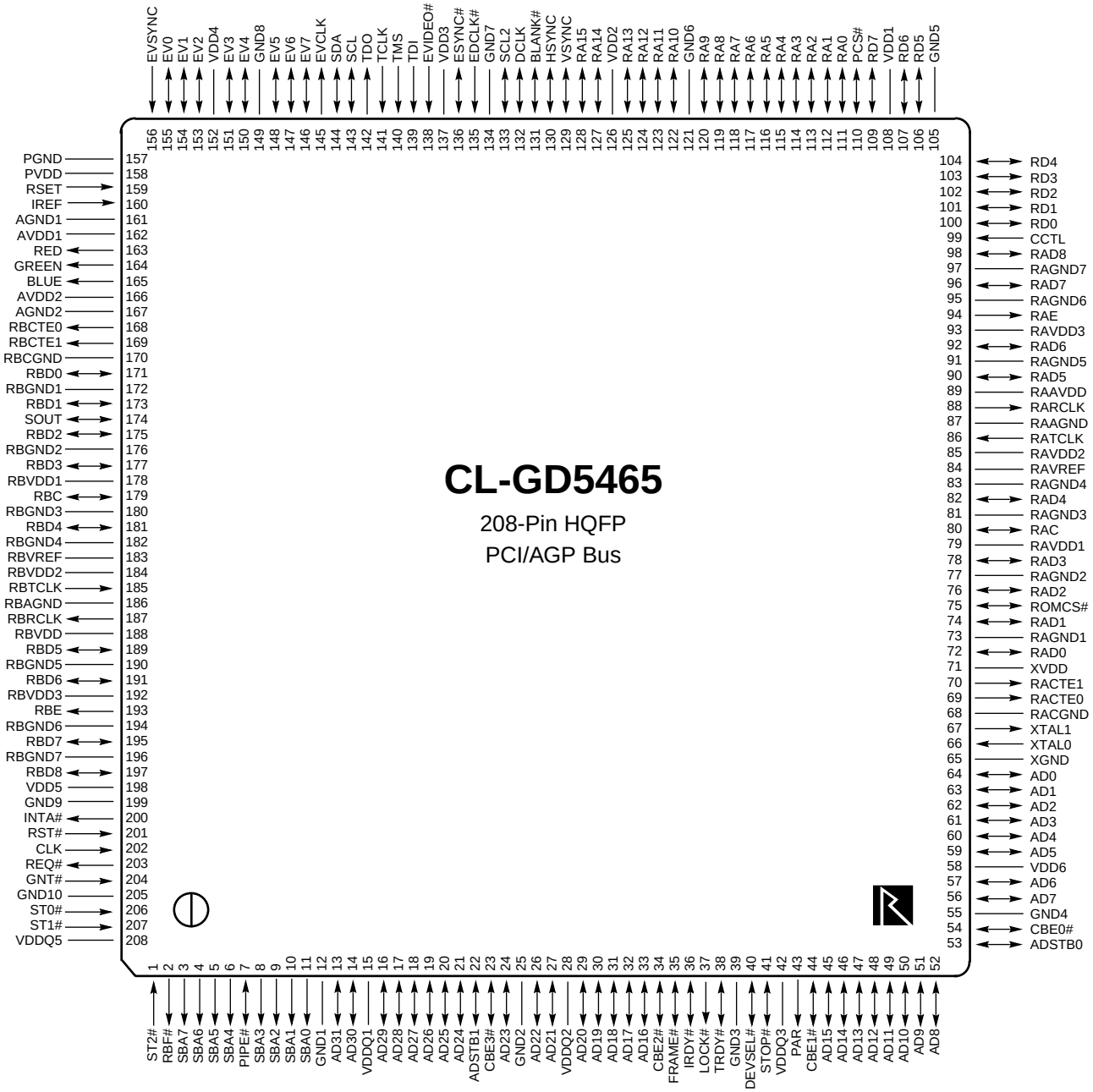
1. PIN INFORMATION

The CL-GD5465 is available in a 208-pin high-performance quad-flat pack device for the PCI/AGP bus interface.

1.1 Pin Diagram — PCI/AGP Bus



1.2 Pin Summary

The following tables list each CL-GD5465 pin by name, functional pin type, and number(s). Functional pin types are abbreviated as follows:

Type	Abbreviation
Input	I
Output	O
Input/output	I/O
Tristate output	TS
Power	PWR

Type	Abbreviation
Ground	GND
Open collector	OC
'–'	Indicates ascending pin numbers
':'	Indicates descending pin numbers
'#'	Indicates active-low

1.2.1 Host Interface Pins

Table 1-1. Host Interface — PCI Bus

Name	Type	Pull-up	I_{OH} (mA)	I_{OL} (mA)	Load (pF)	Pin Number(s)
RST#	I	–	–	–	–	201
CLK	I	–	–	–	–	202
GNT#	I	–	–	–	–	204
PAR	O	–	–2	8	50	43
REQ#	O	–	–	–	–	203
INTA#	TS	–	–2	8	50	200
FRAME#	I/O	–	–2	8	50	35
IRDY#	I/O	–	–2	8	50	36
TRDY#	I/O	–	–2	8	50	38
DEVSEL#	I/O	–	–2	8	50	40
STOP#	I/O	–	–2	8	50	41
AD[31:0]	I/O	–	–2	8	50	13–14, 16–21, 24, 26–27, 29–33, 45–52, 56–57, 59–64
CBE[3:0]#	I/O	–	–2	8	50	23, 34, 44, 54
ADSTB1 (IDSEL)	I/O	–	–2	8	50	22
ADSTB0	I/O	–	–2	8	50	53
LOCK#	O	–	–2	8	50	37
ST[2:0]#	I	–	–	–	–	1, 207, 206
RBF#	O	–	–2	8	50	2
SBA[7:0]	O	–	–2	8	50	3–6, 8–11
PIPE#	I/O	–	–2	8	50	7

1.2.2 ROM/VMI Interface

These pins are used for the BIOS ROM interface, as a connection to a VMI v1.4 peripheral, or as the interface to the VGA feature connector.

Table 1-2. ROM/VMI Interface

ROM	VMI	Feature Connector	Test Output	Type	Pull-up	I_{OH}	I_{OL}	Load (pF)	Pin Number(s)
EVIDEO#	VACTIVE	EVIDEO#	–	I	–	–	–	–	138
ESYNC#	–	ESYNC#	–	I/O	–	–4	8	50	136
EDCLK#	VREF	EDCLK#	–	I	–	–	–	–	135
SCL2	I2CCLK	–	–	I/O	–	–	8	–	133
DCLK	PIXCLK	DCLK	–	I/O	–	–4	8	50	132
BLANK#	HREF	BLANK#	–	I/O	–	–4	8	50	131
HSYNC[a]	–	HSYNC	–	I/O	–	–4	8	50	130
VSYNC	–	VSYNC	–	I/O	–	–4	8	50	129
RA15	I2CDAT	–	–	I/O	–	–	8	50	128
RA14	VID0	P0	T24	I/O	–	–4	8	50	127
RA13	VID1	P1	T25	I/O	–	–4	8	50	125
RA12	VID2	P2	T26	I/O	–	–4	8	50	124
RA11	VID3	P3	T27	I/O	–	–4	8	50	123
RA10	VID4	P4	T28	I/O	–	–4	8	50	122
RA9	VID5	P5	T29	I/O	–	–4	8	50	120
RA8	VID6	P6	T30	I/O	–	–4	8	50	119
RA7	VID7	P7	T31	I/O	–	–4	8	50	118
RA6	DS# or RD#	–	T8	I/O	–	–4	8	50	117
RA5	R/W# or WR#	–	T9	I/O	–	–4	8	50	116
RA4	DTACK# or READY	–	T10	I/O	–	–4	8	50	115
RA3	HA3	–	T11	I/O	–	–4	8	50	114
RA2	HA2	–	T12	I/O	–	–4	8	50	113
RA1	HA1	–	T13	I/O	–	–4	8	50	112
RA0	HA0	–	T14	I/O	–	–4	8	50	111
PCS#	CS#	–	T15	I/O	–	–4	8	50	110
RD7	HD7	–	T7	I/O	–	–4	8	50	109
RD6	HD6	–	T6	I/O	–	–4	8	50	107
RD5	HD5	–	T5	I/O	–	–4	8	50	106

Table 1-2. ROM/VMI Interface *(cont.)*

ROM	VMI	Feature Connector	Test Output	Type	Pull-up	I_{OH}	I_{OL}	Load (pF)	Pin Number(s)
RD4	HD4	–	T4	I/O	–	–4	8	50	104
RD3	HD3	–	T3	I/O	–	–4	8	50	103
RD2	HD2	–	T2	I/O	–	–4	8	50	102
RD1	HD1	–	T1	I/O	–	–4	8	50	101
RD0	HD0	–	T0	I/O	–	–4	8	50	100
ROMCS#	–	–	–	I/O	–	–4	8	50	75

[a] HSYNC and VSYNC are also listed in Table 1-5.

1.2.3 Rambus® Pins

The CL-GD5465 has only one Rambus Channel — Rambus Channel A. Rambus Channel B pins are reserved for future Laguna family members, and are not implemented on the CL-GD5465. The Rambus Channel pins, including SOUT, are not 5-V tolerant. See Section 6.2 on page 35 for restrictions.

Table 1-3. Rambus® Channel A Pins

Name	Type	Pin Number(s)
RAD[8:0]	I/O	98, 96, 92, 90, 82, 78, 76, 74, 72
RARCLK	O	88
RATCLK	I	86
RACTE1	O	70
RACTE0	O	69
RAC	I/O	80
RAE	O	94
RAVREF	I	84
CCTL	I	99

Rambus Channel B pins are not implemented on the CL-GD5465 (except SOUT, pin 174), but are reserved for future Laguna family members.

Table 1-4. Rambus® Channel B Pins

Name	Type	Pin Number(s)
RBD[8:0]	I/O	197, 195, 191, 189, 181, 177, 175, 173, 171
RBRCLK	O	187
RBTCLK	I	185
RBCTE1	O	169
RBCTE0	O	168
RBC	I/O	179
RBE	O	193
RBVREF	I	183
SOUT	I/O	174 (not 5-V tolerant, see Section 6.2)

1.2.4 Monitor Pins

The following pins connect to the DB15 monitor connector. The two control pins for the DACs are included.

Table 1-5. Monitor Pins

Name	Type	Pull-up[a]	I_{OH} (mA)	I_{OL} (mA)	Load (pF)	Pin Number(s)
RED	O	–	Analog output			163
GREEN	O	–				164
BLUE	O	–				165
RSET	I	–	–	–	–	159
IREF	I	–	–	–	–	160
HSYNC[a]	I/O	250K	–4	8	50	130
VSYNC	I/O	250K	–4	8	50	129
SDA	I/O	–	–	8	50	144
SCL	I/O	–	–	8	50	143

[a] HSYNC and VSYNC are also listed in Table 1-2.

1.2.5 TV Output Pins

These pins interface to the CL-GD1052/GD1053 TV encoder. A strapping option allows EV[7:0] to be redefined as P[7:0]. This option precludes their use as TV outputs.

Table 1-6. TV Output Pins

Name	Pixel Bus	Test Output	Type	Pull-up[a]	I_{OH} (mA)	I_{OL} (mA)	Load (pF)	Pin Number(s)
EVCLK	–	–	O	–	–4	8	50	145
EV7	P7	T23	I/O	–	–4	8	50	146
EV6	P6	T22	I/O	–	–4	8	50	147
EV5	P5	T21	I/O	–	–4	8	50	148
EV4	P4	T20	I/O	–	–4	8	50	150
EV3	P3	T19	I/O	–	–4	8	50	151
EV2	P2	T18	I/O	–	–4	8	50	153
EV1	P1	T17	I/O	–	–4	8	50	154
EV0	P0	T16	I/O	–	–4	8	50	155
EVSYNC	–	–	I	–	–	–	–	156

1.2.6 Boundary Scan Pins

The boundary scan (IEEE 1149.1) is not implemented on the CL-GD5465. These pins should be ‘no connects’.

Table 1-7. Boundary Scan Pins

Name	Type	Pull-up	I_{OH} (mA)	I_{OL} (mA)	Load (pF)	Pin Number(s)
TDI	I	–	–	–	–	139
TMS	I	–	–	–	–	140
TCLK	I	–	–	–	–	141
TDO	O	–	–4	8	50	142

1.2.7 Clock Pins

Table 1-8. Clock Pins

Name	Type	Pull-up	I_{OH} (mA)	I_{OL} (mA)	Load (pF)	Pin Number(s)
XTAL0 (RCLK)	I	–	–	–	–	66
XTAL1	O	–	–	–	–	67

1.2.8 Power and Ground Pins

Table 1-9. Power and Ground Pins

Name	Type	Pin Number(s)
VDD[6:1]	Digital power (core logic)	198, 152, 137, 126, 108, 58
VDDQ[5, 3:1]	Digital power (AGP I/O)	208, 42, 28, 15
RAVDD[3:1]	Digital power (Rambus Channel A interface cell)	93, 85, 79
RAAVDD	Analog power (Rambus Channel A interface cell)	89
RBVDD[3:1]	Digital power (Rambus Channel B interface cell)	192, 184, 178
RBAVDD	Analog power (Rambus Channel B interface cell)	188
XVDD	Power (Reference oscillator and Rambus PLL)	71
PVDD	Power (VCLK PLL)	158
AVDD[2:1]	Power (DACs)	166, 162
GND[10:1]	Digital ground (core logic and I/O)	205, 199, 149, 134, 121, 105, 55, 39, 25, 12
RAGND[7:1]	Digital ground (Rambus Channel A interface cell)	97, 95, 91, 83, 81, 77, 73
RAAGND	Analog ground (Rambus Channel A interface cell)	87
RACGND	Ground (Rambus Channel A ClockToEnd drivers)	68
RBGND[7:1]	Digital ground (Rambus Channel B interface cell)	196, 194, 190, 182, 180, 176, 172
RBAGND	Analog ground (Rambus Channel B interface cell)	186
RBCGND	Ground (Rambus Channel B ClockToEnd drivers)	170
XGND	Ground (Reference oscillator and Rambus PLL)	65
PGND	Ground (VCLK PLL)	157
AGND[2:1]	Ground (DACs)	167, 161

2. DETAILED PIN DESCRIPTIONS

The following tables provide a detailed description of each CL-GD5465 pin by name and functional type. Functional pin types are abbreviated as follows:

Type	Abbreviation
Input	I
Output	O
Input/output	I/O
Tristate output	TS
Power	PWR

Type	Abbreviation
Ground	GND
Open collector	OC
'–'	Indicates ascending pin numbers
':'	Indicates descending pin numbers
'#'	Indicates active-low

2.1 PCI/AGP Pins

Table 2-1. Host Interface — PCI/AGP Bus

Name	Type	Description
RST#	I	**System Reset #:** This active-low input initializes the CL-GD5465 to a known state. Configuration bits are loaded on the rising (trailing) edge of this signal. The Subsystem ID registers are loaded from the BIOS ROM after the trailing edge of this signal.
CLK	I	**PCI Bus Clock:** This is the bus timing reference for the CL-GD5465. All synchronous PCI bus activity is referenced to the rising edge of this clock.
GNT#	I	**Bus Grant #:** This active-low input indicates the arbiter has determined that the CL-GD5465 can become master of the PCI bus.
PAR	TS	**Parity:** This pin provides even parity across AD[31:0] and CBE[3:0]#. The CL-GD5465 asserts correct parity when it drives the bus. The CL-GD5465 does not check parity. Correct parity is asserted by the CL-GD5465 (as a target) in the data phase of reads. When the CL-GD5465 is a bus master, it provides correct parity in the address phase and for writes in the data phase.
LOCK#	O	**LOCK #:** This pin indicates an atomic operation that may require multiple transactions to complete.
REQ#	O	**Bus Request #:** This active-low output requests mastership of the PCI bus.
INTA#	TS	**Interrupt Request #:** This active-low output indicates that the CL-GD5465 has an interrupt pending. See register CR11 for a description of the controls for this pin. This pin is functionally an open-drain output driver. INTA# can be tied directly to ground if interrupts are not required. In this case, the CL-GD5465 does not claim an interrupt.
FRAME#	I/O	**Cycle Frame #:** This pin is driven by the current master to indicate the beginning and duration of an access. When the CL-GD5465 is a bus master, this output is a sustained tristate as defined in the PCI specification. FRAME# is asserted to indicate the beginning of a bus transaction. While FRAME# is asserted, data transfers continue. The transaction is in its final data phase when FRAME# is deasserted.
IRDY#	I/O	**Initiator Ready #:** This pin indicates the initiating agent's ability to complete the current data phase. When the CL-GD5465 is a bus master, this output is a sustained tristate as defined in the PCI specification. A data phase is completed on any clock cycles that IRDY# and TRDY# are both asserted.

Table 2-1. Host Interface — PCI/AGP Bus *(cont.)*

Name	Type	Description
TRDY#	I/O	**Target Ready #:** This pin indicates the target agent's ability to complete the current data phase. This output is a sustained tristate as defined in the PCI specification. This pin is an input for palette snooping when the CL-GD5465 is a target. When the CL-GD5465 is a bus master, this pin is an input.
DEVSEL#	I/O	**Device Select #:** This output is driven active-low when the CL-GD5465 has decoded its address as the target of the current access. This output is a sustained tristate as defined in the PCI specification. This pin is an input for palette snooping when the CL-GD5465 is a target. When the CL-GD5465 is a bus master, this pin is an input.
STOP#	I/O	**Stop #:** This active-low output indicates a request to the bus master to stop the current transaction. This output is a sustained tristate as defined in the PCI specification. This pin is an input for palette snooping when the CL-GD5465 is a target. When the CL-GD5465 is a bus master, this pin is an input.
AD[31:0]	I/O	**Address/Data:** These multiplexed and bidirectional pins are used to transfer system address and data during any memory or I/O operation. During the first clock of a transaction, these pins contain a 32-bit physical byte address. During subsequent clocks, they contain data.
CBE[3:0]#	I/O	**Command/Byte Enable #:** These multiplexed pins are used to transfer the bus command and the byte enables. During the address phase of the operation, CBE[3:0]# define the bus command (refer to Table 2-2). The CL-GD5465 responds as a target to the values listed in the following table. When the CL-GD5465 is a bus master, it generates memory read and memory write commands. During the data phase(s), these pins are used as byte enables.
ADSTB1 (IDSEL)	I	**AD Strobe/Initialization Device Select:** The definition of this pin depends on the host bus configuration strapping (RA[6:4]). In PCI modes, this input is a chip select in place of the upper 24 address bits during configuration read and write cycles. In 133-MHz AGP modes, this input strobes data on AD[31:16] and CBE[3:2]#. This pin is not used in 66-MHz AGP mode.

Table 2-2. Commands

CBE[3:0]#	Command Type
02h	I/O read
03h	I/O write
06h	Memory read
07h	Memory write
Ah	Configuration read
Bh	Configuration write

Table 2-1. Host Interface — PCI/AGP Bus *(cont.)*

Name	Type	Description
ADSTB0 (M66EN)	I/O	**AD Strobe:** The definition of this pin depends on the host bus configuration strapping (RA[6:4]). In 133-MHz AGP mode, this input strobes data on pins AD[15:0] and CBE[1:0]#. This pin is not used for 66-MHz AGP mode. In 66-MHz PCI mode, this pin is an input. If this pin is '1' at the trailing edge of RESET, the system runs at 66 MHz and the CL-GD5465 selects the medium DEVSEL speed. If this pin is '0' at the trailing edge of RESET, the system is going to run at 33 MHz and the CL-GD5465 selects the fast DEVSEL speed. In 33-MHz PCI mode, this pin is an output and is driven low (even during RESET). This indicates to the PCI bus that this PCI device is not capable of 66-MHz operation; the fast DEVSEL speed is selected.
ST[2:0]#	I	**Status #:** In AGP mode, this bus provides information from the arbiter to a master on what the master can do. This bus has meaning to the master when its GNT# is asserted and must be otherwise ignored.
RBF#	O	**Read Buffer Full #:** When this output is low, it indicates that the CL-GD5465 is ready to receive previously requested low-priority read data. This pin is not used in PCI mode.
SBA[7:0]	O	**Sideband Address:** This pin is not used in AGP pipelined addressing or PCI modes.
PIPE# (SBSTB)	I/O	**Pipelined Request #:** The definition of this pin depends on the host bus configuration strapping (RA[6:4]). PIPE# is asserted with FRAME# for the PCI master cycles in AGP Stealth mode. This pin is not used in PCI modes.

2.2 ROM/VMI Pins

Table 2-3. ROM/VMI Pins

Name	Type	Description
EVIDEO# (VACTIVE)	I	**Enable Video #:** If the CL-GD5465 is not configured for VMI, this pin controls the buffers on the feature connector pixel bus (either RA[14:7] or EV[7:0]). If the CL-GD5465 is configured for VMI, this input is VACTIVE. VACTIVE indicates that valid pixel data is being transmitted on the VID bus.
ESYNC#	I/O	**Enable Sync and Blank #:** If the CL-GD5465 is not configured for VMI, this pin controls the buffers of the feature connector HSYNC, VSYNC, and BLANK# pins. If the CL-GD5465 is configured for VMI, this pin is a general-purpose I/O.
EDCLK# (VREF)	I	**Enable Dot Clock #:** If the CL-GD5465 is not configured for VMI, this input is used to the control the buffer on DCLK. If the CL-GD5465 is configured for VMI, this is the VREF input.
DCLK (PIXCLK)	I/O	**Dot Clock:** If the CL-GD5465 is not configured for VMI, this is the feature connector DCLK pin. The buffer is controlled by EDCLK#. If the CL-GD5465 is configured for VMI, this is the PIXCLK input.
BLANK# (HREF)	I/O	**BLANK #:** If the CL-GD5465 is not configured for VMI, this is the feature connector BLANK# I/O. The buffer is controlled with ESYNC#. If the CL-GD5465 is configured for VMI, this is the HREF input.
HSYNC[a]	I/O	**Horizontal Sync:** This output supplies the horizontal synchronization signal to the monitor. The polarity of this output is programmable. This pin is put into high-impedance when ESYNC# is low.

Table 2-3. ROM/VMI Pins *(cont.)*

Name	Type	Description
VSYNC	I/O	**Vertical Sync:** This output supplies the vertical synchronization signal to the monitor. The polarity of this output is programmable. This pin is put into high-impedance when ESYNC# is low.
RA15	I/O	**ROM Address 15:** This pin supplies address bit 15 if the CL-GD5465 is configured for a 64K BIOS. This pin is also the data pin for the second I^2C interface. If a pull-down resistor is installed on RA15, the CL-GD5465 is configured for a 32K BIOS and this pin is only used for the second I^2C interface.
RA[14:7]	I/O	**ROM Address [14:7]:** These pins supply address bits 14 through 7. If the CL-GD5465 is configured for VMI mode, these pins are also the video input bus (VID[0–7]). If no pull-down resistor is installed on RA1, these pins are also used for the feature connector pixel bus (P[0–7]). If the CL-GD5465 is in Test mode, these pins are used for T[24–31].
RA6	I/O	**ROM Address 6:** This pin supplies address bit 6. If the CL-GD5465 is configured for VMI mode, this pin supplies DS# or RD#, according to the VMI mode. If the CL-GD5465 is in Test mode, this pin is used for T8.
RA5	I/O	**ROM Address 5:** This pin supplies address bit 5. If the CL-GD5465 is configured for VMI mode, this pin supplies R/W# or WR#, according to the VMI mode. If the CL-GD5465 is in Test mode, this pin is used for T9.
RA4	I/O	**ROM Address 4:** This pin supplies address bit 4. If the CL-GD5465 is configured for VMI mode, this pin is used for DTACK# or READY, according to the VMI mode. If the CL-GD5465 is in Test mode, this pin is used for T10.
RA[3:0]	I/O	**ROM Address [3:0]:** These pins supply address bits 13 through 0. If the CL-GD5465 is configured for VMI mode, these pins also supply the host address (HA[3:0]). If the CL-GD5465 is in Test mode, these pins are used for T[11–14].
PCS#	I/O	**VMI Peripheral Chip Select #:** If the CL-GD5465 is configured for VMI mode, this pin supplies the chip select. If the CL-GD5465 is in Test mode, this pin is used for T15.
RD[7:0]	I/O	**ROM Data [7:0]:** These pins are the ROM data bus. If the CL-GD5465 is configured for VMI mode, these pins are the host data bus (HD[7:0]). If the CL-GD5465 is in Test mode, these pins are used for T[7:0].
ROMCS#	I/O	**ROM Chip Select #:** This pin enables the ROM data onto the RD bus. If this pin is tied to low (it may be tied directly to ground) at RESET, the ROM is disabled.
SCL2	I/O	**Serial Data Clock 2:** This pin is used with RA15 to mechanize the second I^2C port. This is the clock pin; RA15 is the data pin.

[a] HSYNC and VSYNC are also listed in Table 2-6.

2.3 Rambus® Pins

The CL-GD5465 has one Rambus channel — Rambus Channel A. The pins for a Rambus Channel B are allocated, but not used on the CL-GD5465.

The Rambus channels must be designed properly for acceptable results. The trace routing, width, and spacing are all very important. Refer to Appendix B1, "Layout Guidelines" for Rambus channel design information.

2.3.1 Rambus® Channel A

Table 2-4. Rambus® Channel A Pins

Name	Type	Description
RAD[8:0]	I/O	**Rambus A Data [8:0]:** This is the bidirectional data bus for Rambus Channel A. These are low-swing signals as defined in the Rambus electrical specifications.
RARCLK	O	**Rambus A Receive Clock:** Data to the RDRAMs (request and write data packets) are aligned to this clock. This clock is used by the RDRAM to sample data it receives from the CL-GD5465.
RATCLK	I	**Rambus A Transmit Clock:** Data from the RDRAMs (read data and acknowledge packets) are aligned to this clock. This clock is transmitted by the RDRAM along with the data and used by the CL-GD5465 to sample the data from the RDRAM.
RACTE1	O	**Rambus A ClockToEnd 1:** This pin is driven by the CL-GD5465 to the end of the memory expansion module.
RACTE0	O	**Rambus A ClockToEnd 0:** This pin is driven by the CL-GD5465 to the end of the main Rambus channel.
RAC	I/O	**Rambus A Control:** This bidirectional pin is used to frame packets, transmit part of the Rambus operation code, and terminate transactions prematurely on Rambus Channel A. This is a low-swing signal as defined in the Rambus electrical specifications.
RAE	O	**Rambus A Enable:** This output resets or enables the RDRAMs for Rambus Channel A. This is a low-swing signal as defined in the Rambus electrical specifications.
RAVREF	I	**Rambus A Voltage Reference:** This is the logic threshold voltage for low-swing signals for Rambus Channel A.
CCTL	I/O	**Rambus Current Control Program:** This pin is used for the calibration of the RAC output current drivers for both channels. A resistor approximately the value of 1/2 R_{TERM} must be connected between this pin and V_{TERM}.

2.3.2 Rambus® Channel B

The Rambus Channel B pins are not implemented on the CL-GD5465 and are not internally connected to the pins (except SOUT, pin 174), but are reserved for future Laguna family members.

Table 2-5. Rambus® Channel B Pins

Name	Type	Description
RBD[8:0]	I/O	**Rambus B Data [8:0]:** This is the bidirectional data bus for Rambus Channel B. These are low-swing signals as defined in the Rambus electrical specifications.
RBRCLK	O	**Rambus B Receive Clock:** Data to the RDRAMs (request and write data packets) are aligned to this clock. This clock is used by the RDRAM to sample data it receives from the CL-GD5465.
RBTCLK	I	**Rambus B Transmit Clock:** Data from the RDRAMs (read data and acknowledge packets) are aligned to this clock. This clock is transmitted by the RDRAM along with the data and used by the CL-GD5465 to sample the data from the RDRAM.
RBCTE1	O	**Rambus B ClockToEnd 1:** This pin is driven by the CL-GD5465 to the end of the memory expansion module.
RBCTE0	O	**Rambus B ClockToEnd 0:** This pin is driven by the CL-GD5465 to the end of the main Rambus channel.
RBC	I/O	**Rambus B Control:** This bidirectional pin is used to frame packets, transmit part of the Rambus operation code, and terminate transactions prematurely and Rambus Channel B. This is a low-swing signal as defined in the Rambus electrical specifications.
RBE	O	**Rambus B Enable:** This output is used to reset or enable the RDRAMs for Rambus Channel B. This is a low-swing signal as defined in the Rambus electrical specifications.
RBVREF	I	**Rambus B Voltage Reference:** This is the logic threshold voltage for low-swing signals for Rambus Channel B.
SOUT	O	**Rambus Serial Output:** This output initializes the RDRAMs in both Rambus channels. It is used in performing refresh when the RDRAMs are in Power Down mode (this feature is not implemented in the CL-GD5465). This pin is not 5-V tolerant, see Section 6.2 for additional information.

2.4 Monitor Pins

Table 2-6. Monitor Pins

Name	Type	Description
RED	O	**Analog Red Video:** This analog output supplies current corresponding to the red value of the pixel being sent to the monitor. Each DAC output is typically terminated to monitor ground with a 75-Ω, 2-percent resistor. This resistor, in parallel with the 75-Ω resistor in the monitor, yields a 37.5-Ω impedance to ground.
GREEN	O	**Analog Green Video:** This analog output supplies current corresponding to the green value of the pixel being sent to the monitor. See the description of RED for information regarding the termination of this pin.
BLUE	O	**Analog Blue Video:** This analog output supplies current corresponding to the blue value of the pixel being sent to the monitor. See the description of RED for information regarding the termination of this pin.
RSET	I	**DAC Current Set:** A resistor from this pin to DACVSS sets the full-scale current output of the DACs. The value of this resistor is typically 135 Ω. The following equation is derived in Appendix B5, "Signature Generator". $RSET = \frac{2.52\ V \bullet Load}{VFullScale}$ **Equation 2-1**
IREF	I	**DAC Current Reference:** This pin is connected to a 0.1-µF capacitor that is returned to AVDD. This capacitor stabilizes the internal DAC current reference.
HSYNC	I/O	**Horizontal Sync:** This output supplies the horizontal synchronization signal to the monitor. The polarity of this output is programmable. This pin is put into high-impedance when ESYNC# is low.
VSYNC	I/O	**Vertical Sync:** This output supplies the vertical synchronization signal to the monitor. The polarity of this output is programmable. This pin is put into high-impedance when ESYNC# is low.
SCL	I/O	**Serial Clock:** This is the clock pin of the first I^2C port.
SDA	I/O	**Serial Data:** This is the data pin of the first I^2C port.

2.5 TV Output Pins

Table 2-7. TV Output Pins

Name	Type	Description
EVCLK	O	**Encoder Video Clock:** This output clocks the encoder video. This is a 2× clock.
EV[7:0]	I/O	**Encoder Video:** This bus supplies the video to the TV encoder. If a pull-down resistor is installed on RA1, these pins are redefined as the feature connector pixel bus. In this case, the CL-GD5465 cannot supply encoder video.
EVSYNC	I	**Encoder Vertical Sync**: This pin is the vertical sync from the TV encoder.

2.6 Boundary Scan Pins

Table 2-8. Boundary Scan Pins

Name	Type	Description
TDI	I	**Test Data In:** This active-low input puts all pins into high-impedance without resetting the device.
TMS	I	**Test Master Control:** This active-low input enables Pin Scan mode.
TCLK	I	**Test Clock:** This is the IEEE 1149.1 test clock input.
TDO	O	**Test Data Out:** This is the IEEE 1149.1 test data output.

2.7 Clock Pins

Table 2-9. Clock Pins

Name	Type	Description
XTAL0 (RCLK)	I	**Reference Crystal Pin 0:** This pin can be tied to one side of the 14.31818-MHz crystal if the on-chip oscillator is used. If an external reference is used, it is injected on this pin.
XTAL1	O	**Reference Crystal Pin 1:** This pin can be tied to one side of the 14.31818-MHz crystal if the on-chip oscillator is used. If an external reference is used, this pin must be a no-connect.

2.8 Power and Ground Pins

Table 2-10. Power and Ground Pins

Name	Type	Description
VDD[6:1]	PWR	**Digital Power [6:1]:** These six pins supply power to the digital core and I/O logic. Each pin must be connected to the 3.3-V power plane and bypassed to GND with a 0.1-µF capacitor placed as close to the pin as possible.
VDDQ[5, 3:1]	PWR	**Digital AGP Power [5, 3:1]:** The AGP specification specifies that these pins must be isolated from the logic power supply on the board and the chip. Each pin must be connected to the isolated 3.3-V power plane and bypassed to GND with a 0.1-µF capacitor placed as close to the pin as possible.
RAVDD[3:1]	PWR	**Rambus A Digital Power [3:1]:** These three pins supply power for the Rambus Channel A digital logic. Each pin must be bypassed to RAGND.
RAAVDD	PWR	**Rambus A Analog Power:** This pin supplies analog power to Rambus Channel A. This pin must be bypassed to RAAGND with a 10-µF capacitor in parallel with a 0.1-µF capacitor.
RBVDD[3:1]	PWR	**Rambus B Digital Power [3:1]:** These three pins supply power for the Rambus Channel B digital logic. Each pin must be bypassed to RBGND with a 10-µF capacitor in parallel with a 0.1-µF capacitor.
RBAVDD	PWR	**Rambus B Analog Power:** This pin supplies analog power to Rambus Channel B. This pin must be bypassed to RBAGND with a 10-µF capacitor in parallel with a 0.1-µF capacitor.

Table 2-10. Power and Ground Pins *(cont.)*

Name	Type	Description
XVDD	PWR	**Reference Oscillator Power:** This pin supplies power to the reference oscillator and Rambus BCLK synthesizer (common to both channels). This pin must be bypassed to XGND.
PVDD	PWR	**PCLK Synthesizer Power:** This pin supplies power to the pixel clock synthesizer. This pin must be bypassed to PGND.
AVDD[2:1]	PWR	**DAC Power [2:1]:** These two pins supply power to the integrated DACs. Each pin must be connected to the 3.3-V power plane and bypassed to DACGND with a 0.1-µF capacitor placed as close to the pin as possible.
GND[10:1]	GND	**Digital Ground [10:1]:** These 10 pins supply ground reference to the digital core, AGP, and I/O logic. Each pin must be connected to the ground plane.
RAGND[7:1]	GND	**Rambus A Digital Ground [7:1]:** These seven pins supply ground reference to the Rambus Channel A digital logic.
RAAGND	GND	**Rambus A Analog Ground:** This pin supplies analog ground to Rambus Channel A.
RACGND	GND	**Rambus A ClockToEnd Ground:** This pin supplies ground to the Rambus Channel A RACTE drivers.
RBGND[7:1]	GND	**Rambus B Digital Ground [7:1]:** These seven pins supply ground reference to the Rambus Channel B digital logic.
RBAGND	GND	**Rambus B Analog Ground:** This pin supplies analog ground to Rambus Channel B.
RBCGND	GND	**Rambus B ClockToEnd Ground:** This pin supplies ground to the Rambus Channel A RACTE drivers.
XGND	GND	**Reference Oscillator Ground:** This pin supplies ground reference to the reference oscillator and Rambus BCLK synthesizer (common to both channels).
PGND	GND	**PCLK Synthesizer Ground:** This pin supplies ground reference to the pixel clock synthesizer.
AGND[2:1]	GND	**DAC Ground [2:1]:** These two pins supply ground reference to the integrated DACs. Each pin must be connected to the DAC on the ground plane.

3. FUNCTIONAL DESCRIPTION

3.1 General

The CL-GD5465 integrates all the necessary hardware for a flexible multimedia display system, including an integrated palette DAC, clock generators, Enhanced V-Port bus for easy expandability, glueless AGP/PCI host interface, glueless Rambus channels, and a 64-bit graphics engine featuring standard GUI acceleration hardware (such as BitBLT, color expansion, 3D engine, and hardware cursor). The CL-GD5465 also offers advanced features such as stretch BitBLT and line acceleration, a general-purpose I/O port for expansion, front-end and back-end video playback scaling, and color-space conversion for video applications.

Figure 3-1 shows the CL-GD5465 connection to the host, monitor, and memory.

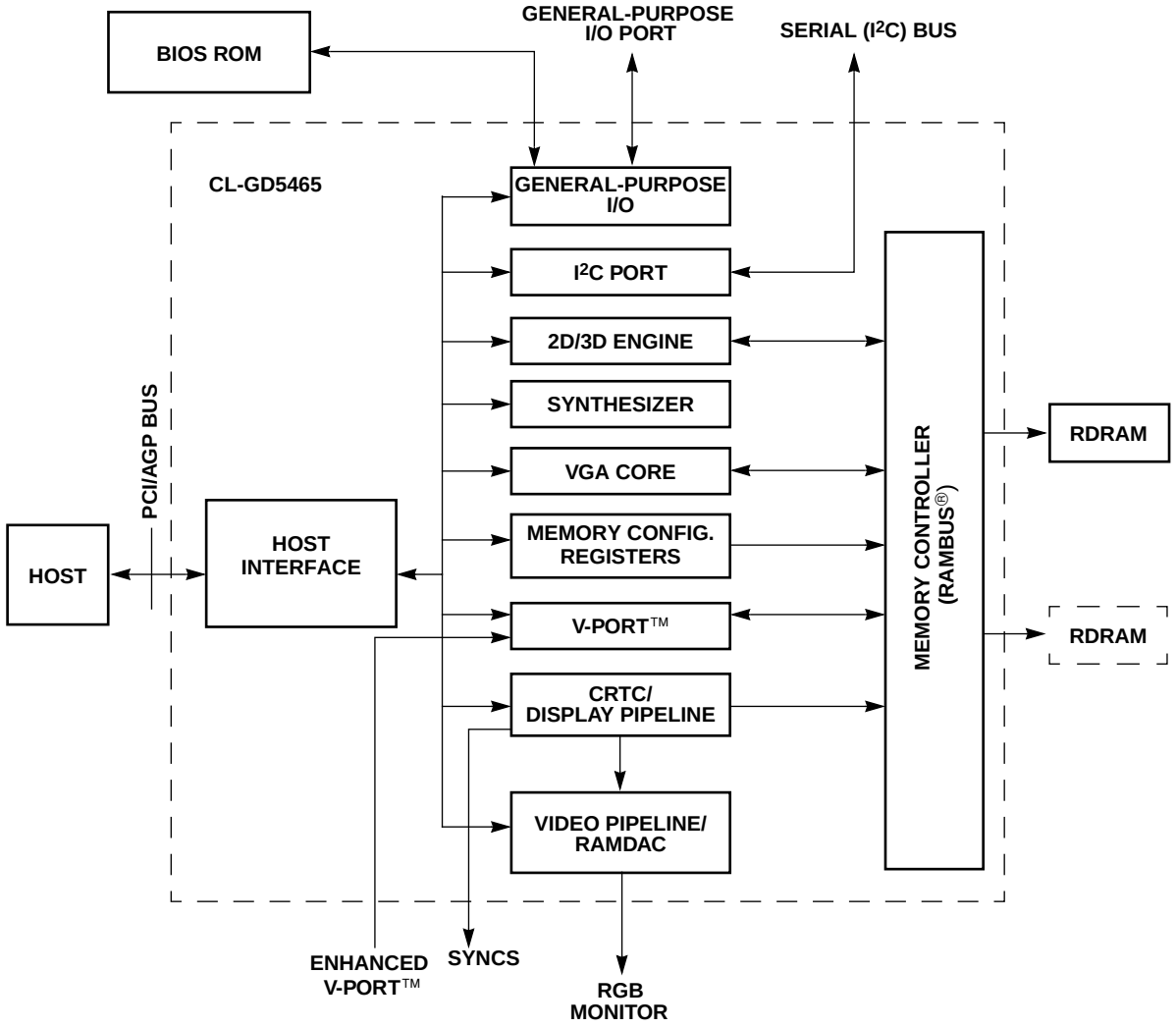


Figure 3-1. CL-GD5465 Block Diagram

The CL-GD5465 is a high-performance VisualMedia solution based on the latest Rambus technology. The CL-GD5465 uses one of two Rambus channels providing 500 to 600 Mbytes/second of memory bandwidth, displaying true-color images at up to 1024 × 768 resolution, and 256-color modes that can reach a maximum of 1600 × 1200 resolution.

3.2 Functional Blocks

The following sections describe the functional blocks that are integrated into the CL-GD5465.

3.2.1 Host Interface

The CL-GD5465 host interface offers AGP v1.0/PCI v2.1-compliant zero-wait-state burst write support up to 66 MHz, and meets single electrical load requirements by buffering the BIOS ROM and local peripheral bus. In addition, the CL-GD5465 supports AGP. The CL-GD5465 host interface implements byte-swapping on a word or dword basis for bi-endian support. There is no need for external glue logic because the CL-GD5465 host interface decodes all 32 bits of address space. It also incorporates an eight-level command/data buffer that improves host throughput by releasing the CPU as soon as the command or data is written into the buffer.

The CL-GD5465 performs as a bus master to fetch instructions and parameters for the 3D engine and allow texture, depth, and color data to be stored in system memory. Bus master accesses offer zero-wait-state read burst and write burst support for efficient use of the AGP and PCI buses.

3.2.2 2D Graphics Engine

The 2D graphics engine in the CL-GD5465 is an advanced 64-bit, three operand engine that accelerates BitBLTs as well as line draws, polygon draw, and polygon fill. The 2D engine is a fast single-cycle 85-MHz engine, matching the 600 Mbytes/sec. Rambus data speed that provides 8 bits of data every 1.5 ns (64 bits of data every 12 ns). This provides more than twice the bandwidth of most other graphics engines that require 32 ns to process 64 bits of data.

There is also hardware support in the 2D engine for monochrome-to-color expansion in 8-, 16-, 24-, and 32-bpp modes. The CL-GD5465 2D engine performs video scaling with a stretch BitBLT feature that takes off-screen video or bit map data and scales it before placing it in on-screen memory. The data can be overlayed with video using color key or chroma key compares. This allows the on-screen memory to contain a homogeneous image. The CL-GD5465 supports YUV-to-RGB color-space conversion during the stretch.

The 2D engine incorporates a 25-entry command and data queue to further improve throughput by releasing both the host CPU and the CL-GD5465 host interface as soon as the command or data is recorded.

3.2.3 3D Graphics Engine

The 3D graphics engine incorporated in the CL-GD5465 can draw randomly oriented triangles with Gouraud shading, texture mapping, alpha blending, and Z-buffering. The CL-GD5465 has support for copy, DECAL, and blended 2D/3D and modulated textures as well as bilinear, bilinear mipmapped, and trilinear textures. The 3D graphics engine uses AGP/PCI bus mastering to fetch instructions and parameters from system memory to render scenes with a minimum of host intervention.

3.2.4 Memory Controller (Rambus®)

The unique CL-GD5465 memory controller is the gateway to the Rambus interface, offering up to 600 Mbytes per second bandwidth per channel. It efficiently allocates the memory bandwidth among the functions: CPU access, DRAM refresh, screen refresh, 2D/3D engine operations, and the Enhanced V-Port access. The CL-GD5465 memory controller is designed to manage a single Rambus channel; however, some future members of the Laguna family will take full advantage of both Rambus channels.

3.2.5 VGA Core

The CL-GD5465 VGA core is an independent unit that shares the memory bus and host interface with the other components of the CL-GD5465. It is enabled only during VGA modes and is totally com-

patible with the IBM VGA standard, supporting video modes 0h through 13h. A strapping option disables the VGA core, allowing operation as a grayscale controller.

3.2.6 V-Port™

The CL-GD5465 writes realtime recorded video from a decoder to the frame buffer, typically for display in the video window. Video can be decimated vertically, horizontally, and temporally. When video is being captured, the capture and display buffers can be swapped automatically as each frame is captured. This prevents the display of partial frames with no host intervention.

The V-Port hardware interface uses the same pins as the VGA pass-through connector. It can be configured for either sense of HREF.

3.2.7 RAMDAC

The CL-GD5465 RAMDAC contains the LUT (lookup table) as well as the true color digital-to-analog converter. The CL-GD5465 RAMDAC supports 8-bpp LUT mode and Direct Data modes for 8-, 16-, and 24-bpp, along with Alpha channel support in 32-bpp modes. The color values in the LUT can be individually addressed, providing for gamma correction.

3.2.8 Video Pipeline

The CL-GD5465 features a programmable hardware window for the simultaneous display of graphics and video streams. The graphics and video formats can have different color spaces and even pixel sizes. The display of 8-bpp palettized graphics with YUV 4:2:2 video is a typical application.

The window can be independently zoomed in both dimensions up to 4×. Both horizontal and vertical zooming are always done with interpolation of 'in between' pixels.

Occlusion support allows the graphics and video streams to be mixed on a pixel-by-pixel basis. Color key matching of the graphics source or chroma key matching of the video source can be used to determine which pixels are replaced.

3.2.9 Programmable Frequency Synthesizer

There are two programmable frequency synthesizers integrated into the CL-GD5465. One synthesizer generates the Rambus clock (300-MHz nominal frequency), and the other synthesizer generates the video clock and CRT controller timing reference (up to 230 MHz). The CL-GD5465 includes an on-chip reference oscillator that requires only an inexpensive two-pin 14.31818-MHz crystal.

3.2.10 CRT Controller

The CL-GD5465 CRTC (CRT controller) handles all screen-refresh activity and generates monitor timing signals (HSYNC and VSYNC) and BLANK#. It coordinates the fetching of data from the display memory and delivering it to the DACs for screen refresh. The CRTC also controls the hardware cursor.

3.2.11 I^2C Ports

The CL-GD5465 offers two I^2C interfaces. One is connected to the monitor, supporting VESA® DDC levels 2B. The other is connected to VMI interface, to control a TV tuner or MPEG decoder.

3.2.12 VMI v1.4

The VMI (video module interface) v1.4 consists of the V-Port and an 8-bit general-purpose I/O port. The V-Port accepts video data from a TV or MPEG decoder and writes it into the frame buffer for subsequent display. The general-purpose I/O port translates the PCI bus into an 8-bit I/O bus that can be configured for either ISA-style or Motorola-style commands.

3.3 Functional Operation

The following sections discuss the seven major operations handled by the CL-GD5465.

3.3.1 2D Graphics Engine

The CL-GD5465 host accesses the registers within the 2D graphics engine to program the desired function. The host interface buffers the operation parameters in its command buffers, releasing the CPU to continue other tasks. To relieve traffic congestion on internal buses, a secondary buffer in the 2D engine also buffers commands and data. When the 2D

engine completes the current operation, the parameters are transferred to the registers from this secondary queue to start the next graphics operation.

3.3.2 3D Graphics

The host CPU constructs display lists containing 3D control and rendering instructions and stores them into host system memory. The CL-GD5465 then fetches the display lists from host system memory by becoming a AGP/PCI bus master and executing them to render the desired scene. The CL-GD5465 has a rich instruction set including rendering primitives such as DRAW_LINE and DRAW_POLYGON; flow-control instructions such as BRANCH, CALL, and RETURN; and animation-support instructions. The CL-GD5465 can provide status in the form of interrupts when it has reached a specified point in the display list.

3.3.3 Display Refresh

The CL-GD5465 CRTC controls and initiates display refresh cycles. The CRTC first fetches the data from the frame buffer by arbitrating for the memory bus. Once the access is granted, as much of a scanline that can fit is fetched and buffered in the display FIFO to be passed to the RAMDAC for display on the monitor. Programmed for a specific display mode, the rate and timing at which display refresh operations occur is controlled by the CRTC. A large display FIFO allows large Rambus transactions, reducing the overhead of memory data fetches and conflicts in the Rambus arbitrator.

3.3.4 Playback and Capture by the V-Port™

The CL-GD5465 has an 8-bit V-Port that allows the display of video overlay. The CL-GD5465 has a data path into the frame buffer, allowing for capture and scaling. Video capture is done by copying video data to an off-screen area. It can then be written to a hard disk. Video scaling is done by fetching the video data from off-screen memory, then scaling/color-space converting and writing the data into the on-screen portion of the frame buffer in actual display size. The CRTC can then fetch the video data to the DAC by the YUV-to-RGB convertor if necessary. Finally, the DAC converts the video data to the analog RGB for direct connection to the monitor.

In the CL-GD5465, video can also be processed as an overlay surface. In this case, the data can be stored off screen and fetched for scaling and color-space conversion, and overlayed onto the graphics data in a non-destructive way. This overlay window can use color keying or chroma keying to allow arbitrary occlusion on a pixel-by-pixel basis.

3.3.5 Playback by the Host Bus

Another alternative to playback video data is using the host bus on the CL-GD5465. To use this alternative, video data must be written to the off-screen frame buffer area. After the video data is in the off-screen portion of the frame buffer, it is used in exactly the same manner as data gathered by the V-Port bus.

3.3.6 I^2C (DDC/External Device Control)

The I^2C ports implemented in the CL-GD5465 are each made up of a generic data line and clock line connected to register bits. The data and clock are controlled by software changes to the register contents, which change the outputs. By using the correct software driver, each I^2C port can be used to send or receive any single-bit data format. VESA DDC level 2B signalling is supported with the CL-GD5465 BIOS. To communicate to other devices, such as a multistandard decoder, special drivers can be written to work with the second I^2C port.

3.3.7 BIOS Read

For compliance with the AGP/PCI single-load specification, the BIOS access must be buffered and accessed with address and data pins. The BIOS ROM is read once during the computer boot process and shadowed in system memory. Once this is complete, the general-purpose I/O port can be used.

3.4 Performance Notes

The CL-GD5465 is designed with the following performance-enhancing features:

- A 64-bit 2D graphics engine with three-operand BitBLT, color expansion for 8-, 16-, 24-, and 32-bpp modes, stretch BitBLT, transparent BitBLT, and linedraw acceleration.

- The CL-GD5464 contains a 3D graphics engine capable of rendering triangles with texture mapping, Gouraud shading, alpha blending, and Z-buffering.
- BitBLT operations stored in a frame buffer display list and triggerable on command or following any scanline of screen refresh.
- Video playback acceleration with bilinear interpolated scaling, three or more occluded video windows simultaneously, and YUV-to-RGB conversion. Frame-rate conversion is done automatically by CL-GD5465 hardware.
- Integrated 230-MHz palette DAC, clock synthesizer, and hardware cursor, supporting non-interlaced resolutions up to 1600 × 1200.
- Rambus® memory architecture allowing up to 600 Mbytes/second bandwidth and a frame buffer up to 8 Mbytes at increments of 1 Mbyte.
- 32-bit configurable host interface compliant with PCI v2.1 and AGP v1.0 standards.
- Memory-mapped registers, linear addressable frame buffer, bi-endian data format support, and 5- or 3.3-V host interface.
- VMI v1.4 support for multimedia expansion.
- VESA® DDC2B-compliant monitor signalling.
- Green PC support with VESA® DPMS and system power down.

3.5 Compatibility

The CL-GD5465 includes all registers and data paths required for VGA controllers, and supports extensions to VGA, including resolutions up to 1024 × 768 × 16.8 million colors non-interlaced. The CL-GD5465 displays true-color images at up to 1024 × 768 resolution, and 256-color modes can reach a maximum of 1600 × 1200 resolution.

3.6 Board Testability

The CL-GD5465 is testable, even when installed on a printed circuit board. By using the pin-scan testing, any IC signal pin not connected to the board or shorted to a neighboring pin or trace is detected. The signature generator allows the entire system, including the display memory, to be tested at operating speed.

4. CONFIGURATION TABLES

4.1 Video Modes

Table 4-1. Standard VGA Video Modes

Mode No.	VESA® No.	No. of Colors	Char. × Row	Char. × Cell	Screen Format	Display Mode	Pixel Freq. MHz	Horiz. Freq. kHz	Vert. Freq. Hz
0, 1	0, 1	16/256K	40 × 25	9 × 16	360 × 400	Text	14	31.5	70
2, 3	2, 3	16/256K	80 × 25	9 × 16	720 × 400	Text	28	31.5	70
4, 5	4, 5	4/256K	40 × 25	8 × 8	320 × 200	Graphics	12.5	31.5	70
6	6	2/256K	80 × 25	8 × 8	640 × 200	Graphics	25	31.5	70
7	7	Monochrome	80 × 25	9 × 16	720 × 400	Text	28	31.5	70
D	D	16/256K	40 × 25	8 × 8	320 × 200	Graphics	12.5	31.5	70
E	E	16/256K	80 × 25	8 × 14	640 × 200	Graphics	25	31.5	70
F	F	Monochrome	80 × 25	8 × 14	640 × 350	Graphics	25	31.5	70
10	10	16/256K	80 × 25	8 × 14	640 × 350	Graphics	25	31.5	70
11	11	2/256K	80 × 30	8 × 16	640 × 480	Graphics	25	31.5	60
11†	11	2/256K	80 × 30	8 × 16	640 × 480	Graphics	31.5	37.5	75
12	12	16/256K	80 × 30	8 × 16	640 × 480	Graphics	25	31.5	60
12[a]	12[a]	16/256K	80 × 30	8 × 16	640 × 480	Graphics	31.5	37.5	75
13	13	256/256K	40 × 25	8 × 8	320 × 200	Graphics	12.5	31.5	70

[a] Higher refresh modes available with generic fix-up TSR.

NOTE: An 8 × 14 font for the EGA modes can be provided with a DOS TSR (terminate and stay resident) program. If the TSR has not been loaded when the mode is set, the 8 × 16 font is used with the two bottom rows deleted. This causes truncation of characters with descenders, but does not restrict program operation. The TSR should be used for absolute compatibility with DOS applications that use the 8 × 14 font.

Table 4-2. Extended Video Modes

Mode No.	VESA® No.	No. of Colors	Char. × Row	Char. × Cell	Screen Format	Display Mode	Pixel Freq. MHz	Horiz. Freq. kHz	Vert. Freq. Hz
5E	100	256/256K	80 × 25	8 × 16	640 × 400	Graphics	25	31.5	70
7A	–	64K	–	–	640 × 400	Graphics	25	31.5	70
5F	101	256/256K	80 × 30	8 × 16	640 × 480	Graphics	25	31.5	60
5F	101	256/256K	80 × 30	8 × 16	640 × 480	Graphics	31.5	37.9	72
5F	101	256/256K	80 × 30	8 × 16	640 × 480	Graphics	31.5	37.5	75
5F	101	256/256K	80 × 30	8 × 16	640 × 480	Graphics	36.0	43.3	85
64	111	64K	–	–	640 × 480	Graphics	25	31.5	60
64	111	64K	–	–	640 × 480	Graphics	31.5	37.9	72
64	111	64K	–	–	640 × 480	Graphics	31.5	37.5	75
64	111	64K	–	–	640 × 480	Graphics	36.0	43.3	85
71	112	16M	–	–	640 × 480	Graphics	25	31.5	60
71	112	16M	–	–	640 × 480	Graphics	31.5	37.9	72
71	112	16M	–	–	640 × 480	Graphics	31.5	37.5	75
71	112	16M	–	–	640 × 480	Graphics	36.0	43.3	85
76#	–	16M+A	–	–	640 × 480	Graphics	25	31.5	60
76#	–	16M+A	–	–	640 × 480	Graphics	31.5	37.9	72
76#	–	16M+A	–	–	640 × 480	Graphics	31.5	37.5	75
76#	–	16M+A	–	–	640 × 480	Graphics	36.0	43.3	85
58, 6A	102	16/256K	100 × 37	8 × 16	800 × 600	Graphics	36	35.2	56
58, 6A	102	16/256K	100 × 37	8 × 16	800 × 600	Graphics	40	37.8	60
58, 6A	102	16/256K	100 × 37	8 × 16	800 × 600	Graphics	50	48.1	72
58, 6A	102	16/256K	100 × 37	8 × 16	800 × 600	Graphics	49.5	46.9	75
58, 6A	102	16/256K	100 × 37	8 × 16	800 × 600	Graphics	56.25	53.7	85.1
5C	103	256/256K	100 × 37	8 × 16	800 × 600	Graphics	36	35.2	56
5C	103	256/256K	100 × 37	8 × 16	800 × 600	Graphics	40	37.9	60
5C	103	256/256K	100 × 37	8 × 16	800 × 600	Graphics	50	48.1	72
5C	103	256/256K	100 × 37	8 × 16	800 × 600	Graphics	49.5	46.9	75
5C	103	256/256K	100 × 37	8 × 16	800 × 600	Graphics	56.25	53.7	85.1
65	114	64K	–	–	800 × 600	Graphics	36	35.2	56
65	114	64K	–	–	800 × 600	Graphics	40	37.8	60

Table 4-2. Extended Video Modes *(cont.)*

Mode No.	VESA® No.	No. of Colors	Char. × Row	Char. × Cell	Screen Format	Display Mode	Pixel Freq. MHz	Horiz. Freq. kHz	Vert. Freq. Hz
65	114	64K	–	–	800 × 600	Graphics	50	48.1	72
65	114	64K	–	–	800 × 600	Graphics	49.5	46.9	75
65	114	64K	–	–	800 × 600	Graphics	56.25	53.7	85.1
78	115	16M	–	–	800 × 600	Graphics	36	35.2	56
78	115	16M	–	–	800 × 600	Graphics	40	37.9	60
78	115	16M	–	–	800 × 600	Graphics	50	48.1	72
78	115	16M	–	–	800 × 600	Graphics	49.5	46.9	75
78	115	16M	–	–	800 × 600	Graphics	56.25	53.7	85.1
72#	–	16M+A	–	–	800 × 600	Graphics	36	35.2	56
72#	–	16M+A	–	–	800 × 600	Graphics	40	37.8	60
72#	–	16M+A	–	–	800 × 600	Graphics	50	48.1	72
72#	–	16M+A	–	–	800 × 600	Graphics	49.5	46.9	75
72#	–	16M+A	–	–	800 × 600	Graphics	56.25	53.7	85.1
5D†	104	16/256K	128 × 48	8 × 16	1024 × 768	Graphics	44.9	35.5	43i†
5D	104	16/256K	128 × 48	8 × 16	1024 × 768	Graphics	65	48.3	60
5D	104	16/256K	128 × 48	8 × 16	1024 × 768	Graphics	75	56	70
5D	104	16/256K	128 × 48	8 × 16	1024 × 768	Graphics	78.7	60	75
5D	104	16/256K	128 × 48	8 × 16	1024 × 768	Graphics	94.5	68.3	85
60†	105	256/256K	128 × 48	8 × 16	1024 × 768	Graphics	44.9	35.5	43i†
60	105	256/256K	128 × 48	8 × 16	1024 × 768	Graphics	65	48.3	60
60	105	256/256K	128 × 48	8 × 16	1024 × 768	Graphics	75	56	70
60	105	256/256K	128 × 48	8 × 16	1024 × 768	Graphics	78.7	60	75
60	105	256/256K	128 × 48	8 × 16	1024 × 768	Graphics	94.5	68.3	85
74†	117	64K	–	–	1024 × 768	Graphics	44.9	35.5	43i†
74	117	64K	–	–	1024 × 768	Graphics	65	48.3	60
74	117	64K	–	–	1024 × 768	Graphics	75	56	70
74	117	64K	–	–	1024 × 768	Graphics	78.7	60	75
74	117	64K	–	–	1024 × 768	Graphics	94.5	68.3	85
79	118	16M	–	–	1024 × 768	Graphics	44.9	35.5	43i†
79	118	16M	–	–	1024 × 768	Graphics	65	48.3	60

Table 4-2. Extended Video Modes *(cont.)*

Mode No.	VESA® No.	No. of Colors	Char. × Row	Char. × Cell	Screen Format	Display Mode	Pixel Freq. MHz	Horiz. Freq. kHz	Vert. Freq. Hz
79	118	16M	–	–	1024 × 768	Graphics	75	56	70
79	118	16M	–	–	1024 × 768	Graphics	78.7	60	75
79	118	16M	–	–	1024 × 768	Graphics	94.5	68.3	85
73#	–	16M+A	–	–	1024 × 768	Graphics	44.9	35.5	43i†
73#	–	16M+A	–	–	1024 × 768	Graphics	65	48.3	60
73#	–	16M+A	–	–	1024 × 768	Graphics	75	56	70
73#	–	16M+A	–	–	1024 × 768	Graphics	78.7	60	75
73#	–	16M+A	–	–	1024 × 768	Graphics	94.5	68.3	85
6C†	106	16/256K	160 × 64	8 × 16	1280 × 1024	Graphics	75	48	43i
6C	106	16/256K	160 × 64	8 × 16	1280 × 1024	Graphics	108	65	60
6C	106	16/256K	160 × 64	8 × 16	1280 × 1024	Graphics	126	76	71.2
6C	106	16/256K	160 × 64	8 × 16	1280 × 1024	Graphics	135	80	75
6C	106	16/256K	160 × 64	8 × 16	1280 × 1024	Graphics	157	91.1	85
6D†	–	256/256K	160 × 64	8 × 16	1280 × 1024	Graphics	75	48	43i
6D	–	256/256K	160 × 64	8 × 16	1280 × 1024	Graphics	108	65	60
6D	–	256/256K	160 × 64	8 × 16	1280 × 1024	Graphics	126	76	71.2
6D	–	256/256K	160 × 64	8 × 16	1280 × 1024	Graphics	135	80	75
6D	–	256/256K	160 × 64	8 × 16	1280 × 1024	Graphics	157	91.1	85
75	11A	64K	–	–	1280 × 1024	Graphics	75	48	43i†
75	11A	64K	–	–	1280 × 1024	Graphics	108	65	60
75	11A	64K	–	–	1280 × 1024	Graphics	126	76	71.2
75	11A	64K	–	–	1280 × 1024	Graphics	135	80	75
75	11A	64K	–	–	1280 × 1024	Graphics	157	91.1	85
7B	–	256/256K	200 × 75	8 × 16	1600 × 1200	Graphics	135	62.5	48i†
7B	–	256/256K	200 × 75	8 × 16	1600 × 1200	Graphics	162	75	60

NOTES:

1) '†' character indicates interlaced mode.
2) '#' character indicates 16M colors, but with 32-bit-per-pixel format.
3) '+A' indicates 16M colors + Alpha channel.
4) Some modes are not supported by all releases of the CL-GD5465 BIOS. Refer to the *CL-GD5465 Software Release Kit* for the list of video modes supported by the CL-GD5465 BIOS.

5) Some modes are not supported by all monitors. The fastest vertical refresh rate for the monitor type selected is automatically used.

6) An 8 × 14 font for mode 55h is provided with a DOS TSR. If the TSR has not been loaded when the mode is set, the 8 × 16 font is used with the two bottom rows deleted. This causes truncation of characters with descenders, but does not restrict program operation nor does it make characters particularly difficult to read. For absolute compatibility with some DOS applications that use the 8 × 14 font, the TSR should be used.

The DAC operating frequencies allow the CL-GD5465 to achieve the refresh rates indicated in Table 4-3. The Cirrus Logic BIOS supports the refresh rates noted in Table 4-2.

Table 4-3. Maximum Refresh Rates

Resolution	170-MHz DAC	230-MHz DAC
1024 × 768	100+ Hz	100+ Hz
1280 × 1024	85 Hz	100+ Hz
1600 × 1200	60 Hz	85 Hz

4.2 Power-Up Configuration

On the rising edge of RST#, the CL-GD5465 samples the levels on certain pins. These levels are stored in a group of latches that establish fundamental operating characteristics of the device, such as host bus type. Software can determine the configuration options by reading PCI configuration register ECh (PCIEC).

These pins are pulled up with internal 250-kΩ pull-up resistors; the default configuration is ‘1’. A ‘0’ is selected by installing an external 6.8-kΩ pull-down resistor on the corresponding pin (or by connecting the pin directly to ground if appropriate). Table 4-4 summarizes the Configuration bits and their functions..

Table 4-4. CL-GD5465 Configuration Bits

Pin Name	Pin No.	Level	Description	PCIEC	Additional Readback
INTA#	200	1	Request INTA#	INT_EN (26)	PCI interrupt line
		0	Do not request INTA#, disable PCI Interrupt Line register		
ROMCS#	75	1	Enable ROM decode	ROM_EN (25)	PCI ROM base address
		0	Disable ROM decode and PCI Adapter ROM Base Address register		
SOUT	174	1	Normal RAC operation	RAC_BYPASS (24)	–
		0	RAC Bypass mode (for ATE test)		
RA15	128	1	RCLK pin operates normally	RCLK_ATE (15)	–
		0	RCLK pin drives SYSCLK directly		
RA14	127	1		Reserved (14)	–
		0			

Table 4-4. CL-GD5465 Configuration Bits *(cont.)*

Pin Name	Pin No.	Level	Description	PCIEC	Additional Readback
RA13	125	1		Reserved (13)	–
		0			
RA12	124	1		Reserved (12)	–
		0			
RA11	123	1		Reserved (11)	–
		0			
RA10	122	1		Reserved (10)	–
		0			
RA9	120	1		Reserved (9)	–
		0			
RA8	119	1		Reserved [8]	–
		0			
RA7	118	1		Reserved [7]	–
		0			
RA6 RA5 RA4	117 116 115	111	AGP, no sideband, 66 MHz	AGP_CFG [6:4]	–
		110	AGP, no sideband, 133 MHz		
		101	PCI 33 MHz (fast DEVSEL# speed)		
		100	PCI 66 MHz (medium DEVSEL# speed)		
		011	Reserved		
		010	Reserved		
		001	Reserved		
		000	Reserved		
RA3 RA2	114 113	11	VMI host interface disabled	VMI_MODE [3:2]	VMI Mode register
		10	VMI host interface disabled		
		01	VMI host interface Mode A		
		00	VMI host interface Mode B		
RA1	112	1	Put feature connector data on RA [14:7]	FC_SEL [1]	–
		0	Put feature connector data on EV [7:0]		
RA0	111	1	Enable feature connector at reset	FC_EN [0]	–
		0	Disable feature connector at reset		
RD7	109	1	Enable VGA operation	VGA_EN [23]	PCI Subclass [7]
		0	Disable VGA operation		

Table 4-4. CL-GD5465 Configuration Bits *(cont.)*

Pin Name	Pin No.	Level	Description	PCIEC	Additional Readback
RD6	107	1	Enable 64K ROM decode[a]	64KROM [22]	PCI Expansion ROM Base Address 15
		0	Disable 64K ROM decode (32K only)		
RD5	106	1	SCL2 pin operates normally	DCLK_ATE [21]	–
		0	SCL2 pin drives internal video clock (VCLK) directly (for ATE)		
RD4	104	1	V-Port data comes in on RA [14:7]	VPORT_DATA_SRC [20]	–
		0	V-Port data comes in TV [7:0] (test only)		
RD3	103	1	TV-Out devices is not attached	TV_PRESENT_N [19]	PV1_STATUS [0]
		0	TV-Out device is attached		
RD2	102	1	TV-Out device is NTSC	TV_NTSC [18]	–
		0	TV-Out device is PAL		
RD1	101	1	V-Port device is not attached	V-PORT_ PRESENT_N [17]	PV0_STATUS [0]
		0	V-Port device is attached		
RD0	100	1	Select PCI pad characteristics	PCI_PAD MODE [16]	–
		0	Select AGP pad characteristics		

[a] For Revision AA and AB of the CL-GD5465, the functions of RD6 and RA15 are swapped. Revision AC and later will function as described.

5. VGA REGISTER I/O MAP

Table 5-1. VGA Register Port Map

Address	Port
3B4	CRT Controller Index (read/write — monochrome)
3B5	CRT Controller Data (read/write — monochrome)
3BA	Feature Control (write), Input Status Register 1 (read — monochrome)
3C0	Attribute Controller Index/Data (write)
3C1	Attribute Controller Index/Data (read)
3C2	Miscellaneous Output (write), Input Status Register 0 (read)
3C4	Sequencer Index (read/write)
3C5	Sequencer Data (read/write)
3C6	Video DAC Pixel Mask (write only)
3C7	Pixel Address Read Mode (write), DAC State (read)
3C8	Pixel Address Write Mode (write only)
3C9	Pixel Data (read/write)
3CA	Feature Control Readback (read)
3CC	Miscellaneous Output Readback (read)
3CE	Graphics Controller Index (read/write)
3CF	Graphics Controller Data (read/write)
3D4	CRT Controller Index (read/write — color)
3D5	CRT Controller Data (read/write — color)
3DA	Feature Control (write), Input Status Register 1 (read — color)

6. ELECTRICAL SPECIFICATIONS

6.1 Absolute Maximum Ratings

Maximum case temperature under bias ..... 85°C
Storage temperature .....–65°C to 150°C
Voltage on any pin .....GND – 0.5 V to V_{DD} + 0.5 V (volt)
Voltage on 5-V tolerant pin ..... GND – 0.5 V to 5.5 V
Operating power dissipation .....2.0 W (watt)
Power supply voltage .....5.0 V
Injection current (latch-up testing) .....100 mA

CAUTION: Stresses above those listed may cause permanent damage to system components. These are stress ratings only. Functional operation at these or any conditions above those indicated in the operational ratings of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect system reliability.

6.2 DC Specifications

(V_{DD} = 3.3 V ± 0.15 V, T_C = 0°C to 85°C, unless otherwise specified)

Symbol	Parameter	MIN	MAX	Units	Test Conditions	Note
V_{DD} (+3.3 V)	Power supply voltage	3.15	3.45	V	Normal operation	
V_{IL}	Input low voltage	–0.5	0.3 V_{DD}	V	(non 5-V tolerant)	
V_{IH}	Input high voltage	0.7 V_{DD}	1.05 V_{DD}	V	(non 5-V tolerant)	
V_{IH5T}	Input high voltage	0.7 V_{DD}	5.5V	V	(5-V tolerant)	1
V_{OL}	Output low voltage	–	0.1 V_{DD}	V	I_{OL} = 3.2 mA	2
V_{OH}	Output high voltage	0.9 V_{DD}	–	V	I_{OH} = –200 µA	3
I_{DD} (+3.3 V)	Supply current	–	–	–	V_{DD} nominal	4
I_{IH}	Input high current	–	10	µA	V_{IL} = V_{DD}	
I_{IL}	Input low current	–10	–	µA	V_{DD} = 3.45, V_{IL} = 0	
I_{IHP}	Input high current (pull-up)	–	–10	µA	V_{IL} = V_{DD}	
I_{ILP}	Input low current (pull-up)	–45	–12	µA	V_{DD} = 3.45, V_{IL} = 0	
I_{OZ}	Input leakage	–10	10	µA	0 < V_{IN} < V_{CC}	
C_{IN}	Input capacitance	–	10	pF	–	5
C_{OUT}	Output capacitance	–	10	pF	–	5

NOTES:

1) 5-V tolerant pins — all except Rambus access channel, SOUT, and ROMCS#.
2) I_{OL} is specified for a standard buffer. See Section 1.2 for further information.
3) I_{OH} is specified for a standard buffer. See Section 1.2 for further information.
4) I_{DD} is measured with PCLK and BCLK as indicated below:

PCLK	BCLK	I_{DD} (+3.3 V)
230 MHz	300 MHz	850 mA

5) This is not 100% tested, but is periodically sampled.

6.3 DAC Characteristics

(V_{CC} = 3.3 V ± 0.15 V, T_C = 0°C to 85°C, unless otherwise specified)

Symbol	Parameter		MAX	Units	Test Conditions	Note
R	Resolution		8	Bits		
IO	Output current		30	mA	VO < 1 V	
TR	Analog output rise/fall time		3	ns		1, 2, 3
TS	Analog output settling time		15	ns		1, 2, 4
TSK	Analog output skew		tbd	ns		1, 2, 5
FDT	DAC-to-DAC correlation		2.5	%		5, 6
GI	Glitch impulse	Typical	tbd	pV – sec.		1, 2, 5
IL	Integral linearity		1.5	LSB		
DL	Differential linearity		1.5	LSB		1

NOTES:

1) Load is 37.5 Ω and 30 pF per analog output.
2) 130-Ω resistor to DACVSS on VREF pin.
3) TR is measured from 10% to 90% full-scale.
4) TS is measured from 50% of full-scale transition to output remaining within 2% of final value.
5) Outputs loaded identically.
6) About the midpoint of the distribution of the three DACs measured at full-scale output.
7) ‘tbd’ indicates values that are to be determined.

6.4 List of Timings

Table 6-1. PCI Bus Timing

Symbol	Parameter	MIN	MAX	Units
t_1	CLK period	30	–	ns
t_2	High period (CLK) PCI bus	40	60	% of t_1
t_3	CLK to signal valid delay — bused signals	2	11	ns
t_3	CLK to signal valid delay — point to point	2	12	ns
t_4	CLK to active delay	2	–	ns
t_5	CLK to float delay	7	–	ns
t_6	Input setup time to CLK — bused signals	7	–	ns
t_6	Input setup time to CLK — GNT#	10	–	ns
t_7	Input hold time from CLK	0	–	ns

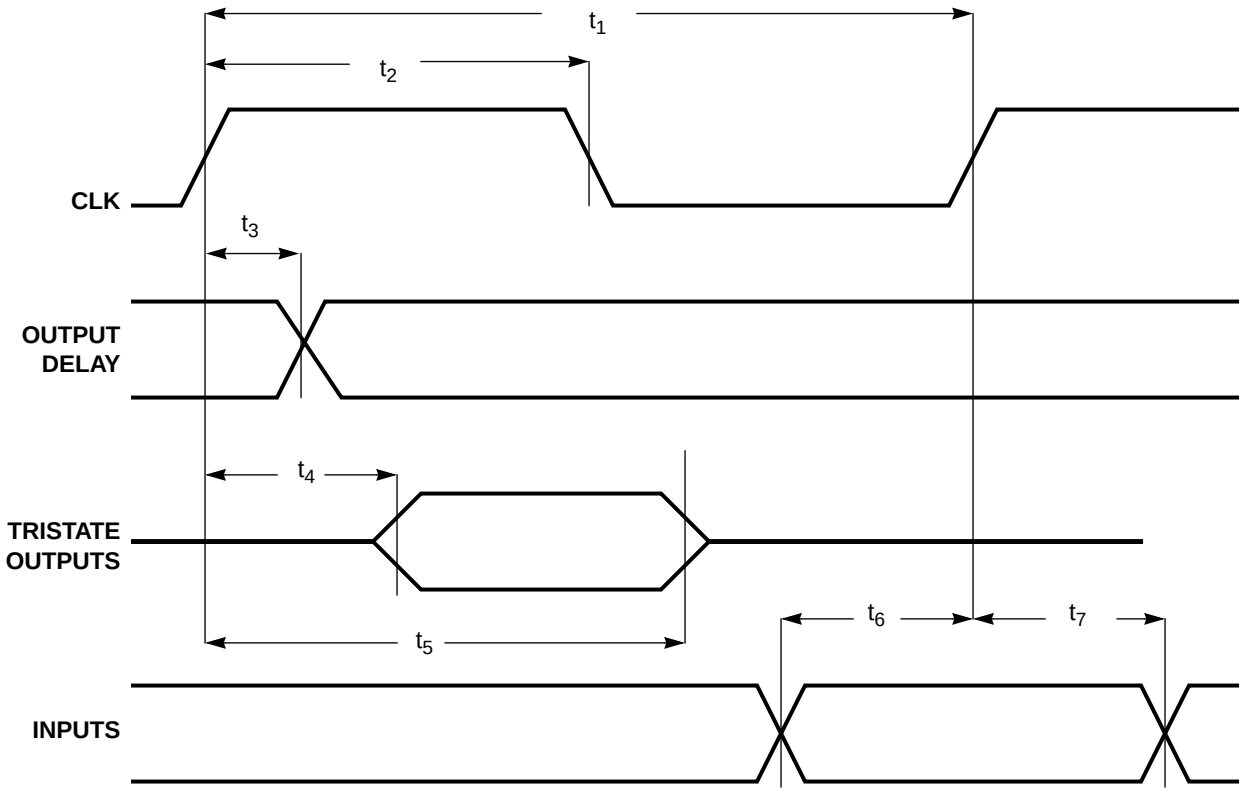


Figure 6-1. PCI Bus Timing

Table 6-2. AGP Bus Timing

Symbol	Parameter	MIN	MAX	Units
t_1	CLK period	15	30	ns
t_2	High period (CLK) PCI bus	6	–	ns
t_3	CLK to signal valid delay	1.5	6	ns
t_4	CLK to active delay	1.5	6	ns
t_5	CLK to float delay	1	14	ns
t_6	Input setup time to CLK	5	–	ns
t_7	Input hold time from CLK	0.5	–	ns

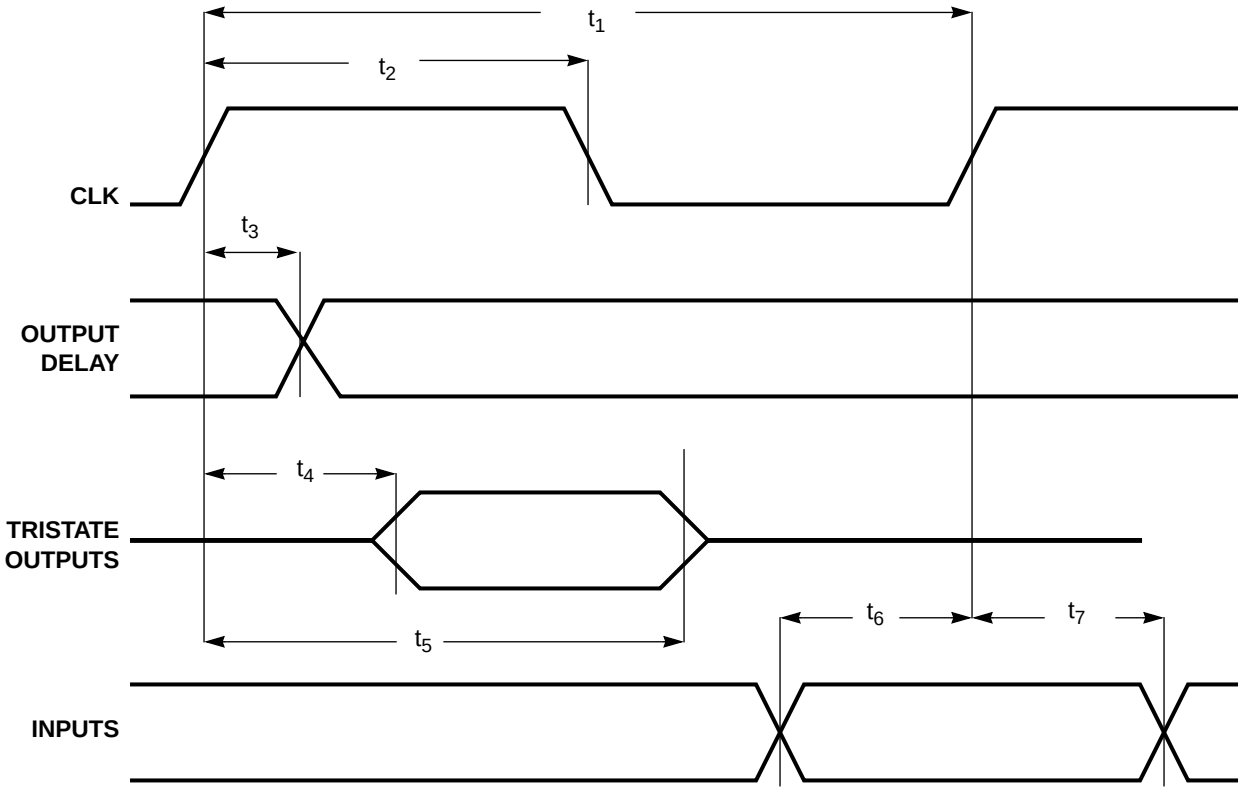


Figure 6-2. AGP Bus Timing

Table 6-3. Rambus® Timing

Symbol	Parameter	MIN	Nominal	MAX	Units
t_1	BCLK period	–	3.33	–	ns
t_2	BCLK pulse width high	0.45	0.5	0.55	t_1
t_3	BCLK pulse width low	0.45	0.5	0.55	t_1
t_4	Data, control setup to RATCLK, RBTCLK	0.3	–	–	ns
t_5	Data, control hold from RATCLK, RBTCLK	0.3	–	–	ns
t_6	RARCLK, RBRCLK to data, control invalid (t_Q MIN)	$0.25 \times t_1 - 0.3$	–	–	ns
t_7	RARCLK, RBRCLK to data, control valid (t_Q MAX)	–	–	$0.25 \times t_1 + 0.3$	ns

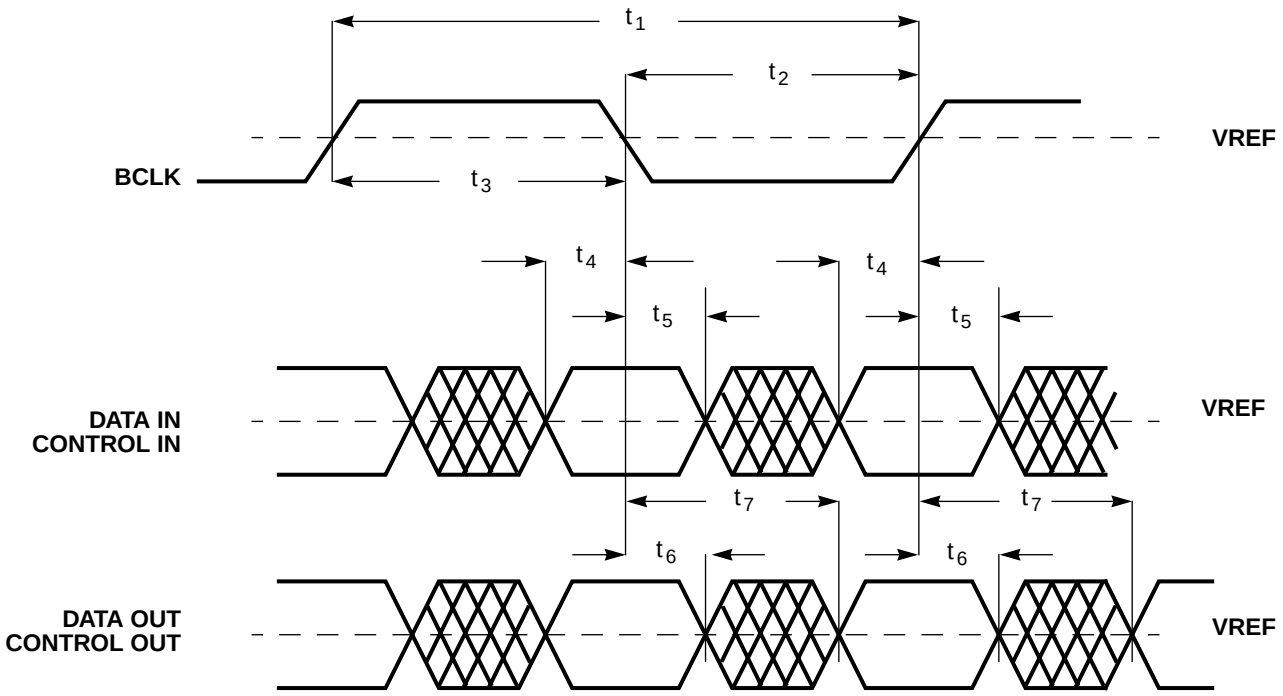


Figure 6-3. Rambus® Timing

Table 6-4. Feature Connector Input

Symbol	Parameter	MIN	MAX	Units
t_1	P[7:0], BLANK# setup to DCLK	0	–	ns
t_2	P[7:0], BLANK# hold from DCLK	6	–	ns

NOTE: Laguna RAMDAC driven externally.

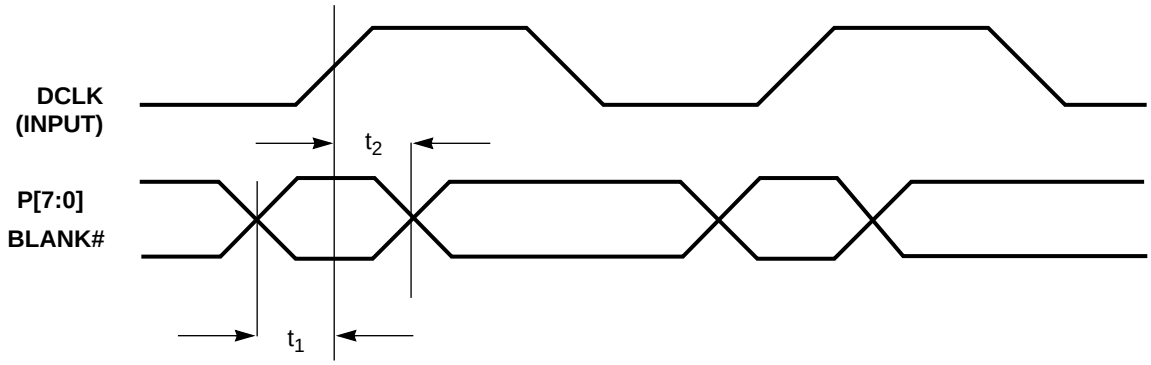


Figure 6-4. Feature Connector Input

Table 6-5. Feature Connector Output

Symbol	Parameter	MIN	MAX	Units
t_1	DCLK to BLANK# delay	–1	1	ns
t_2	DCLK to HSYNC, VSYNC delay	1	3	ns
t_3	DCLK to P[7:0] delay	–2	0	ns

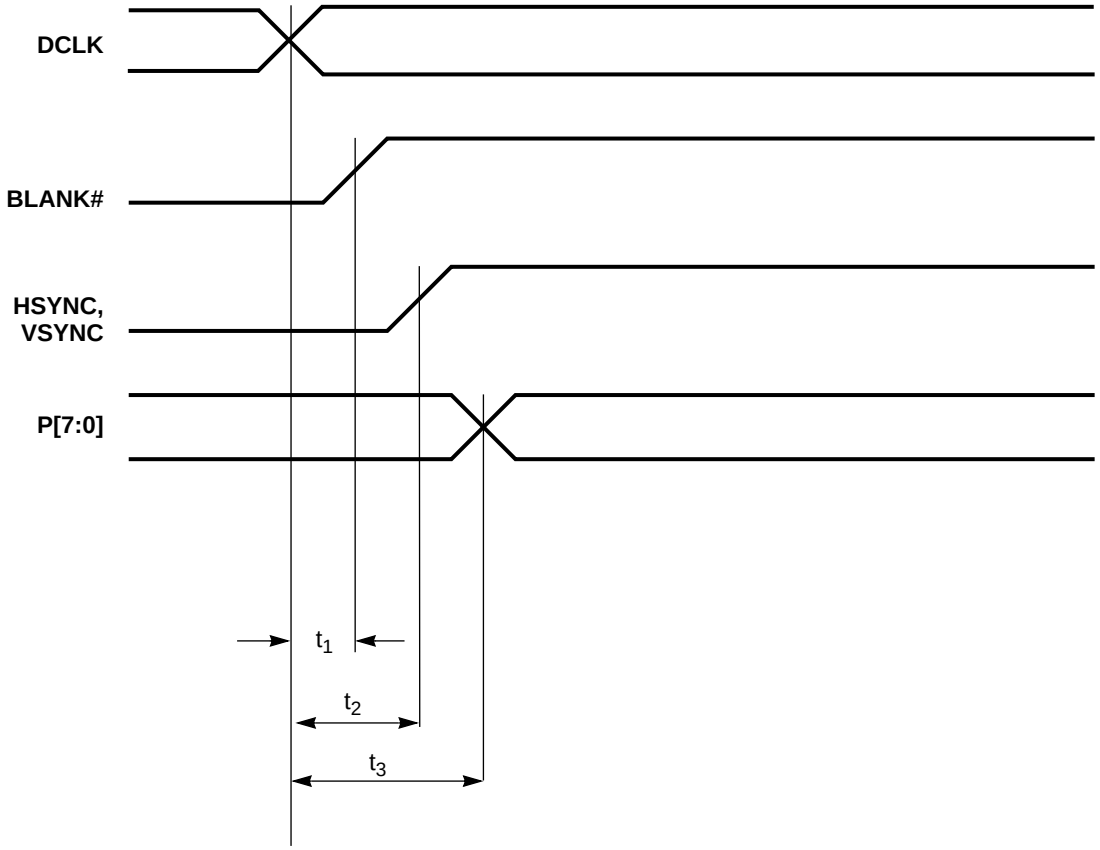


Figure 6-5. Feature Connector Output

Table 6-6. YUV Port (VMI Video) Timing

Symbol	Parameter	MIN	MAX	Units
t_1	VACTIVE setup to PIXCLK	tbd	–	ns
t_2	VACTIVE hold from PIXCLK	tbd	–	ns
t_3	VID[7:0] setup to PIXCLK	tbd	–	ns
t_4	VID[7:0] hold from PIXCLK	tbd	–	ns
t_5	PIXCLK period	35	–	ns

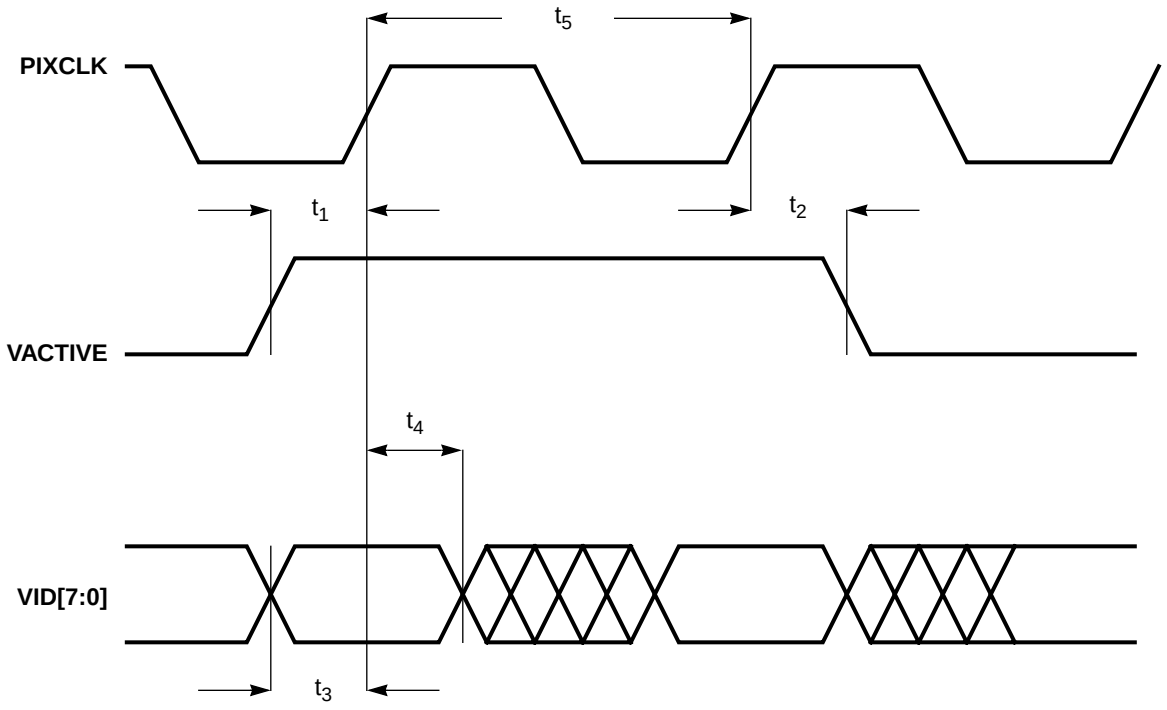


Figure 6-6. YUV Port (VMI Video) Timing

Table 6-7. TV Encoder Out Timing

Symbol	Parameter	MIN	MAX	Units
t_1	EV[7:0] setup to EVCLK	tbd	–	ns
t_2	EV[7:0] hold from EVCLK	tbd	–	ns

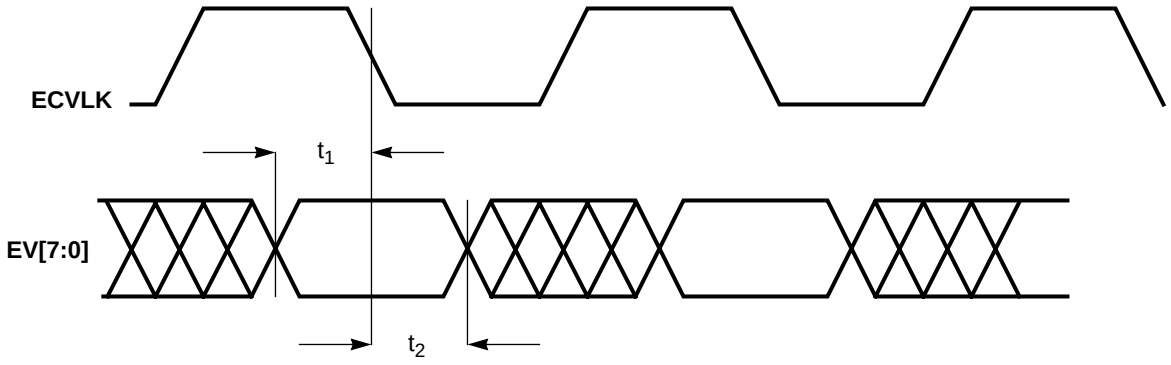


Figure 6-7. TV Encoder Out Timing

Table 6-8. DCLK as Input

Symbol	Parameter	MIN	MAX	Units
t_1	Rise time	–	3	ns
t_2	Fall time	–	3	ns
t_3	High period	40	60	% of t_5
t_4	Low period	40	60	% of t_5
t_5	Period	12.5	–	ns

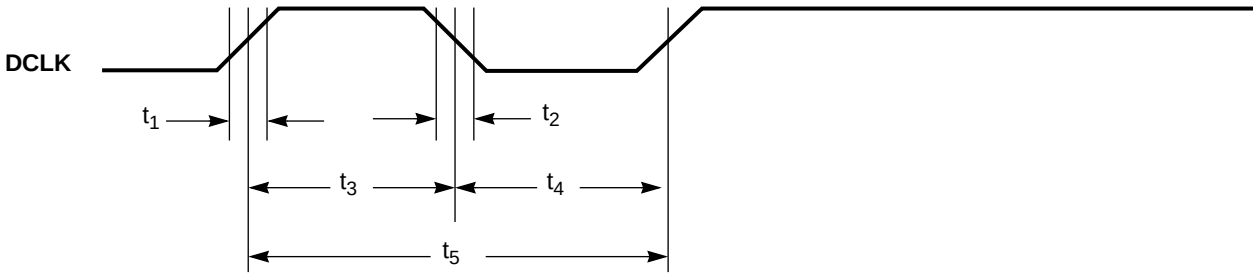


Figure 6-8. DCLK as Input

Table 6-9. RESET Timing

Symbol	Parameter	MIN	MAX	Units
t_1	RESET pulse width	12	–	MCLK
t_2	Configuration pins setup to RST# rising edge	5	–	ns
t_3	Configuration pins hold from RST# rising edge	2	–	ns
t_4	RST# recovery time to first command	tbd	–	ns

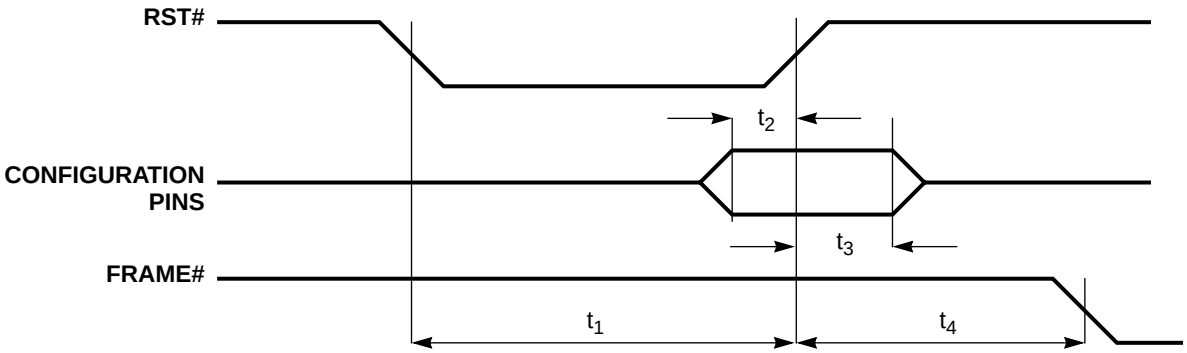
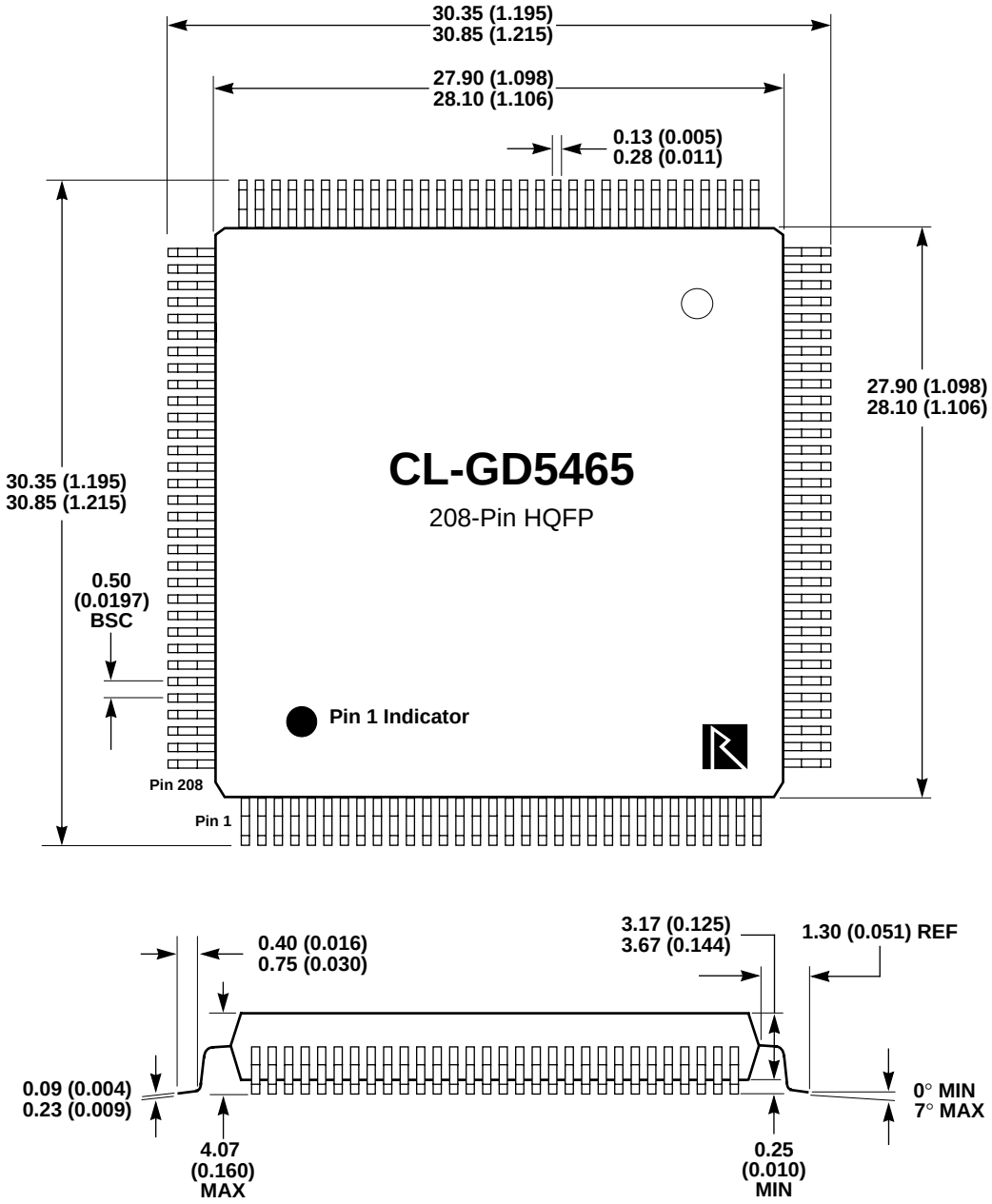


Figure 6-9. RESET Timing

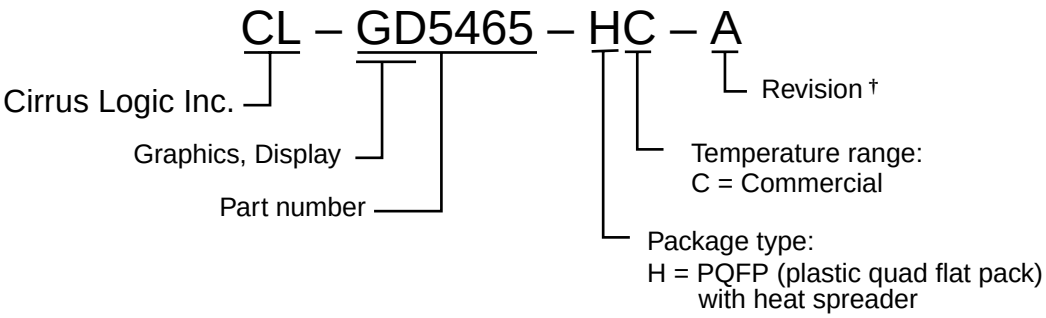
7. PACKAGE SPECIFICATIONS



NOTES:

1) Dimensions are in millimeters (inches), and controlling dimension is millimeter.
2) Drawing above does not reflect exact package pin count.
3) Before beginning any new design with this device, please contact Cirrus Logic for the latest package information.
4) HQFP is a high-performance QFP with an exposed or unexposed heat sink.

8. ORDERING INFORMATION



† Contact Cirrus Logic for up-to-date information on revisions.

Appendix E1

E

Glossary and Bibliography

GLOSSARY

AccuPak®: A video compression method proprietary to Cirrus Logic, Inc. See Chapter 16 and Chapter 17.

Add-in Card, Adapter Card: A circuit board that plugs into a computer motherboard and connects it to some external device, such as a video monitor or storage subsystem.

Alpha Blending: A technique for adding transparency information for translucent objects.

APA (all points addressable): Each pixel on the screen is individually programmable. Any pattern (subject to the resolution of the system) can be displayed. This typically requires that one to two orders of magnitude more information be manipulated than is the case with an AN system. These modes are also referred to as Graphics modes. All extended modes are APA.

AN (alphanumeric): Only those patterns defined in the font tables are displayed. Information can usually be displayed more quickly than is the case with APA images because fewer bits need to be manipulated by the software. These modes are also referred to as Text modes.

Analog Interface: The interface between a video controller and a video display in which pixel colors are determined by the voltage levels on three output lines (RGB). Theoretically, an unlimited number of colors are supported by this method (the maximum number anyone talks about is 16,777,216). The voltage level on any line varies between zero volts (for black) to about 700 mV (for maximum brightness). The lines are typically terminated in 75 Ω at each end. In the IBM world, the analog interface is usually mechanized with a 15-pin, 3-row connector (DB15).

Analog Monitor: A video monitor that uses an analog interface and displays a wide range of color variations. Nearly all monitors currently available are analog monitors.

Analog: A signal that can assume intermediate levels between on and off. Contrast with Digital.

Artifact: A flaw that appears in a display image as a result of a physical disruption of the display image. Examples of artifacts include unwanted flicker, noise, spotting, contouring, or other pattern motion.

ASCII: American Standard Code for Information Interchange. This is a 7-bit code used to encode alphanumeric information. In the IBM-compatible world, this is expanded to eight bits to encode a total of 256 alphanumeric (AN) and control characters.

AUTOEXEC.BAT: A file used to direct a series of activities that occur during system boot-up.

Auto-Monitor Detect: A feature of Cirrus Logic VGA controllers and BIOS that senses the type of monitor that is connected. This uses a scheme that involves the use of comparators to sense the terminations present on the RGB lines. This is replaced with DDC1 and DDC2B.

Bi-linear Interpolation: The process of determining the value of a point (Y) on a plane based on the values of the closest four points. See **Linear Interpolation**.

BIOS-Level Compatibility: With regard to a VGA subsystem, this means that the BIOS supplied is in compliance with the IBM VGA standard. This is the minimum level of compatibility necessary to accommodate the majority of standard applications.

BIOS (basic input output system): In IBM-compatible personal computers, this is a set of ROM-based firmware routines that control the resources of the system and make them available to application programs in an orderly manner. These routines provide basic input/output services for the operating system and for applications programs that use interrupts to call them. Also called ROM BIOS. The Cirrus Logic, Inc. BIOS is written in 80386/486 Assembly Language.

Bit: Binary Digit. A single piece of information: on or off, '0' or '1', high or low, closed or open, up or down, in or out.

BitBLT (bit boundary block transfer): A type of graphics drawing routine that moves a rectangle of data from one area of display memory to another or moves data from system memory to display memory. Graphics controllers frequently include varying degrees of hardware to help speed BitBLT operations.

Bitmap: A rectangular array of locations, each of which is associated with a location (pixel) on a monitor. The contents of each location determines the color of the pixel. Often times there are more locations in the bitmap than on the screen, which allow images to be maintained for later presentation.

Blanking: On a CRT monitor, the beam that causes light to appear on the CRT monitor display screen is said to undergo blanking (that is, made so that it does not appear) during the non-active parts of each scanline and during each horizontal and vertical retrace.

Block Diagram: A diagram in which blocks are used to represent components or subsystems of a system. Usually the blocks are connected with lines indicating data or control flow.

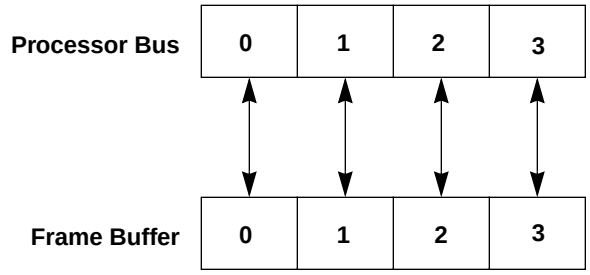
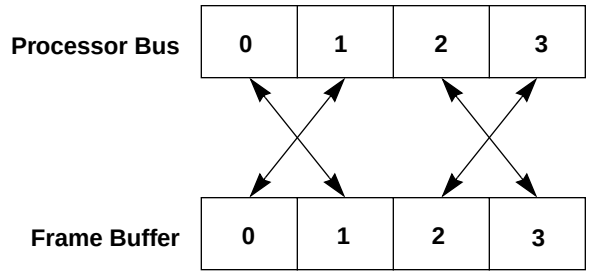
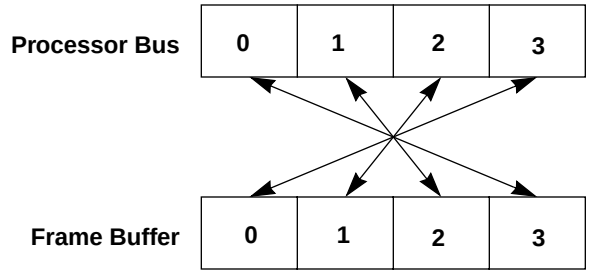
Bus Master: The PCI bus Specification provides for alternate agents to take temporary control of the bus and initiate transfers. When an agent had control of the bus, it is the 'bus master'. The CL-GD546X becomes a bus master to fetch display lists from system memory, as well as other purposes.

Byte: A group of eight bits addressed as a unit. Can take any of 256 (2^8) values.

Byte BitBLT: See MBitBLT.

Byte Swapping: To support operation in a PowerPC PCI system, the CL-GD546X provides byte swapping logic in the host interface. The PowerPC and the PCI bridge perform the swapping required to support byte data. Data types that are larger than a single byte, such as 16-, 24-, and 32-bpp graphics data, require further alignment. Therefore, the frame buffer, host data port, and Memory-Mapped registers each have four different address maps or 'apertures'. This allows the application software to control the data alignment depending on the pixel depth. In Table E1-1, the first aperture (1) performs no swapping; the second aperture (2) swaps bytes within words; the third (3) aperture swaps bytes within dwords. The fourth aperture is for YUV support.

Table E1-1. Byte Swapping for Bi-Endian Support

Aperture	Swap	Diagram
Base address	No swap	
Base address plus 8 Mbytes	word swap	
Base address plus 16 Mbytes	dword swap	
Base address plus 24 Mbytes	–	YUV support

CAS (column address strobe): One of the DRAM control signals.

Capture Resizing: The data being captured can be expanded (zoom) or compressed (shrink) as it is prepared for storage. These two cases are collectively called 'capture resizing'.

CGA (color graphics adapter): This was the first color adapter available for the IBM personal computer. It has low resolution, both spatial and color. While CGA is generally considered obsolete, the VGA standard includes the video modes originally designed for CGA.

Character Cell Matrix: In Text mode, the area of display used to display one character. On the VGA, character cells are either 8, 9, 12, or 16 pixels wide and usually are 8, 14, or 16 pixels high.

Character Clock: This clock is generated by dividing the VCLK by eight or nine. The Monitor Timing Signals (HSYNC, VSYNC) are derived by dividing the character clock.

Chroma Key: The CL-GD5465 can compare the Y, U, and V values of video pixels to upper and lower limits to determine which should be replaced with graphics data. For example, television news programs use chroma key to superimpose the weather reporter on a background ('blue screen' effect).See **Transparent BitBLT**.

Chrominance: The color component of a 2-channel video signal. See **Luminance**.

Clipping: Normally, when doing a BitBLT, the destination rectangle (destination point + destination extents) defines which screen pixels will be affected. When hardware clipping is turned on, the user can also specify a second destination rectangle, called a clipping rectangle. The pixels on the screen that are affected by the BitBLT are those contained in the intersection between the destination rectangle and the clipping rectangle. See Section 14.7 on page 14-21.

CLUT (color lookup table): Translates pixel values from the display memory into color information for the CRT display. It can be found in a Video DAC.

Color Key: The CL-GD5465 can overlay the computer-generated graphics on a pixel-by-pixel basis, with external video. One method of determining whether to overlay a pixel involves comparing it with a specific color or range of colors.

Color Modes: Uses two, four, eight, or more bits-per-pixel. Table E1-2 summarizes the number of colors and the standards for which the colors were first available.

Table E1-2. Color Modes

Bits per Pixel	Number of Colors	Standards
2	4	CGA
4	16	CGA
8	256	VGA
15	32,368	TARGA™
16	65,536	VGA/XGA™
24	16,777,216	Cirrus Logic True Color
32	16,777,216	True Color with Alpha Channel

Color Planes: In planar modes, the display memory is separated into four independent planes of memory, with each plane dedicated to controlling one color component (Red, Green, Blue, and Intensify). Each pixel of the display occupies one bit position in each plane. Planar modes are generally 16 colors. In character modes and packed pixel modes, the data is organized differently.

Comparator: A hardware element used to perform an arithmetic or logical comparison between two fields. The two fields are typically the same width. Arithmetic comparisons include equal, greater than, and less than. Logical comparisons are generally identity.

CONFIG.SYS: A file that provides the system with information regarding application requirements. This information may include peripherals that are connected and require special drivers (such as a mouse). Other information that might be specified is the number of files that can be open simultaneously, or the number of disk drives that can be accessed.

CMOS: Complementary Metal Oxide Semiconductor. A digital logic family that is characterized by high density, low-to-medium power, and medium-to-high speeds. All modern VGA controllers are fabricated using CMOS.

CPU (central processing unit): The master computer unit in a system. In the VGA world, this is typically a 80386, 80486, or Pentium microprocessor.

CRT (cathode ray tube): An electron beam is generated, accelerated, and made to strike a phosphor coating on the inside of an evacuated glass enclosure. The phosphor glows as a result of the energy imparted by the beam. By precisely controlling the position and intensity of the electron beam, meaningful patterns are made to appear in the phosphor and are visible through the glass.

DAC (digital-to-analog converter): The DACs in a VGA system convert the 6- or 8-digital bits-per-color (RED, GREEN, and BLUE) to analog levels suitable for the Analog Interface.

DCLK: The package pin on which the pixel clock (or a multiple or sub-multiple) is present. See also VCLK.

DDC (display data channel): A definition of a communication channel between a computer display and the host system. This is a VESA proposed format. Current Cirrus Logic components and software support either DDC1 or DDC2B.

Digital Interface: A type of interface used between video controller and video display in which display color is controlled by digital color control lines switching on and off. The number of colors that can be supported depends on the number of signal lines in the interface, and is generally either 8, 16, or 64. Most digital interfaces are TTL (transistor-transistor logic)-compatible. CGA, MDA, and EGA use digital interfaces. In the IBM world, the digital interface is usually mechanized with a 9-pin connector.

Digital Monitor (TTL): A monitor that receives its input in the form of a digital code. Typical digital monitors display 8, 16, or 64 colors. Digital monitors are more or less obsolete.

Digital: A method of representing data whereby the individual components are either fully on or fully off.

Digitize: To convert an analog image or signal to a corresponding series of numbers.

Display Memory: The area in the computer memory where the information used to update the screen is kept. In the IBM VGA world, the range of addresses for this data is A000:0 through BFFF:F. Linearly addressed display memory can be placed nearly anywhere in the system address space.

Display Modes: In the IBM-compatible world, a number of standard display modes are defined. Video mode is used interchangeably with Display mode. In addition to the standard modes enumerated below, there are many Extended Display modes.

Table E1-3. Standard Display Modes

Mode(s)	Colors	Alphanumeric Resolution	Pixel Resolution	AN/APA
0,1	16	40 × 25	360 × 400	AN
2,3	16	80 × 25	720 × 400	AN
4,5	4	40 ×25	320 × 200	APA
6	2	80 × 25	640 × 200	APA
7	Mono.	80 × 25	720 × 400	AN
D	16	40 × 25	320 × 200	APA
E	16	80 × 25	640 × 200	APA
F	Mono.	80 × 25	640 × 250	APA
10	16	80 × 25	640 × 350	APA
11	2	80 × 30	640 × 480	APA
12	16	80 × 30	640 × 480	APA
13	256	40 × 25	320 × 200	APA

Dithering: To intersperse a pattern of one color (for example, blue) with a pattern of another color (for example, red) to give the subjective effect of a color somewhere between the two colors (blue and red together make magenta). This technique is effective over large surfaces but fails if the area is too small. This technique creates the appearance of more colors at the expense of resolution.

DIP (dual-inline package): A method of packaging semiconductor chips that was essentially ubiquitous until the 1980s. It is being replaced with plastic quad flatpack and pin grid arrays for devices with high pin counts, and small outline packages for devices with low or medium pin counts.

DPMS (display power management signaling): A proposal to standardize on a common definition and methodology in which the display controller sends a signal to the display that enables it to enter various power management states. This is a VESA proposal. The VGA controller can instruct the monitor go enter one of a number of reduced power states. DPMS is supported by current Cirrus Logic desktop products.

DRAM (dynamic random access memory): A memory technology that is characterized by extreme high density, low power, and low cost. It must be more or less continuously refreshed to avoid loss of data.

Driver: A software module that interfaces a particular display device to an application program to allow operation at higher resolutions than standard VGA.

EEPROM (electrically erasable programmable read-only memory): A memory storage device that can be written repeatedly with no special erasure fixture. EEPROMs do not lose their contents when they are powered down. The Cirrus Logic BIOS can use EEPROMs to record information regarding the connected monitor. This is being replaced with DDC.

EGA (enhanced graphics adapter): This was the second color adapter available for IBM-compatible computers. While EGA is generally considered obsolete, the VGA standard includes the modes originally designed for EGA.

Emulation: Simulation of unavailable hardware by available hardware and software. Emulations improve the usefulness of a product by making it compatible with other products. EGA is capable of emulating MDA and sometimes CGA and Hercules. VGA is capable of emulating EGA, CGA, and MDA.

EPROM (electrically programmable read-only memory): A memory storage device that can be written once (per erasure cycle) and read many times. In the VGA world, it is used for holding the BIOS.

Fast-Page Mode: A read or write mode of DRAMs that is characterized by a decrease in cycle time of about 2–3 times and a corresponding increase in performance. The data accessed in Fast-Page mode cycles must be adjacent in memory.

Feature Connector: An expansion connector on the VGA that can be used to accept or drive video signals to or from the VGA. This is used in applications involving video overlay. This is also called the VESA Pass-through connector.

FIFO: First In First Out. A memory that can temporarily hold data so that the sending device can send data faster than the receiving device can accept it. The sending and receiving devices typically operate asynchronously.

Fixed-Frequency Monitor: A monitor that can accept a fixed horizontal frequency, usually 31.5 kHz. Such monitors can accommodate different vertical resolutions by operating at different vertical frequencies, usually 60 and 70 Hz.

Flicker: Flicker occurs when the display is not refreshed at a fast enough rate. Specific items on the screen seem to appear and disappear at a high frequency. Flicker depends on the refresh rate, the ambient lighting, and very strongly on what the observer is used to. Many U.S. users notice flicker on PAL TV in Europe until they become adjusted.

Fog Effect: An imaging effect where objects further from the observer are made less distinct, usually by being rendered with additional white.

Frequency Synthesizer: An electronic circuit that can generate a number of frequencies from a fixed reference frequency. Some frequency synthesizers can generate only a relatively small number of frequencies; others can generate hundreds of different frequencies.

Glue Logic: Additional logic devices required to interconnect the major components of a system.

Graphics Controller: On EGA and VGA, a section of circuitry that can provide hardware assist for graphics drawing algorithms by performing logical functions on data written to display memory.

Graphics Mode: (Also APA) A display mode in which all pixels on the display screen can be controlled independently to draw graphics objects (as opposed to Text mode, in which only a pre-defined set of characters can be displayed).

Hardware: A computing system is normally spoken of as having two major components: hardware and software. Hardware is the portion that executes the step-by-step procedure necessary to perform a particular task as instructed by the software.

Hardware Occlusion: When graphics and video are mixed on a pixel-by-pixel basis, one is said to occlude, or *overlay* the other. This can be accomplished by mixing the images in software, but is more often done in the display pipeline.

HERC (Hercules® graphics adapter) (HGC): The third display format standardized for the PC family of computers, following the MDA and CGA. It provides standard 80-character-by-25-row alphanumeric display, and 720 horizontal by 348 vertical pixels in Monochrome Graphics mode. It was designed as a replacement for MDA, and provided monochrome APA. Cirrus Logic BIOSs generally do not provide Hercules emulation.

Hex Code, Hexadecimal: A numbering system using base 16. The allowable digits are 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, A, B, C, D, E, and F. A base 16 numbering system is useful because conversion to and from base 2 is trivial. Numbers written in base 16 are typically denoted by a prepended ‘0x’ or an appended ‘h’.

High Color: 15- to 16-bits-per-pixel color providing photo-realistic image quality.

Interlaced: A graphics system in which the even scanlines are refreshed in one vertical cycle (field), and the odd scanlines are refreshed in another vertical cycle. The advantage is that the video bandwidth is roughly half that required for a non-interlaced system of the same resolution. This results in less costly hardware. It also may make it possible to display a resolution that would otherwise be impossible on given hardware. The disadvantage of an interlaced system is flicker, especially when displaying objects that are only a single scan line high.

Interpolation: A function that may be used to obtain additional values from sampled values.

ISA (industry standard architecture): In reference to IBM-compatible computers, it was the definition of the standard bus until the introduction of VESA and PCI in the early 1990s.

Linear Addressing: This is a modern method of addressing the display memory. The display memory (in the IBM PC world) was originally was located in a 128-Kbyte area from A000:0 through BFFF:F, too small for the display systems of today with multi-megabyte memories. Linear addressing allows the display memory to be addressed in upper memory, where a large contiguous area is set aside for it.

Linear Interpolation: the process of determining the value of a point on a line based on the values of the two nearest adjoining points.

Luminance: The black-and-white (that is, brightness) component of a 2-channel video signal. The luminance of a color is the color wavelength (also known as 'spectral radiance') and its conversion to luminance values. The luminance component is often called the 'Y' component. See **Chrominance**.

Mapping: Mapping refers to the definition of memory for storing data used by a particular Video mode. The range of addresses reserved for video information in IBM-compatible systems is from A000:0 to BFFF:F.

MBitBLT (Byte BitBLT): Byte BitBLTs are available at all pixel depths to simplify off-screen memory management, making large parts of typical drivers independent of the color depth. Byte BitBLTs are also called monochrome BitBLTs although they are not monochrome BitBLTs.

MCGA (multicolor graphics array): A graphics adapter designed for the PS/2 series of personal computers, with similar function to the CGA and downwardly compatible to the CGA at the BIOS, control register, and display memory levels. Like the VGA, the MCGA drives either an analog monochrome or analog RGB monitor.

MDA (monochrome display adapter): The original display adapter marketed by IBM for personal computers. MDA has no bit-mapped graphics capability.

Memory-Mapped I/O: Using memory-mapped I/O, registers can be addressed in memory space. This is generally faster than using I/O cycles since more data can be transferred per access and the processors are often optimized for memory cycles.

Monitor: Another term for a CRT display.

Monochrome Modes: Uses one bit per pixel. 'Two-color' modes are similar to monochrome modes because they can display two colors; the two colors do not need to be black and white, sometimes they are amber or green with black.

Motherboard: The large printed circuit board in a personal computer into which the adapter boards plug. It contains the CPU and core memory. It can also contain the video controller and a number of other peripheral controllers.

Multiple-FIFO Architecture: A video controller architecture that is characterized by having multiple (two or more) FIFOs or Write Buffers. There is typically one FIFO or Write Buffer at the CPU interface and one or more FIFOs in the screen refresh stream.

Multifrequency Monitor: A monitor that accommodates a variety of horizontal and vertical synchronization frequencies. This type of monitor accepts inputs from many different video display adapters, and is typically capable of either analog or digital input.

Nibble: A group of four bits, typically contiguous. It can take any of 16 (2^4) values.

Non-interlaced: A video system in which every pixel is refreshed during every vertical scan. A non-interlaced system is normally more expensive than an interlaced system of the same resolution, and is usually said to have a more pleasing appearance.

NTSC (National Television Standards Committee): A color encoding scheme used for television. NTSC is used in North America and Japan, as well as some other areas. NTSC is often spoken of as a timing standard; it is an extension of RS-170.

Occlusion: The superimposition of individual pixels of graphics onto video or video onto graphics. The CL-GD5465 supports occlusion based on color key or chroma key. See also **Chroma Key** and **Color Key**.

Offset: In the CL-GD546X, the MMIO offset of a register is the distance from the MMIO base address specified in PCI14.

Off Screen: The frame buffer comprises two major classes of storage. These is the image being displayed at the moment; this is in on-screen memory. In addition, these are other things, such as fonts, the Z-buffer, texture maps, and images that are not being displayed; these are in off-screen memory.

On Screen: See **Off Screen**.

Overlay: The superimposition of video (typically live) onto computer generated graphics.

Overscan: That portion on all four sides of the display between active video and blanking. The overscan area is also called the border.

Packed Pixel: Color information for a pixel packed into one word of memory data. For a system with few colors, this packed pixel may require only a part of one word of memory; for very elaborate systems, a packed pixel might be several words long. See **Planar**.

PAL: A color encoding scheme used for television. PAL is used in Europe (except France), as well as some other places.

Palette: The range of colors available on the screen, not necessarily simultaneously. For VGA, this is either 16 or 256 simultaneous colors out of 262,144. For nearly all Cirrus Logic products, the palette is extended to 32,768, 65,536, or 16,777,216 simultaneous colors on the screen.

Palette DAC: The triple eight-bit DAC with its associated lookup table.

Pitch: The scanline-to-scanline byte address offset. Also called stride or offset.

Pixel: An acronym for picture element, and is also called a pel. A pixel is the smallest addressable graphic on a display screen. In RGB systems, the color of a pixel is defined by some Red intensity, some Green intensity, and some Blue intensity.

Planar: In video terms, the pixel color information is stored in four bits across four memory planes. This allows a maximum of 16 colors (2^4). See **Packed Pixel**.

Primary RGB: The red, green, and blue bits that are present for a display image.

RAM BIOS: The BIOS can be copied from relatively slow ROM into relatively fast RAM. When this is done, it executes faster, enhancing performance of the subsystem being controlled.

RAM (random access memory): This term has come to mean any semiconductor memory whose write access time is approximately the same as its read access time. This is typically taken to include SRAMs (Static RAMs) and DRAMs (dynamic RAMs). This definition specifically eliminates memories that cannot be altered at all and memories that require a special fixture for erasing (such as EPROMs).

RDRAM (Rambus® DRAM): A DRAM technology characterized by a very high transfer rate. The the CL-GD546X family is designed to be used with RDRAMs.

RAS (row address strobe): A DRAM control signal.

Refresh (Display or Screen Refresh): An image drawn on a CRT display remains visible only for a few milliseconds (the persistence of the screen phosphor), unless it is redrawn continuously. This process is called display refresh or screen refresh. Different displays use different refresh rates, but display refresh is normally required between 60 and 80 times a second to avoid any visible screen flickering. 75 times a second is a common refresh rate. In general, a higher refresh rate results in more stable appearing display.

Register-Level Compatibility: If a peripheral is compatible at the register level with another peripheral, it means that every bit in every register of the two devices has precisely the same meaning. This implies that application programs can circumvent the BIOS and directly program registers in a peripheral device without functionality problems. Cirrus Logic controllers are register-level-compatible with the IBM VGA standard.

Registers: In a VGA controller, these are the storage elements that contain data relating to the mode or configuration of the device, as opposed to the display memory that contains the image. Traditionally, the registers are divided into six groups: General, Sequencer, CRTC, Graphics Controllers, Attribute, and Extensions. The VGA registers are accessed by a number of addressing schemes, each involving an index or address register and a data register. In current Cirrus Logic products, extension registers are often addressable using memory-mapped I/O.

Resolution, Color: The number of simultaneous colors is determined by the number of bits associated with each pixel in the display memory. The more colors, the more bits. If n bits-per-pixel are used, 2^n color combinations can be generated. EGA uses from one to four bits-per-pixel, permitting up to 16 (2^4) colors to be displayed on the screen at the same time. The VGA has an added mode that supports eight bits-per-pixel, or 256 (2^8) simultaneous colors. Current Cirrus Logic products have additional modes that support up to 24 bits-per-pixel or 16,777,216 (2^{24}) simultaneous colors. In addition, some modes use a fourth byte, the alpha byte.

Resolution, Spatial: The number of pixels in an area or on the screen. Resolution is typically specified as pixels per scanline and scanlines per frame. Higher resolution images require more processing and greater storage requirements per image. In addition, monitor costs increase with resolution, particularly above about one million pixels. Different applications require different resolutions.

RGB (red, green, and blue): Used with color displays, an interface that uses three color signals (red, green, and blue), as opposed to an interface used with a monochrome display that requires only a single signal. Both digital and analog RGB interfaces exist.

ROM (read-only memory): A type of memory that is characterized by not being alterable (see EPROM). ROMs are typically used to contain low-level programs that do not change, such as BIOS.

ROP (Raster Operation): A BitBLT operation that combines source bytes with destination bytes, using various logic operations. See **BitBLT**.

Saturation: In the HIS color scheme, saturation is the degree that the hue of a color appears to be undiluted by its complementary color. to form white.

Scanline: Pixels on the screen that have the same vertical address are on the same scanline.

Simultaneous Colors: The number of colors in a display system that can be displayed on the screen at one time. This number is limited by the circuitry of the display adapter, and is sometimes much smaller than the number of colors the display device can actually support. The number of simultaneous colors that a display adapter supports is normally determined by the number of color planes, or bits per pixel, that it uses. For example, a device with four bits-per-pixel supports 16 simultaneous colors.

Sleep Mode: A VGA controller can be put to 'sleep' by writing a value to a particular bit of a particular register. The register is normally at address 3C3 or 46E8 in the IBM-compatible world. When a VGA controller is asleep, it responds to no further commands except a command to wake up or a BIOS read. This allows two VGA controllers to share common addresses, so long as their sleep addresses and BIOS addresses are not the same. PCI uses a different sleep mechanism than do ISA and VESA VL-Bus.

SMT (surface mount technology): A method of mounting devices (such as integrated circuits, resistors, capacitors, and others) on a printed circuit board, characterized by not requiring mounting holes. Rather, the devices are soldered to pads on the printed circuit board. Surface-mount devices are typically smaller than the equivalent through-hole devices.

Software: A computing system is normally spoken of as having two major components: hardware and software. Software is that portion that instructs the hardware in the step-by-step procedure necessary to perform a particular task.

Swizzle: To swap bits within a byte. For example, bit 7 with bit 0 and bit 0 with bit 7; bit 6 with bit 1 and bit 1 with bit 6; bit 5 with bit 2 and bit 2 with bit 5; bit 4 with bit 3 and bit 3 with bit 4.

SVGA (Super VGA): Graphics adapters that extend the capabilities of the features provided by the original IBM VGA. The first Super VGA provided a 640 x 480 x 256-Color mode.

Texel: The entries in the texture map in the TLUT. Texel is derived from texture pixel.

TLUT (texture lookup table): Translates texel values from the display memory into color information for the CRT display.

Transparent BitBLT: A type of BitBLT that uses chroma keying (a type of masking) to combine two sources of data. In the figure that follows, where the chroma key is:

- Not detected in source 1, data is taken from source 1.
- Detected in source 1, data is taken from source 2.

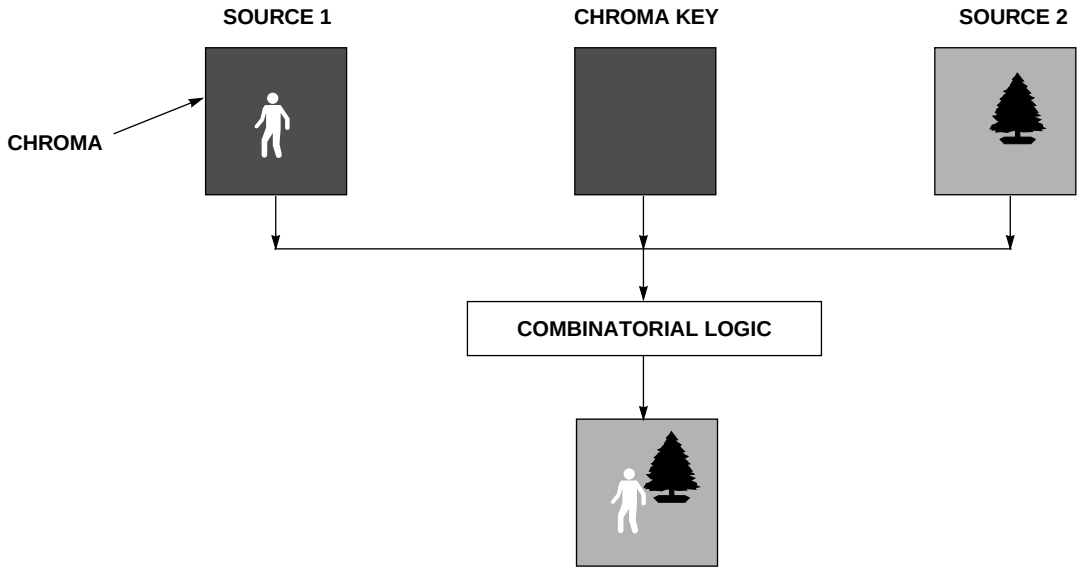


Figure E1-1. Chroma Key: Transparent BitBLT

True Color: 24-or 32-bits-per-pixel color providing photo-realistic image quality.

TTL (transistor-transistor logic): A collection of logic families developed beginning in the 1960s. TTL is gradually being replaced with CMOS for all but the fastest or most cost-sensitive applications.

VCLK: The internal signal operating at the pixel rate.

Vertical Retrace: The time interval immediately following the completion of a complete frame (or field for an interlaced display). The electron beam returns to the top of the display screen in preparation for the next frame or field during this period.

VESA® (Video Electronics Standards Association): A consortium of CRT monitor vendors, graphics chip vendors, and graphics software vendors that set hardware and software standards for PC-compatible graphics monitors and software interfaces. Cirrus Logic is an active participant on many of the VESA committees.

VGA (video graphics array): The VGA standard was introduced by IBM in 1987. In the IBM definition, the maximum spatial resolution is 640 x 480 (modes 11 and 12), and the maximum color resolution is 256 colors (mode 13). Now the spatial resolution is enhanced or extended through third party chip vendors to 1600 x 1200 with up to 16,777,216 colors.

Video Capture: The act of transferring a video stream to the frame buffer. Once captured, video is typically displayed in realtime or transferred to a disk for later display or analysis.

Video Pipeline: The hardware that fetches data from the frame buffer, processes it (for example, YUV-to-RGB color space conversion or zoom), and presents it to the DAC for conversion to analog and display. This term is used at Cirrus Logic to include the hardware used to process graphics information, as well as video information.

Video Stream: Video information taken over an extended time (many frames).

Video Window: An area of a computer display screen that has been allocated for an overlay image. The video window can be positioned anywhere on a display screen.

VLSI (very large scale integration): The technology of manufacturing integrated circuits (chips) with thousands of transistors on a single device. The personal computer was made possible because of VLSI technology.

VRAM (video random access memory) (dynamic): Memory chips with two ports, one used for random accesses and the other capable of serial accesses. Once the serial port has been initialized (with a transfer cycle), it can operate independently of the random port. This frees the random port for CPU accesses. The result of adding the serial port is a significantly reduced amount of interference from screen refresh. VRAMs cost more per bit than DRAMs.

Wait State: When a system processor is reading or writing a memory or peripheral device that cannot respond fast enough, one or more time intervals (typically on the order of tens of nanoseconds each) are inserted during which the processor does nothing but wait for the slower device. While this has a detrimental effect on system throughput, it is unavoidable. The number of wait states can be reduced using techniques such as CPU-bus caches or write FIFOs.

Word: The amount of memory that a given computer can access in a single cycle. In the IBM-compatible world, this is either 16 or 32 bits.

Write Buffer: A term used in the CL-GD546X literature to denote the buffer that is logically positioned between the CPU interface and the display memory.

YCrCb: A color space defined in CCIR601. The ‘Y’ stands for the black-and-white (also called the ‘luminance’) component of the color space. ‘Cr’ and ‘Cb’ are respective scaled versions of ‘U’ and ‘V’, the color (also called ‘chrominance’) components in the YUV color space

YUV: A color space format generally associated with broadcast television. The ‘Y’ stands for the black-and-white (also called ‘luminance’) component of the color space. The ‘U’ and ‘V’ stand for the color (also called ‘chrominance’) components of the color space.

Z-Buffer: The depth buffer. This is an array that have an entry for each pixel on the screen. Each entry contains a value that indicates the depth (that is, how far from the observer) of the corresponding pixel.

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