

# V6355D

(LCDC)

## ■ OUTLINE

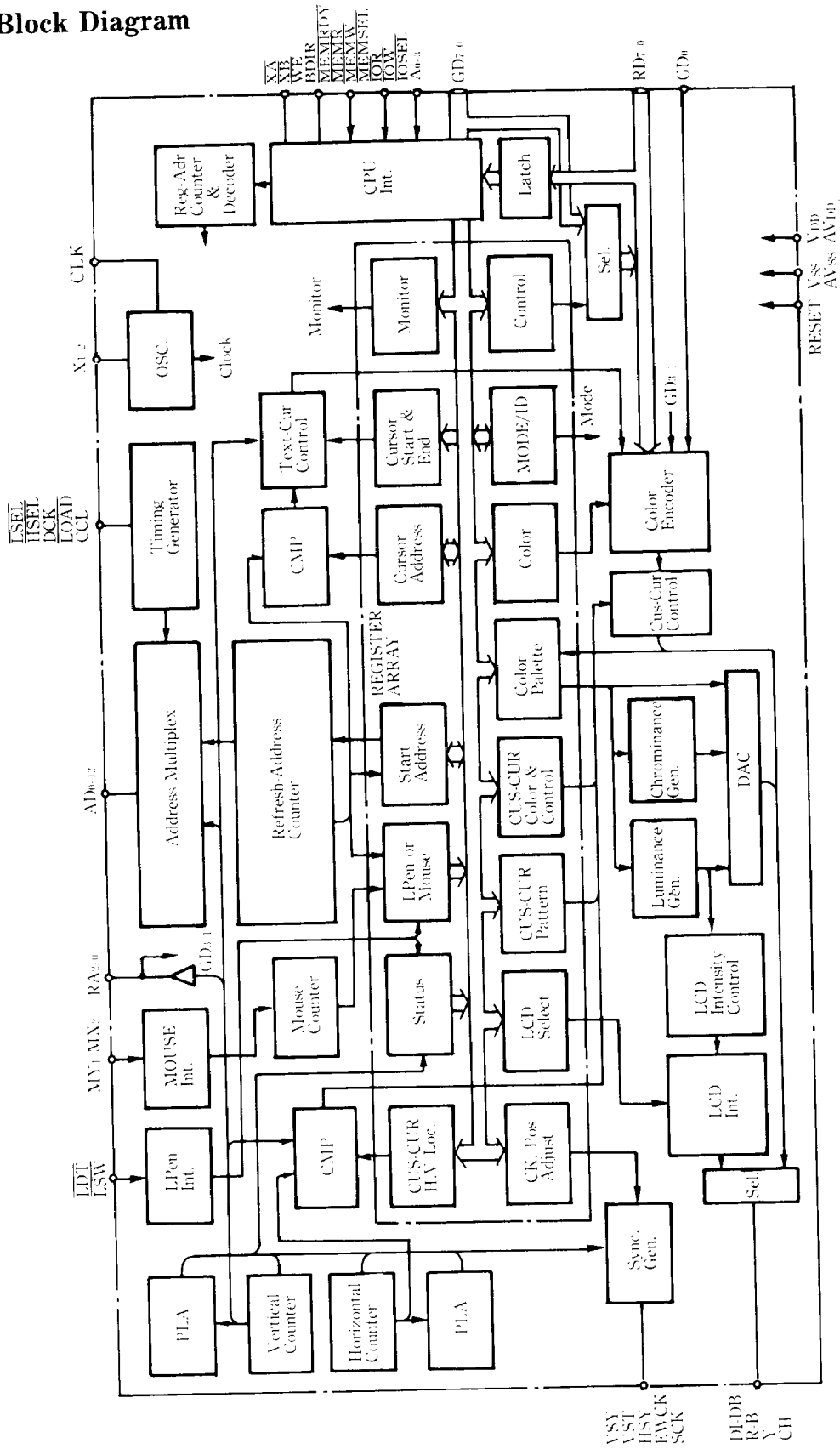
V6355D (LCDC) is a silicon gate CMOS device. This controller can be connected to both LCD and CRT displays. It is software compatible with IBM-PC and has a function to expand it.

V6355-DF is a 100 pin plastic flat package (QFP) type and V6355-DJ is a 84 pin plastic chip carrier type.

## ■ FEATURES

- Capable of controlling both LCD and CRT displays.
- Includes 6845 restricted mode and CRT peripheral circuits for IBM-PC.
- Both SRAM and DRAM are usable as VRAM.
- Includes MOUSE and LIGHT PEN interface.
- Cursor position can be specified by any  $16 \times 16$  dot patterns in the bit unit (AND and EXOR screens).
- Includes color palette (16/512 colors).
- LCD intensity controllable (16 or 8 gradation steps)
- Screen modes are available in combinations of the following.
  - Horizontal dot number: 640, 320, 512, 256
  - Vertical dot number: 192, 200, 204, 64 (64 only with LCD)
  - Raster adjustment: 0, 2, 4 or 6 specifiable
- Capable of displaying 16 colors in  $640 \times 204$  by using external circuits.
- CRT monitor selectable from among IBM Color, Monochrome, NTSC system and PAL system.
- Can be interfaced with 3 types of LCD driver.
- Usable with 16 bit bus CPU.

LCDC Block Diagram

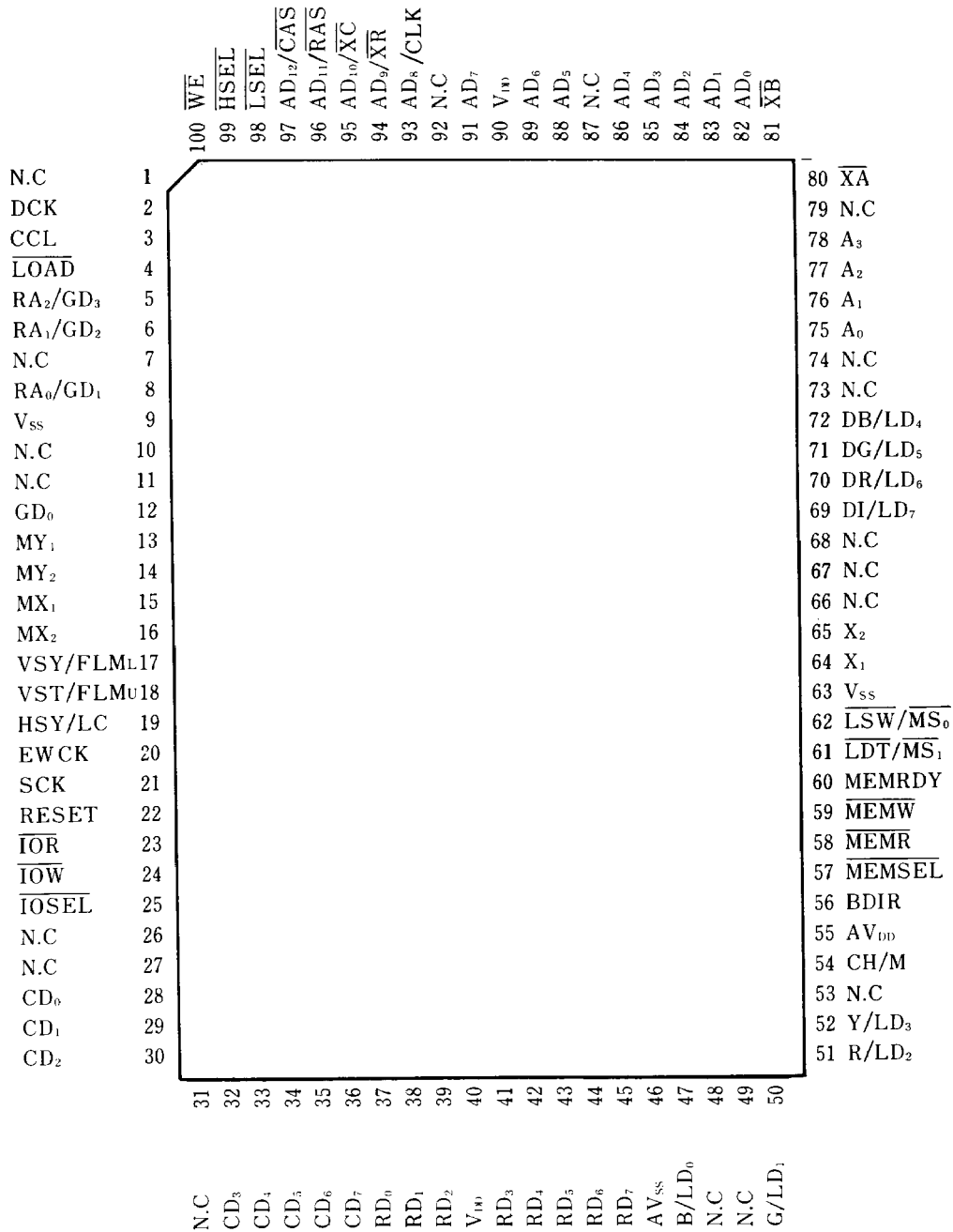


## ■ Pin Functions

Signature	I/O	Description	
$\overline{\text{IOR}}$	I	Read enable for I/O register, Active at low level	
$\overline{\text{IOW}}$	I	Write enable for I/O register, Active at low level	
$\overline{\text{IOSEL}}$	I	High-order bit decode signal of I/O register address signal, selected at low level	
A <sub>0</sub> A <sub>1</sub> A <sub>2</sub> A <sub>3</sub>	I I I I	I/O register address signal	
$\overline{\text{MEMSEL}}$	I	High-order bit decode signal of memory address signal, selected at low level	
$\overline{\text{MEMR}}$	I	Read enable for memory, Active at low level	
$\overline{\text{MEMW}}$	I	Write enable for memory, Active at low level	
$\overline{\text{MEMRDY}}$	O	Memory (VRAM) access ready signal, Busy (wait) at low level (High impedance state when memory non-selected ( $\overline{\text{MEMSEL}}$ = high level))	
$\overline{\text{WE}}$	O	Write enable for memory	
$\overline{\text{BDIR}}$	O	Direction control of bi-directional buffer (for CPU data bus)	
$\overline{\text{RESET}}$	I	Reset signal	
CD <sub>0</sub> ⋮ CD <sub>7</sub>	I/O I/O I/O	Data bus with CPU	
RD <sub>0</sub> ⋮ RD <sub>7</sub>	I/O I/O I/O	Data bus with VRAM	
AD <sub>0</sub> ⋮ AD <sub>7</sub>	O O O	VRAM address	
AD <sub>8</sub> / $\overline{\text{CLK}}$  AD <sub>9</sub> / $\overline{\text{XR}}$ AD <sub>10</sub> / $\overline{\text{XC}}$ AD <sub>11</sub> / $\overline{\text{RAS}}$ AD <sub>12</sub> / $\overline{\text{CAS}}$ $\overline{\text{XB}}$  $\overline{\text{XA}}$	O  O O O O O	At SRAM	At DRAM
		VRAM address	Outputs external clock dividing signal of 14.31818MHz. Usable for CPU clock by dividing. CPU row Address enable CPU column Address enable
		do.	$\overline{\text{RAS}}$
		do.	$\overline{\text{CAS}}$
		do.	—
		do.	—
Data enable when memory read/write	—		
Memory read/write timing (CPU address enable at SRAM)	—		
$\overline{\text{LSEL}}$ $\overline{\text{HSEL}}$	O O	At SRAM (8bit CPU)	16bit CPU
		1st 8K byte selected 2nd 8K byte selected	Low byte selected High byte selected

Signature	I/O	Description	
		A/N Mode	640 × 200 Color mode
RA <sub>2</sub> /GD <sub>3</sub> RA <sub>1</sub> /GD <sub>2</sub> RA <sub>0</sub> /GD <sub>1</sub> GD <sub>0</sub>	I/O I/O I/O I	Raster address (Output)  Dot data for character display	Graphic data (Input)
		CRT	LCD
VS <sub>Y</sub> /FLM <sub>L</sub> VS <sub>T</sub> /FLM <sub>U</sub> HS <sub>Y</sub> /LC EWCK  SCK	O O O O  O	Vertical synchronizing signal Vertical retrace line period Horizontal synchronizing signal Display valid period  —	Lower block FLM Upper block FLM Latch clock Driver enable signal or tone graduation intensifying signal Shift clock
CH/M Y/LD <sub>3</sub>  R/LD <sub>2</sub> G/LD <sub>1</sub> B/LD <sub>0</sub> DI/LD <sub>7</sub> DR/LD <sub>6</sub> DG/LD <sub>5</sub> DB/LD <sub>4</sub>	O O  O O O O O O O	Chrominance signal Brightness (black/white composite) signal  Output for linear RGB  Output for IBM monitor	Signal to change into AC  Data output for upper block  Data output for lower block
DCK CCL <u>LOAD</u>	O O O	Dot shift clock (for P/S) VRAM data latch clock Load signal for P/S	
MY <sub>1</sub> MY <sub>2</sub> MX <sub>1</sub> MX <sub>2</sub> <u>LDT/MS<sub>1</sub></u> <u>LSW/MS<sub>0</sub></u>	I I I I I I	Counter pulse for MOUSE Y direction  Counter pulse for MOUSE X direction  Light pen detect signal or mouse switch signal Switch signal of light pen or mouse	
X <sub>1</sub> X <sub>2</sub> AV <sub>SS</sub> AV <sub>DD</sub> V <sub>SS</sub> V <sub>SS</sub> V <sub>DD</sub> V <sub>DD</sub>	I O I I I I I I	For X'tal oscillation, Input to X <sub>1</sub> when inputting external clock  0V +5V 0V 0V +5V +5V Analog (for DAC) power supply  Digital power supply	

## ■ Pin Assignment



■ Electrical Characteristics

① Absolute maximum ratings

Parameter	Signature	Min.	Max.	Unit
Supply voltage	V <sub>DD</sub>	-0.5	+7.0	V
Input voltage	V <sub>I</sub>	-0.5	V <sub>DD</sub> +0.5	V
Output voltage	V <sub>O</sub>	-0.5	V <sub>DD</sub> +0.5	V
Operating temperature	T <sub>OP</sub>	0	+70	°C
Storage temperature	T <sub>STG</sub>	-50	+125	°C

(V<sub>SS</sub>, AV<sub>SS</sub>=0.0V as standard)

② Recommended conditions for use

Parameter	Signature	Min.	Typ.	Max.	Unit
Supply voltage	V <sub>DD</sub>	4.75	5.0	5.25	V
Operating temperature	T <sub>OP</sub>	0	25	70	°C

Used with V<sub>DD</sub> and AV<sub>DD</sub> at the same voltage and V<sub>SS</sub>, AV<sub>SS</sub>=0.0V.

③ DC characteristics

Parameter	Signature	Conditions	Min.	Max.	Unit
High-level output voltage (TTL)	V <sub>OH</sub>	I <sub>OH</sub> =-0.4mA	2.7		V
Low-level output voltage (TTL)	V <sub>OL</sub>	I <sub>OL</sub> =0.8mA		0.4	V
High-level output voltage (CMOS)	V <sub>OH</sub>	I <sub>OH</sub> <1μA		V <sub>DD</sub> -0.4	V
Low-level output voltage (CMOS)	V <sub>OL</sub>	I <sub>OL</sub> <1μA		0.4	V
High-level input voltage	V <sub>IH</sub>		2.2		V
Low-level input voltage	V <sub>IL</sub>			0.8	V
High-level output current	I <sub>OH</sub>	V <sub>OH</sub> =2.7V	-0.4		mA
Low-level output current	I <sub>OL</sub>	V <sub>OL</sub> =0.4V	0.8		mA
Input leak current	I <sub>L</sub>		-10	10	μA
Output leak current (tri-state)	I <sub>LZ</sub>		-10	10	μA
Supply current (at normal operation)	I <sub>DD</sub>	R <sub>L</sub> =5.6KΩ		70	mA
Supply current (at standby)	I <sub>DD</sub>	R <sub>L</sub> =5.6KΩ		50	mA
High-level clock input voltage	V <sub>CH</sub>		3.6		V
Low-level clock input voltage	V <sub>CL</sub>			0.6	V

• V<sub>DD</sub>, AV<sub>DD</sub>=5.0V ± 5%, T<sub>OP</sub>=0~70°C

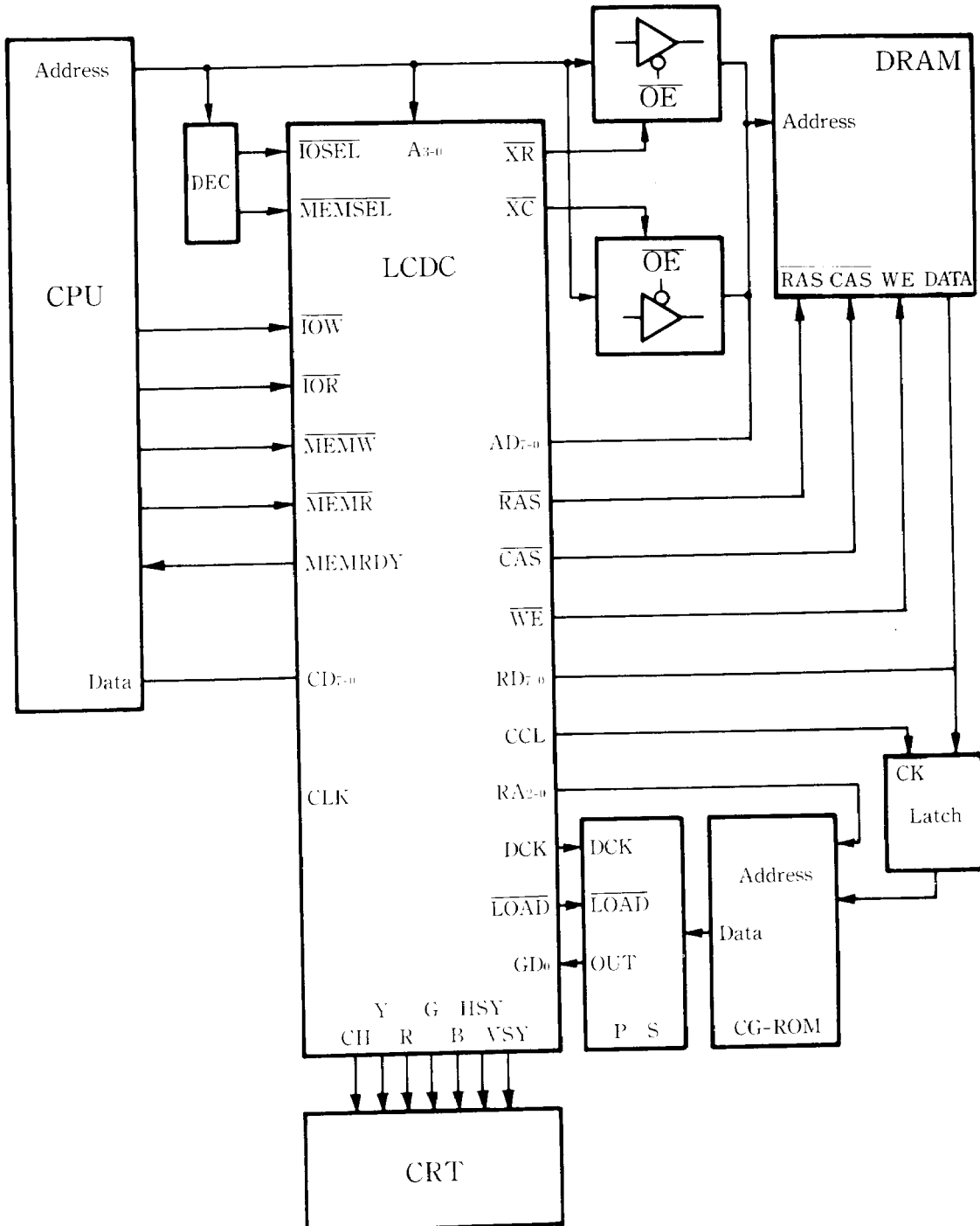
Supply voltage is obtained by adding mean current at V<sub>DD</sub> and AV<sub>DD</sub> terminals.

• R<sub>L</sub>: Terminal resistance between Y, R, G, B, CH terminals and GND.

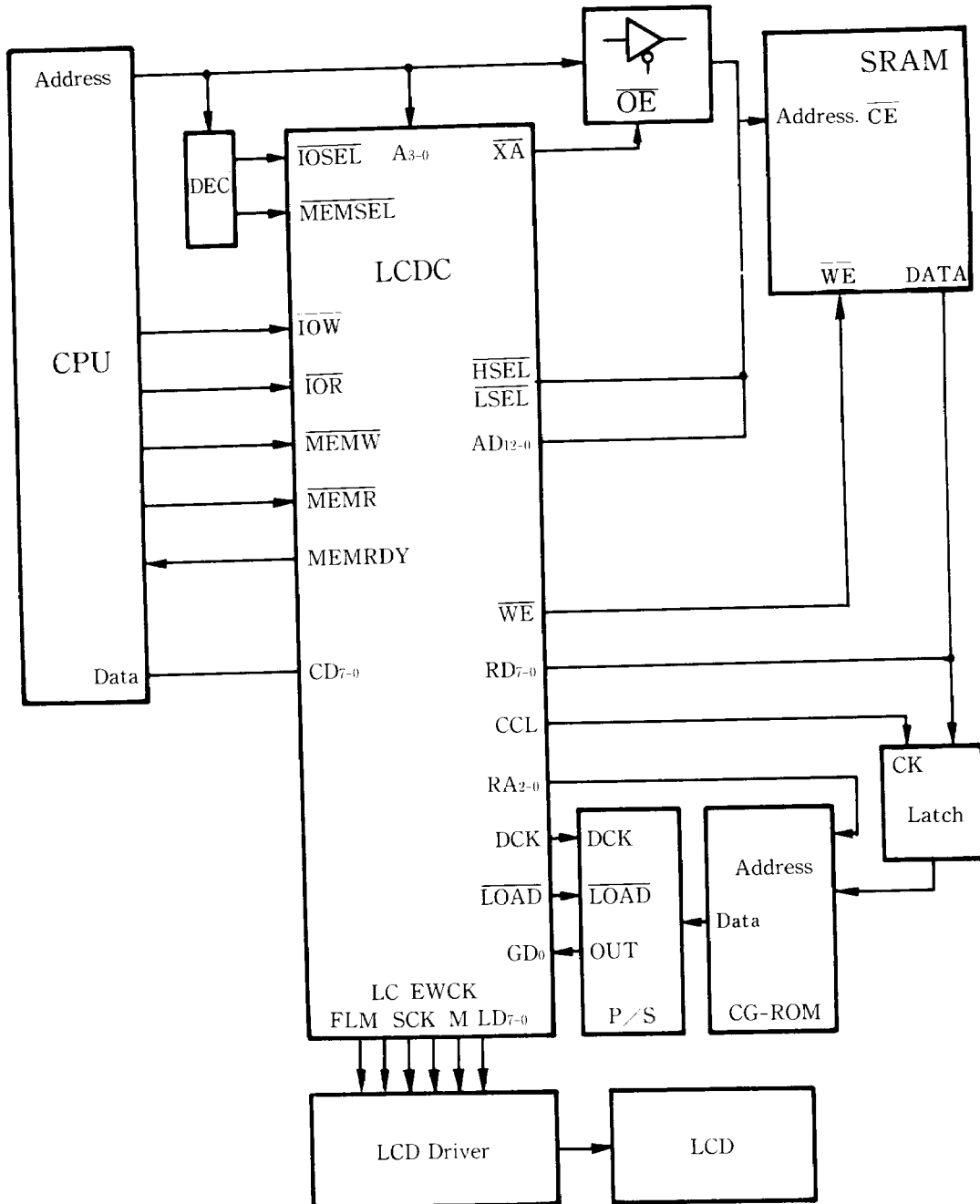
Output leak current (tri-state) is for when CD<sub>0-7</sub>, RD<sub>0-7</sub> and RA<sub>2</sub>/GD<sub>3</sub>~RA<sub>0</sub>/D<sub>1</sub> are in the input mode and when AD<sub>0</sub>~AD<sub>12</sub>  $\overline{\text{CAS}}$ ,  $\overline{\text{LSEL}}$ ,  $\overline{\text{HSEL}}$  and MEMRDY are in the high impedance mode.

## ■ System Configuration (Examples)

### ① When using CRT display (DRAM used)



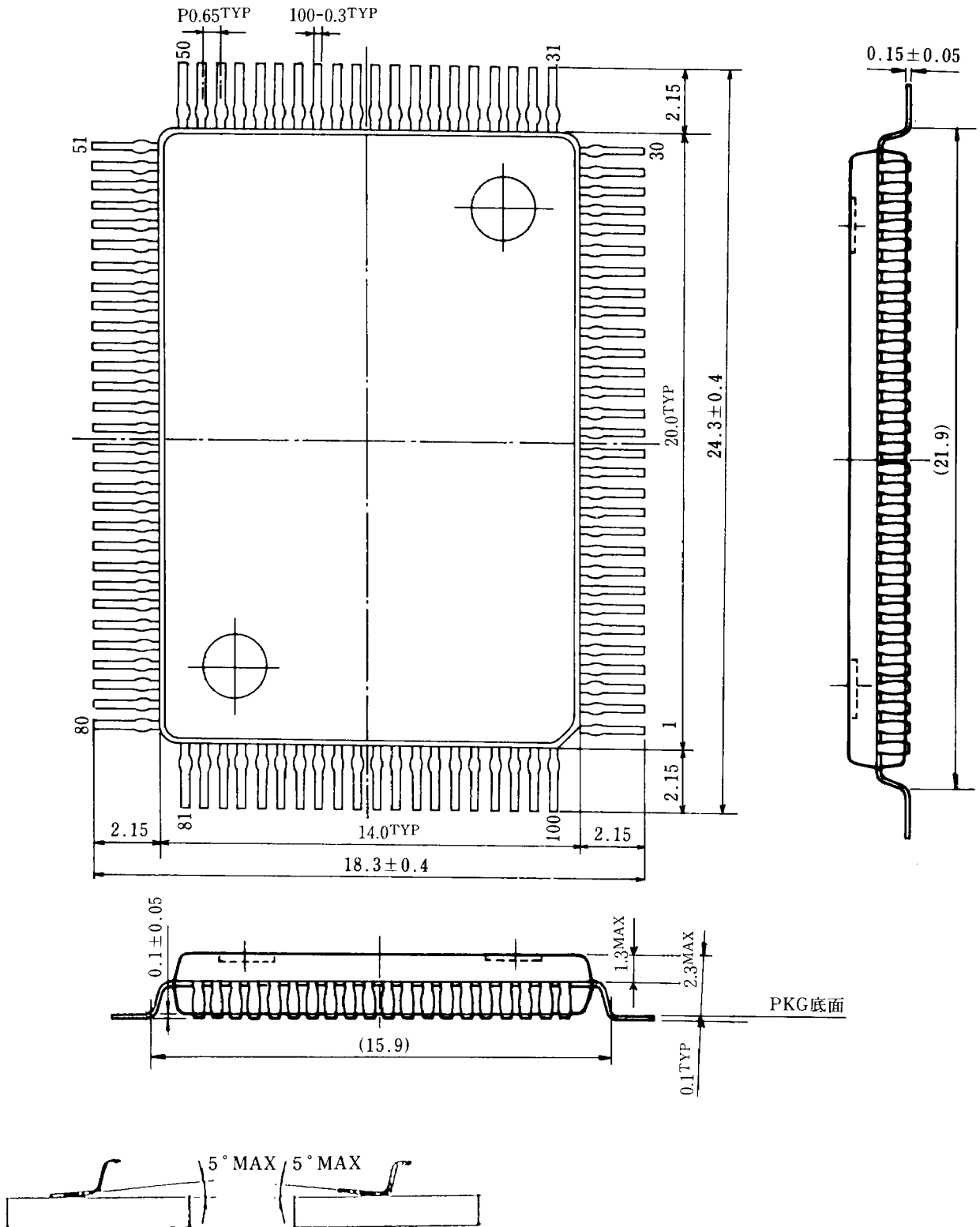
② When using LCD display (SRAM used)



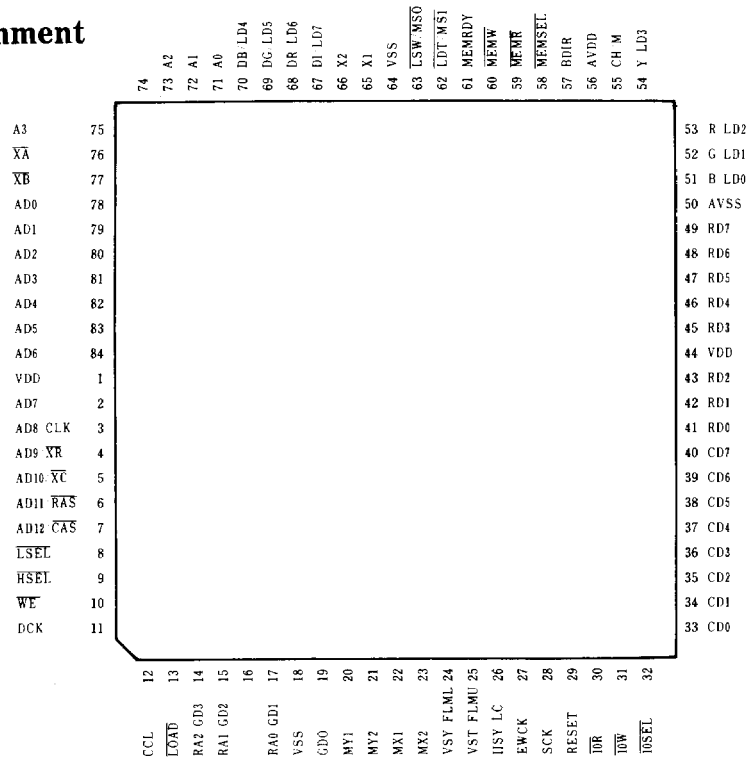


## ■ V6355D-F Package Dimensions

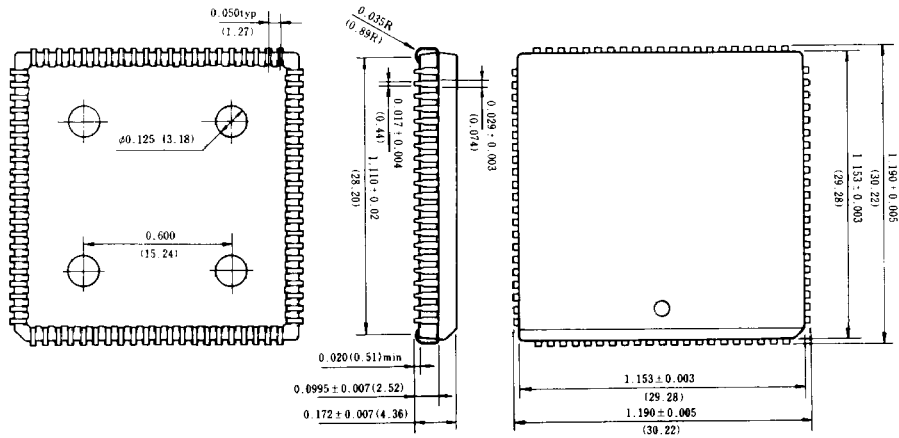
Base of package



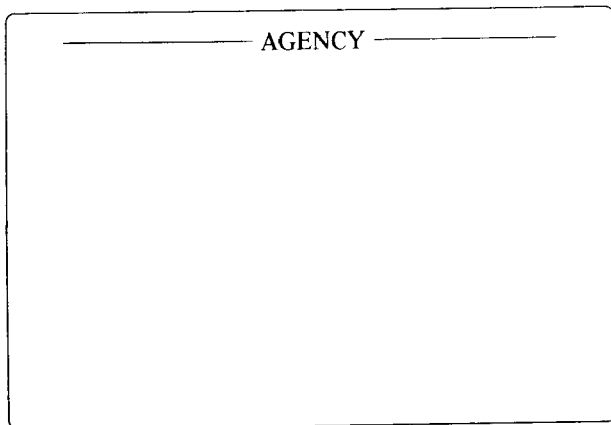
## ■ V6355D-J Pin Assignment



## ■ V6355D-J Package Dimensions



The specifications of this product are subject to improvement changes without prior notice.



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