TGX

DATA SHEET

TurboGX™ Graphics Accelerator

DESCRIPTION

The STP3010 employs over 128,000 gates and implements an extended superset of previous GX architectures. This chip provides an integral SBus interface, VRAM (video random-access memory) controller, a high-performance math engine, plus a high-performance rendering (or drawing) engine. A complete graphics accelerator can be built utilizing this chip, a clock device, VRAM, and a RAMDAC.

The STP3010 delivers an unparalleled level of integration that has allowed for its inclusion on a single-wide SBus card. These products also make multi-headed acceleration a cost-effective reality. In addition to the STP3010's enhanced functionality, it offers high-resolution, off-screen memory, and multi-buffering capabilities.

The STP3010 comes in a 223-pin ceramic pin grid array (CPGA) package.

FEATURES

- 100 percent compatibility with previous GX implementations
- Complete graphics accelerator in a single chip—just add RAM, a RAMDAC, and a clock device
- Large-scale integration in 0.6-micron custom CMOS
- Over 128,000 gates (~500,000 transistors)
- Integral high-performance rendering engine (up to 1600 Mpixels/s)
- Integral high-performance math engine (up to 100 MFLOPS)
- Integral asynchronous SBus interface (rendering and math performance independent of SBus clock rate)
- 1-Mb, 2-Mb, and 4-Mb VRAM support
- Integral high-performance VRAM controller
- New block mode support for high-speed solid fill
- Multi-vector processing capability for 2 vectors per command
- 8x16 Font FIFO
- FIFO and destination caches
- Multi-mode, multi-buffering support assuring MIT X11 compliance
- High-speed block copy for raster copies between buffers (eliminates visual anomalies, or tearing during double buffering)
- Off-screen rendering support (improves window system performance)
- Enhanced programmable timing logic with support for flicker-free 76 Hz vertical refresh rates and multi-resolution support including 1024x768, 1152x900, 1280x1024, and 1600x1280.
- Software driver for the device is included in Solaris 1.X and 2.X

BLOCK, LOGIC, AND TYPICAL APPLICATION DIAGRAMS

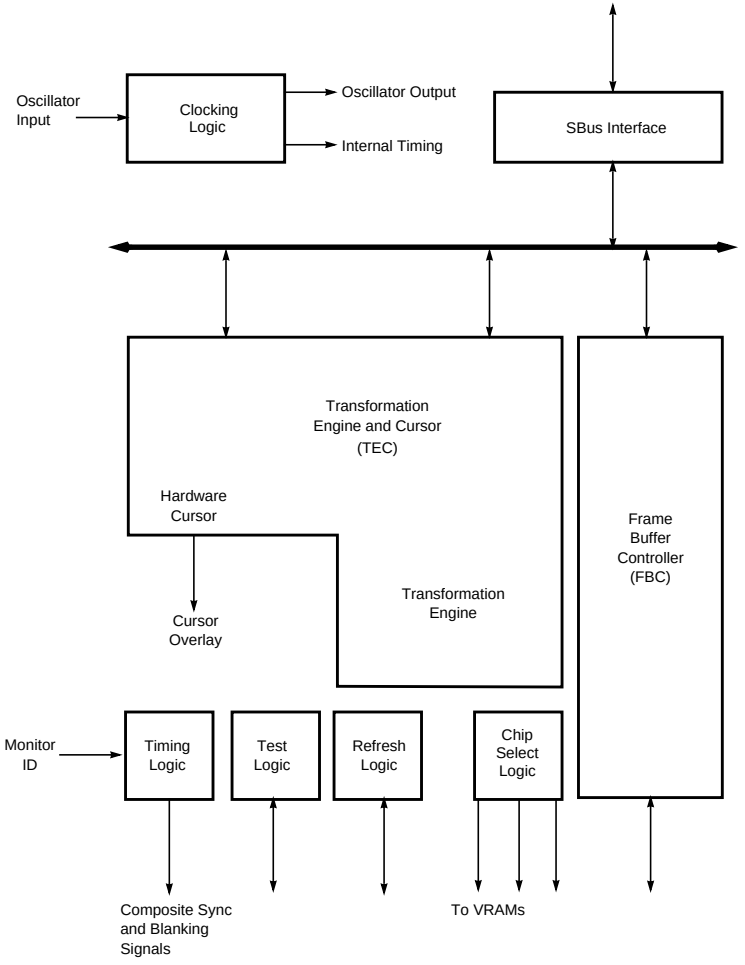


Figure 1. STP3010 Block Diagram

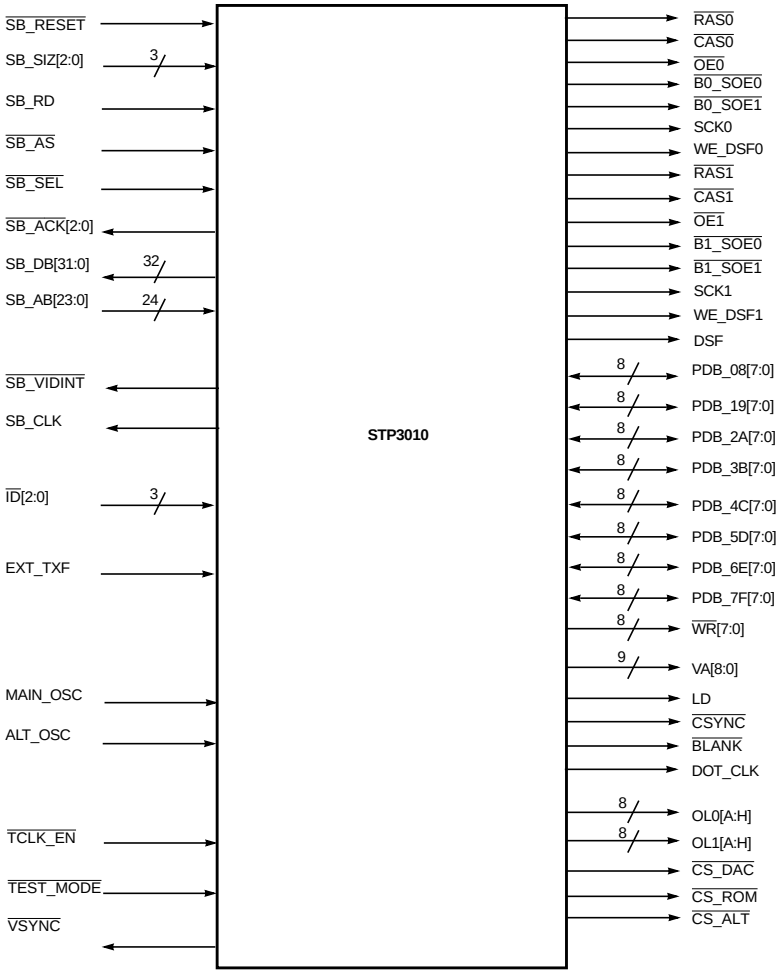


Figure 2. STP3010 Logical Connections

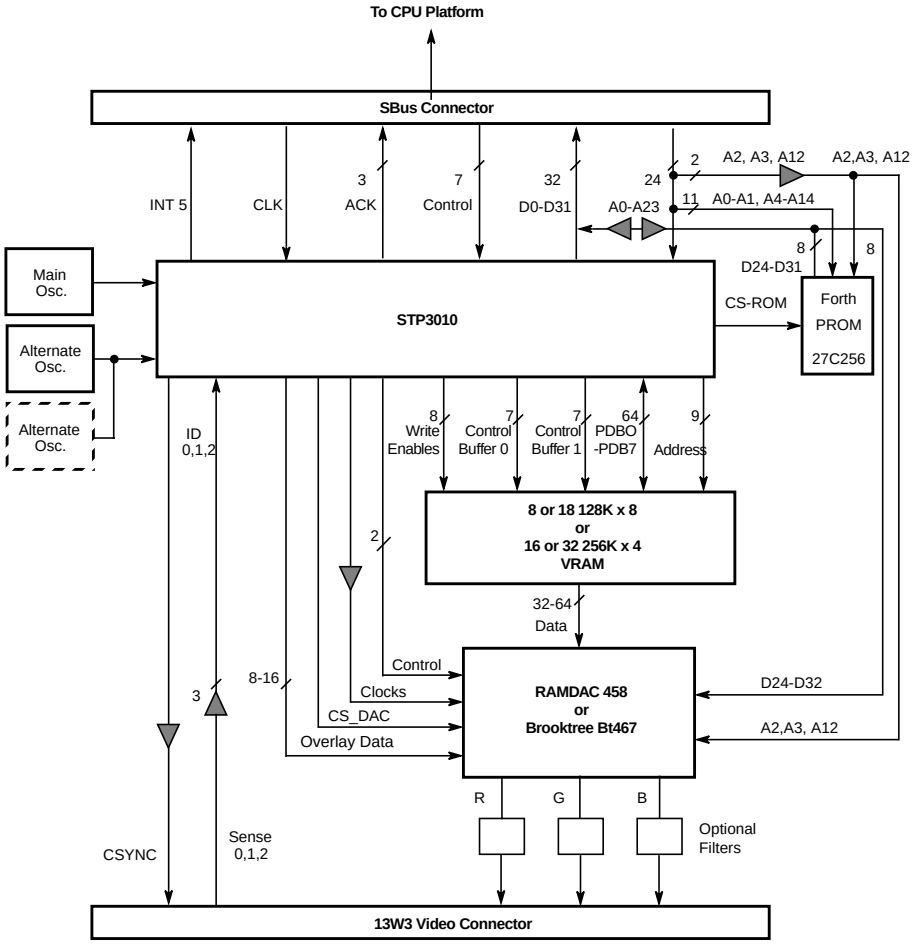


Figure 3. STP3010 Typical Applications

SIGNAL DESCRIPTIONS

SBus Interface

Signal	Type	Description
$\overline{\text{SB\_ACK}}$[2:0]	Output	SBus Transfer Acknowledge. These outputs indicate the conclusion of a STP3010 SBus transaction. These lines are normally tristate and get driven actively for only the concluding two cycles of a STP3010 SBus access.
$\overline{\text{SB\_AS}}$	Input	SB Address Strobe. This input indicates that the SBus address, data, and control signals are valid on the SBus. This pin has an internal pullup.
SB_CLK	Input	SBus Clock. This pin provides the basic timing for the STP3010's SBus interface logic. It should run in the 16-25 MHz range and should be symmetrical. This pin has Schmidt trigger TTL input and an internal pullup.
SB_DB[31:0]	Bidir	SBus Data Bus. These pins contain data being transferred between the STP3010 and the SBus. These pins have internal pullups.
$\overline{\text{SB\_IRQ5}}$	Output	SBus Interrupt for VBLANK event. This open-drain output indicates that the STP3010 is requesting an SBus interrupt to indicate that occurrence of a vertical blanking event.
SB_AB[23:0]	Input	SBus Address Bus. These pins contain the address of where data is being transferred between the STP3010 and the SBus. These pins have internal pullups.
SB_RD	Input	SBus Read. This input indicates whether a SBus access is a read (high) or write (low). This pin has an internal pullup.
$\overline{\text{SB\_RESET}}$	Input	SBus Reset. In general, this input causes the STP3010 to reset to a known state.This pin has a schmidt trigger TTL input and an internal pullup.
$\overline{\text{SB\_SEL}}$	Input	SBus Slave Select. This input indicates that the SBus is selecting the STP3010 for access. This pin has an internal pullup.
SB_SIZ[2:0]	Input	SBus Size. These inputs tell the STP3010 the size of the access being made by the SBus. These lines are only used when SB_SEL and SB_AS are active. The STP3010 will return an error if the SB_SIZ lines indicate that a BURST cycle has been requested. These pins have internal pullups.

Video Connector Interface

Signal	Type	Description
$\overline{\text{CSYNC}}$	Output	Composite Sync. This output is the combined sync signal for use by the monitor. This output is synchronous with the oscillator input (MAIN OSC or ALT_OSC) selected for video timing generation.
$\overline{\text{ID[2:0]}}$	Input	Identification. These inputs contain the monitor sense code taken from the 13W3 connector. This code shows up in the STP3010's CONFIG register within the FBC/FHC address space. These pins have internal pullups. Whenever $\overline{\text{TEST\_MODE}}$ = 0, ID[0] is used as the (uncomplemented) serial scan chain input. ID[1] is used as a high-true scan chain shift enable.

External Transfer

Signal	Type	Description
EXT_TXFR	Input	External Transfer. When enabled by the EXT_TRANSFER bit in the STP3010 STRAP register, this input indicates to the STP3010 that an external memory controller is requesting a transfer cycle. The leading (rising) edge is synchronized and fed to the memory control arbitration logic instead of the transfer signal generated by the STP3010 timing-generation logic. Transfer cycles are given the highest priority and are thus guaranteed service once memory accesses already in progress are concluded. The EXT_TXFR signal needs to be asserted for a minimum time greater than or equal to 3 internal clk periods (64.5 ns if the STP3010 is running internally at 46.48 MHz). The assertion of this signal will schedule a split read transfer cycle to start within 8 internal clock periods. Note that the STP3010 will only provide a Transfer Address of 0 in this mode. The transfer address should be multiplexed in with the VA[8:0] generated by the STP3010. This input has an internal pullup.

Clock Input

Signal	Type	Description
ALT_OSC	Input	Alternative Oscillator. This oscillator input (or binary divisions of it) can be selected to provide the basic video timing control and thus be used to generate the DOT_CLK and LD clocks and related synchronous signals. The maximum frequency of ALT_OSC is 117 MHz. This signal has a schmidt trigger TTL input with an internal pullup.
MAIN_OSC	Input	Main Oscillator. This oscillator input (or a half frequency version of it) is used to clock the core logic of the STP3010, transformation engine, and its RAS/CAS/OE memory timing. It can also be selected to provide the basic video timing control and thus be used to generate the DOT_CLK and LD clocks and related synchronous signals. The internal clocking rate can be selected to be either the same as MAIN_OSC (if THC strap[5] = 1) or one half MAIN_OSC (if THC strap[5] = 0). Since the maximum internal clock rate is 50 MHz, MAIN_OSC is restricted to be less than or equal to 100 MHz or 50 MHz depending on the state of THC strap[5]. This signal has a schmidt trigger TTL input with an internal pullup.

Test

Signal	Type	Description
TCLK_EN	Input	Test Clock Enable. This input is intended to be utilized on I/C test equipment only. It enables the SBUS_CLK input to be used as the main internal CLK source, allowing the SBus interface to be used synchronously. It also controls the selection of the output PERF_OSC. This signal has a schmidt trigger TTL input with an internal pullup.
TEST_MODE	Input	Test Mode. This input along with the SB_RESET and TCLK_EN determine which test or functional mode the STP3010 is in. For basic chip functionality, it should be tied high. This signal has a schmidt trigger input and has an internal pullup.

Frame Buffer Interface

Signal	Type	Description
B0_SOE0, B0_SOE1	Output	Bank 0 VRAM Serial Data Output Enable 0. In hardware applications with a 4-pixel wide DAC B0_SOE0 and B0_SOE1 alternate for each shift clock to multiplex 8 pixels down into the 4-pixel DAC input. In hardware applications with an 8-pixel wide DAC, B0_SOE0 and B0_SOE1 are both low continuously. Single buffered hardware.
RAS0, CAS0, OE0	Output	Bank 0 VRAM control. In single-buffered HW applications, these outputs are intended to drive the VRAM control inputs. In double buffered H/W applications, these outputs should drive just BANK 0 VRAM control inputs. Applications use only B0_SOE0 and B0_SOE1. These outputs are synchronous within the oscillator input (MAIN_OSC or ALT_OSC) selected for video timing generation.
SCK0	Output	Bank 0 serial shift clock. In single buffered H/W applications, this output is intended to drive the VRAM shift clock inputs. In double buffered H/W applications, this output should drive just BANK 0 VRAM shift clock inputs. This output is synchronous with the oscillator input (MAIN_OSC or ALT_OSC) selected for video timing generation.
WE_DSF0	Output	Bank 0 Write Enable or DSF. When the STP3010 is used in a compatibility mode (THC strap [18] = 0) with an LSC/LAF on a Duplo/Quadro configuration, this output will be always “low” so as to enable all writes through the external “OR” gates. When the STP3010 is in alternate DSF mode (THC strap [18] = 1), this pin is the STP3010's DSF output pin for driving the bank 0 VRAM DSF input pins in a one or two bank system.
B1_SOE0, B1_SOE1	Output	Bank 1 VRAM Serial Output Enable 0. This output as well as B1_SOE1 are the serial output enables for the 2nd bank in double buffer hardware applications. B1_SOE0 and B1_SOE1 alternate on each shift clock when bank 1 is being displayed. They remain high when bank 0 is displayed.
RAS1, CAS1, OE1	Output	Bank 1 VRAM control. In single buffered H/W applications, these outputs are not used. In double buffered H/W applications, these outputs should drive just BANK 1 VRAM control inputs.

Frame Buffer Interface

Signal	Type	Description
SCK1	Output	Bank 0 serial shift clock. In single buffered H/W applications, this output is not used. In double buffered H/W applications, this output should drive just BANK 1 VRAM shift clock inputs. This output is synchronous with the oscillator input (MAIN_OSC or ALT_OSC) selected for video timing generation.
VSYNC_TXD	Output	VSync_ or Transmit Data: This output is multiplexed from two internal sources based on the value of the $\overline{\text{SENSE\_EN}}$ bit in the Sense Bus Register (thc_space + 0x80). When $\overline{\text{SENSE\_EN}}$ = 1, the pin outputs VSYNC_TXD. When this signal is asserted, the TGX video is in vertical Sync. When $\overline{\text{SENSE\_EN}}$ = 0, the output is Transmit Data, driving serial data out onto the Sense Bus.
WE_DSF1	Output	Bank 1 Write Enable or DSF. When the STP3010 is used in a compatibility mode (THC strap [18] = 0), this output will be always “low” so as to enable all writes through the external “OR” gates. When the STP3010 is in alternate DSF mode (THC strap [18] = 1), this pin is the STP3010's DSF output pin for driving the bank 1 VRAM DSF input pins in a two bank system. When in a 1 bank system, this output will always be “low.”
DSF_VSYNC	Output	VSync or DSF. When the STP3010 is used in a compatibility mode (THC strap [18] = 0) with an LSC/LAF, this pin is the STP3010's DSF output for driving all bank's VRAM DSF input pins. When the STP3010 is in alternate DSF mode (THC strap [18] = 1) this pin is the STP3010's VSYNC_TXD output pin. When asserted, the STP3010 video is in vertical Sync.
$\overline{\text{WR}}$[7:0]	Output	Write Enable. These outputs are used to enable individual pixels during VRAM write cycles. All $\overline{\text{WR}}$ signals are driven low when the row address is on the address bus for loading the plane mask into the video RAMs.
PDB_xx[7:0]	Bidir	Pixel data bus. These pins are bidirectional data lines that transfer data to and from the VRAM memory. These pins have internal pullups.
VA[8:0]	Output	VRAM address. These outputs can be used to drive the multiplexed VRAM address inputs directly. The linear address bits that appear on the VA output bus is a function of the memory control operation and the type of VRAM utilized (indicated in the THC address space's STRAP register).

DAC Interface

Signal	Type	Description
$\overline{\text{BLANK}}$	Output	Blank. This output is the blanking signal for the video DACs. This output is synchronous with the oscillator input (MAIN_OSC or ALT_OSC) selected for video timing generation.
$\overline{\text{CS\_DAC}}$	Output	DAC chip select. This output is asserted low when the STP3010 detects an SBus access intended for the DAC.
DOT_CLK	Output	Video dot clock. This output can be selected via the THC address space STRAP register to reflect either the MAIN_OSC or ALT_OSC input.
LD	Output	This output is derived from the oscillator input selected to generate the DOT_CLK output. This output can be a divide-by-4 or a divide-by-8 of the DOT_CLK frequency depending on the DAC_MUX setting in the THC address space STRAP register.
OL0[A:H]	Output	Overlay planes. These outputs are for plane 0 of the hardware cursor. Groups of four planes use OL0[A:H]. Bit A is the left-most pixel. These outputs are synchronous with the oscillator input (MAIN_OSC or ALT_OSC) selected for video timing generation.

ROM Interface

Signal	Type	Description
$\overline{\text{CS\_ROM}}$	Output	ROM chip select. This output is asserted low when the STP3010 detects an SBus access intended for the DAC.

ALT Interface

Signal	Type	Description
$\overline{\text{CS\_ALT}}$	Output	Alternate chip select. This output is asserted low when the STP3010 detects an SBus access intended for an external device accessed through the alternate device address space.

ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings

Symbol	Parameter	Max	Units
V_{cc}	Power supply voltage	5.25	V

Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Max	Units
T_C	Ambient operating temperature		0	70	˚C
V_{CC}	Power supply voltage		4.75	5.25	V
I_{IN}	Input current	$0 < V_I < V_{CC}$	50	100	A
I_{CC}	Supply current		–	~300	mA

Capacitance

Output	Notes	Loading	Unit
VA[8:0]		150	pF
$\overline{\text{RASx}}$		85	pF
$\overline{\text{CASx}}$		85	pF
$\overline{\text{OEx}}$		85	pF
SCKx		85	pF
$\overline{\text{Bx\_SOEx}}$		85	pF
$\overline{\text{WR}}$[7:0]		30	pF
PDB_xx[7:0]		30	pF
WE_DSFx		85	pF
LD		25	pF
DOT_CLK		25	pF
$\overline{\text{CSYNC}}$		25	pF
$\overline{\text{BLANK}}$		25	pF
VSYNC_TXD		25	pF
DSF_VSYNC		25	pF
OLx[A:H]		25	pF
$\overline{\text{CS\_xxx}}$		25	pF
SB_DB[23:0]	R_1 = 1 KΩ	160	pF
$\overline{\text{SB\_xxxINT}}$	R_1 = 10 KΩ	160	pF
$\overline{\text{SB\_ACK}}$[2:0]	R_1 = 1 KΩ	160	pF

DC Characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
V_{OH}	LD, BLANK, CS_DAC, CS_ROM, CSYNC, OLx[A:H]	I_{OH}= –2 mA	3.0	–	V
	PDB_xx[7:0], WE_DSFx, Bx_SOEy, CS_ALT, SCKx, VSYNC_TXD	I_{OH} = –4 mA	3.0	–	V
	RASx, CASx, OEx, WR[7:0], VA[8:0], DSF_VSYNC	I_{OH} = –6 mA	3.0	–	V
	SB_DB[31:0], DOT_CLK	I_{OH} = –4 mA*	2.4	–	V
	SB_ACK[2:0]	I_{OH} = –8 mA*	2.4	–	V
V_{OL}	LD, BLANK, CS_DAC, CS_ROM, CSYNC, OLx[A:H]	I_{OL} = 2 mA	0.8	–	V
	PDB_xx[7:0], WE_DSFx, Bx_SOEy, CS_ALT, SCKx, VSYNC_TXD, SB_DB[31:0], DOT_CLK	I_{OL} = 4 mA	0.8	–	V
	RASx, CASx, OEx, WR[7:0], VA[8:0], DSF_VSYNC	I_{OL} = 6 mA	0.8	–	V
	SB_ACK[2:0]	I_{OL} = 8 mA	0.0		V
R_I	All inputs	Input pullup	50	100	KΩ
C_I	All inputs		–	12	pF

* All output pins, except SB_DB, SB_ACK, and DOT_CLK are driven with an LV-TTL driver. The intent is to draw less power and still remain TTL compatible.

AC Characteristics: SBus

Symbol	From (Input)	To (Output)	Notes	Min	Max	Unit
F_{Clock}	SB_CLK high	SB_CLK high		16.67	25	MHz
t_{CP}	SB_CLK high	SB_CLK high		40	60	ns
t_{CH}	SB_CLK high	SB_CLK low		17		ns
t_{CL}	SB_CLK low	SB_CLK high		17		ns
t_{CR}, t_{CF}	SB_CLK		Rise/fall	1	3	ns
t_{IS}	SB_SIZ, SB_RD, $\overline{\text{SB\_AS}}$, SB_SEL, SB_DB, SB_AB, $\overline{\text{SB\_RESET}}$	SB_CLK high		15		ns
t_{IH}	SB_CLK high	SB_SIZ, SB_RD, $\overline{\text{SB\_AS}}$, SB_SEL, SB_DB, SB_AB, $\overline{\text{SB\_RESET}}$		–	0	ns
t_F	$\overline{\text{SB\_xxxINT}}$		Fall	5	20	ns
t_{IR}	$\overline{\text{SB\_xxxINT}}$		Rise	5	1200	ns
t_R, t_F	SB_ACK, SB_DB		Rise/fall	5	20	ns
t_{OD25}	SB_CLK high	SB_DB, $\overline{\text{SB\_ACK}}$ valid		2.5	20	ns
t_{OH}	SB_CLK high	SB_DB, $\overline{\text{SB\_ACK}}$ hold		2.5		ns
t_Z	SB_CLK high	SB_DB, $\overline{\text{SB\_ACK}}$ tri-state			35	ns
t_{13}	SB_CLK high	$\overline{\text{CS\_ROM}}$, $\overline{\text{CS\_DAC}}$, $\overline{\text{CS\_ALT}}$ valid		0	20	ns

Notes:

1) There are no timing requirements for asserting $\overline{\text{SB\_RESET}}$. It must remain asserted for at least 512 SB_CLK cycles. It must then meet the specified setup and hold times for unassertion.

2) $\overline{\text{SB\_VIDINT}}$ is totally asynchronous from SB_CLK. It may be asserted and unasserted without regard for setup and hold times with respect to SB_CLK. Once asserted, it must remain asserted until cleared by the CPU.

Memory Control: Common Timing

Symbol	Output		Notes	Min	Max	Unit
	From	To				
t_T	Any high/low	Any low/high	Transition	3		ns
t_{RP}	$\overline{RAS}$x high	$\overline{RAS}$x low	High PW	80		ns
t_{CP}	$\overline{CAS}$x high	$\overline{CAS}$x low	High PW	20		ns
t_{RAS}	$\overline{RAS}$x low	$\overline{RAS}$x high	Low PW	100		ns
t_{CAS}	$\overline{CAS}$x low	$\overline{CAS}$x high	Low PW	30		ns
t_{ASR}	VA[8:0] valid	$\overline{RAS}$x falling	Setup	1		ns
t_{RAH}	$\overline{RAS}$x low	VA[8:0] invalid	Hold	15		ns
t_{ASC}	VA[8:0]	$\overline{CAS}$x falling	Setup	1		ns
tCAH	$\overline{CAS}$x low	VA[8:0] invalid	Hold	20		ns
tCSH	$\overline{RAS}$x low	$\overline{CAS}$x high	$\overline{CAS}$ hold	100		ns

Memory Control: Write Timing

Symbol	Output		Notes	Min	Max	Unit
	From	To				
t_{WP}	$\overline{WR}$[7:0] low	$\overline{WR}$[7:0] high	Low PW	20		ns
t_{CWL}	$\overline{WR}$[7:0] low	$\overline{CAS}$x high		30		ns
t_{RWL}	$\overline{WR}$[7:0] low	$\overline{RAS}$x high		30		ns
t_{DS}	PDBxx[7:0] valid	$\overline{WR}$[7:0] low	Data setup	1		ns
t_{DH}	$\overline{WR}$[7:0] low	PDBx[7:0]	Data hold	25		ns
t_{MS}	PDBxx[7:0] valid	$\overline{RAS}$x low	Setup	1		ns
t_{MH}	$\overline{RAS}$x low	PDBxx[7:0] invalid	Hold	15		ns

Memory Control: Read Timing

Symbol	Output		Notes	Min	Max	Unit
	From	To				
t_{RAC}	$\overline{RAS}$x falling	PDBxx[7:0] valid	$\overline{RAS}$ access		100	ns
t_{CAC}	$\overline{CAS}$x falling	PDBxx[7:0] valid	$\overline{CAS}$ access		30	ns
t_{OEA}	$\overline{OE}$x falling	PDBxx[7:0] valid	$\overline{OE}$ access		30	ns
t_{AA}	VAx valid	PDBxx[7:0] valid	Address access		55	ns

Video-Related Output Characteristics

Symbol	Output		Notes	Min	Max	Unit
	From	To				
t_{SC}	SCKx high	SCKx high		35		ns
t_{SL}	SCKx high	$\overline{OEx}$ high		10		ns
t_{SD}	$\overline{OEx}$ high	SCKx high		15		ns

Miscellaneous

Symbol	Input		Notes	Min	Max	Unit
	From	To				
f_2	MAIN_OSC	MAIN_OSC	5		106	MHz
f_3	ALT_OSC	ALT_OSC	5		117	MHz
t_{PWL}	MAIN_OSC falling	MAIN_OSC rising		3		ns
t_{PWH}	MAIN_OSC rising	MAIN_OSC falling		3		ns
t_{PWL}	ALT_OSC falling	ALT_OSC rising		3		ns
t_{PWH}	ALT_OSC rising	ALT_OSC falling		3		ns

Notes:

1) The PDB input setup time needs to be measured against the internal signals' DACK0 and DACK1 falling edges. Buffered versions of these signals latch the PDB bus into latches in SLAVEROP and MASTEROP submodules of the OCTAPIN module. Externally, all that can be specified is a maximum prop delay from $\overline{RAS}$, VA, $\overline{CAS}$, $\overline{OE}$ that the chip needs to reliably accept data. $t_{PSU0,1}$ are the setup times from the PDB valid at the pins to DACK0,1 falling inside the chip.
The following equations must be satisfied:

$t_{RDAC} > t_{RAC} + t_{PSU0}$
$t_{CD} > t_{CAC} + tP_{SU0,1}$
$t_{OD} > t_{OEA} + t_{PSU0,1}$

2) Memory specs assume 100-ns VRAMs and a 43-ns CLK_43 (clk1x). Specs assuming 80-ns VRAMs and a 37.9-ns CLK_43 (CLK1x) will be forthcoming.

3) Nominal 50% duty cycle expected.

TIMING DIAGRAMS

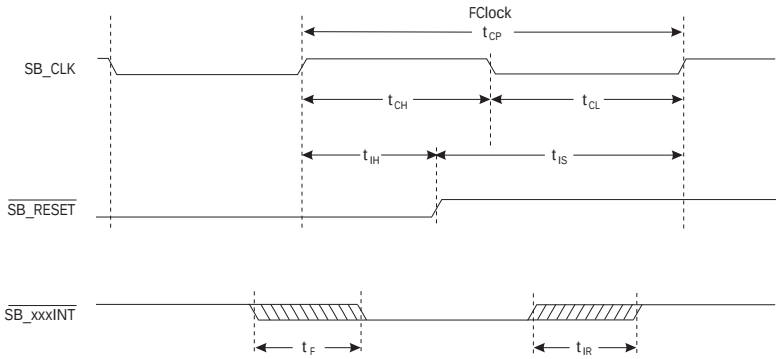


Figure 4. SBus Miscellaneous Signals

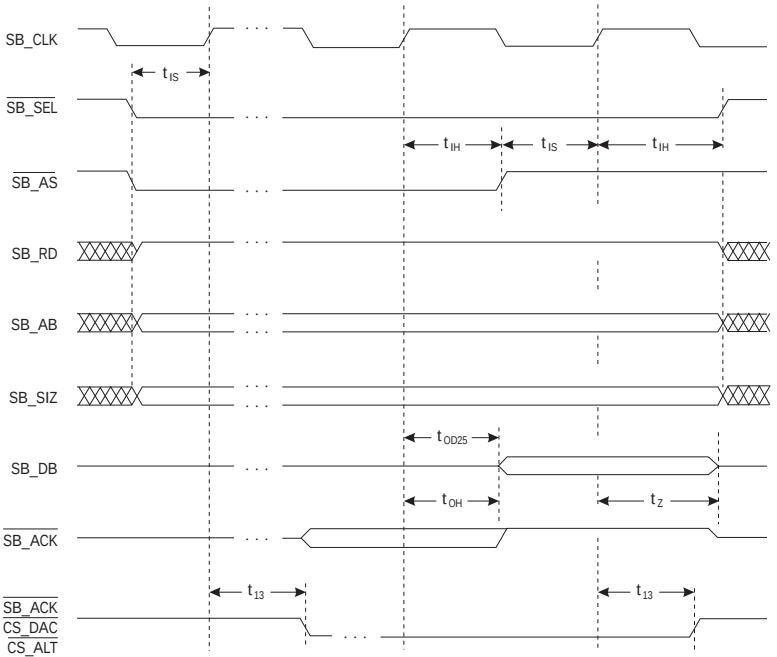


Figure 5. SBus Read Cycle

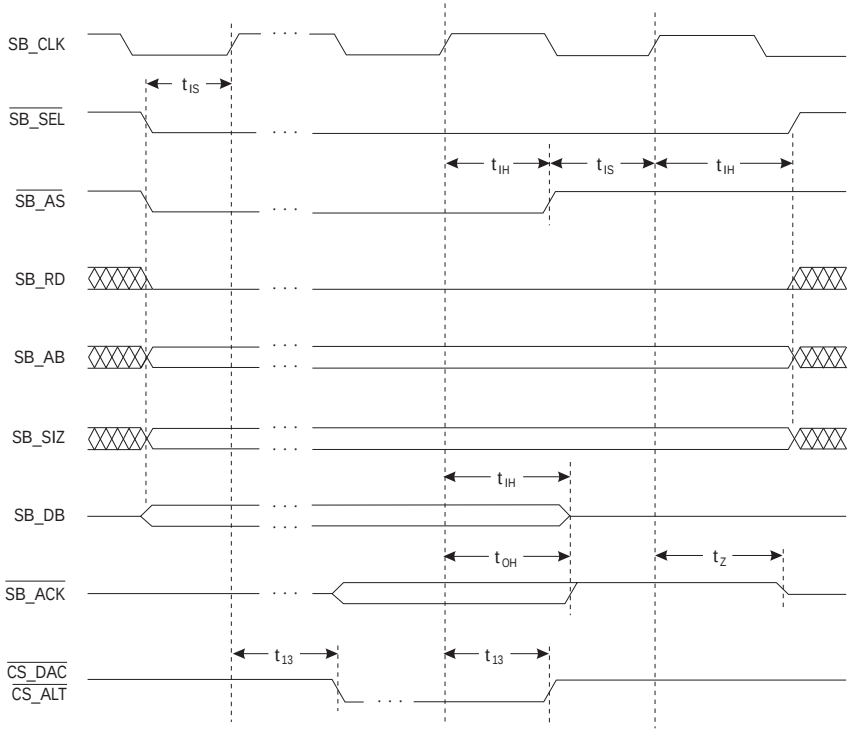


Figure 6. SBus Write Cycle

PACKAGE INFORMATION

223-Pin Ceramic Pin Grid Array (CPGA) Pin Assignments

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
A2	V_{CC}	C12	SB_DB10	G16	PDB_7F3	N4	SCK1	T16	PDB_3B2
A3	SB_AB4	C13	SB_DB6	G17	PDB_6E5	N15	PDB_4C4	T17	PDB_3B4
A4	SB_AB0	C14	SB_DB4	G18	PDB_6E3	N16	PDB_4C6	T18	PDB_3B5
A5	SB_SIZ1	C15	$\overline{SB\_AS}$	H1	GND	N17	PDB_4C5	U1	V_{CC}
A6	SB_DB29	C16	VA7	H2	SB_AB23	N18	PDB_4C7	U2	GND
A7	SB_DB25	C17	VA6	H3	MAIN_OSC	P1	$\overline{CSYNC}$	U3	OL0A
A8	GND	C18	VA5	H4	SB_AB20	P2	SCK0	U4	OL0D
A9	V_{CC}	D1	$\overline{CAS1}$	H15	PDB_7F1	P3	WE_DSF1	U5	OL0G
A10	GND	D2	$\overline{OE1}$	H16	$\overline{WR7}$	P4	$\overline{CAS0}$	U6	OL1B
A11	SB_DB19	D3	SB_AB11	H17	PDB_6E2	P15	PDB_3B7	U7	OL1F
A12	SB_DB15	D4	SB_AB7	H18	PDB_6E1	P16	PDB_4C1	U8	PDB_080
A13	SB_DB11	D5	SB_AB3	J1	V_{CC}	P17	PDB_4C2	U9	PDB_082
A14	SB_DB7	D6	SB_RD	J2	$\overline{SB\_RESET}$	P18	PDB_4C3	U10	PDB_084
A15	SB_DB2	D7	SB_SIZ0	J3	DOT_CLK	R1	VSYNC_TXD	U11	PDB_087
A16	SBUS_CLK	D8	SB_DB28	J4	ALT_OSC	R2	WE_DSF0	U12	PDB_191
A17	V_{CC}	D9	SB_DB24	J15	PDB_6E6	R3	$\overline{RAS0}$	U13	PDB_195
A18	GND	D10	SB_DB16	J16	PDB_6E4	R4	$\overline{ID2}$	U14	PDB_2A0
B1	V_{CC}	D11	SB_DB12	J17	$\overline{WR6}$	R5	OL0B	U15	PDB_2A6
B2	GND	D12	SB_DB8	J18	V_{CC}	R6	OL1A	U16	PDB_3B1
B3	SB_AB5	D13	SB_DB3	K1	GND	R7	OL1E	U17	V_{CC}
B4	SB_AB1	D14	SB_DB0	K2	EXT_TXFR	R8	$\overline{WR0}$	U18	GND
B5	$\overline{SB\_IRQ5}$	D15	VA8	K3	$\overline{SB\_ACK0}$	R9	PDB_083	V1	GND
B6	SB_DB31	D16	VA3	K4	$\overline{SB\_ACK2}$	R10	PDB_192	V2	V_{CC}
B7	SB_DB27	D17	VA2	K15	PDB_5D7	R11	PDB_196	V3	$\overline{TEST\_MODE}$
B8	SB_DB23	D18	VA1	K16	PDB_6E0	R12	PDB_2A1	V4	OL0E
B9	SB_DB21	E1	SB_AB15	K17	PDB_5D6	R13	PDB_2A4	V5	OL0H
B10	SB_DB20	E2	SB_AB13	K18	GND	R14	$\overline{WR3}$	V6	OL1D
B11	SB_DB17	E3	SB_AB12	L1	DSF_VSYNC	R15	PDB_3B3	V7	OL1H
B12	SB_DB13	E4	SB_AB10	L2	$\overline{SB\_ACK1}$	R16	PDB_3B6	V8	GND
B13	SB_DB9	E15	VA4	L3	$\overline{CS\_ROM}$	R17	$\overline{WR4}$	V9	V_{CC}
B14	SB_DB5	E16	PDB_7F6	L4	$\overline{CS\_ALT}$	R18	PDB_4C0	V10	GND
B15	SB_DB1	E17	PDB_7F4	L15	PDB_5D3	T1	$\overline{OE0}$	V11	PDB_086
B16	$\overline{SB\_SEL}$	E18	PDB_7F2	L16	PDB_5D5	T2	$\overline{ID0}$	V12	$\overline{WR1}$
B17	GND	F1	SB_AB19	L17	PDB_5D4	T3	$\overline{ID1}$	V13	PDB_193
B18	V_{CC}	F2	SB_AB17	L18	V_{CC}	T4	OL0C	V14	PDB_197
C1	SB_AB9	F3	SB_AB14	M1	$\overline{B1\_SOE0}$	T5	OL0F	V15	PDB_2A5
C2	SB_AB8	F4	$\overline{RAS1}$	M2	$\overline{B1\_SOE1}$	T6	OL1C	V16	PDB_3B0
C3	SB_AB6	F15	VA0	M3	LD	T7	OL1G	V17	GND
C4	SB_AB2	F16	PDB_7F7	M4	$\overline{CS\_DAC}$	T8	PDB_081	V18	V_{CC}
C5	$\overline{TCLK\_EN}$	F17	PDB_7F0	M15	$\overline{WR5}$	T9	PDB_085		
C6	SB_SIZ2	F18	PDB_6E7	M16	PDB_5D1	T10	PDB_190		
C7	SB_DB30	G1	SB_AB22	M17	PDB_5D0	T11	PDB_194		
C8	SB_DB26	G2	SB_AB21	M18	PDB_5D2	T12	$\overline{WR2}$		
C9	SB_DB22	G3	SB_AB18	N1	$\overline{B0\_SOE0}$	T13	PDB_2A3		
C10	SB_DB18	G4	SB_AB16	N2	$\overline{B0\_SOE1}$	T14	PDB_2A2		
C11	SB_DB14	G15	PDB_7F5	N3	$\overline{BLANK}$	T15	PDB_2A7		

Pinout Information

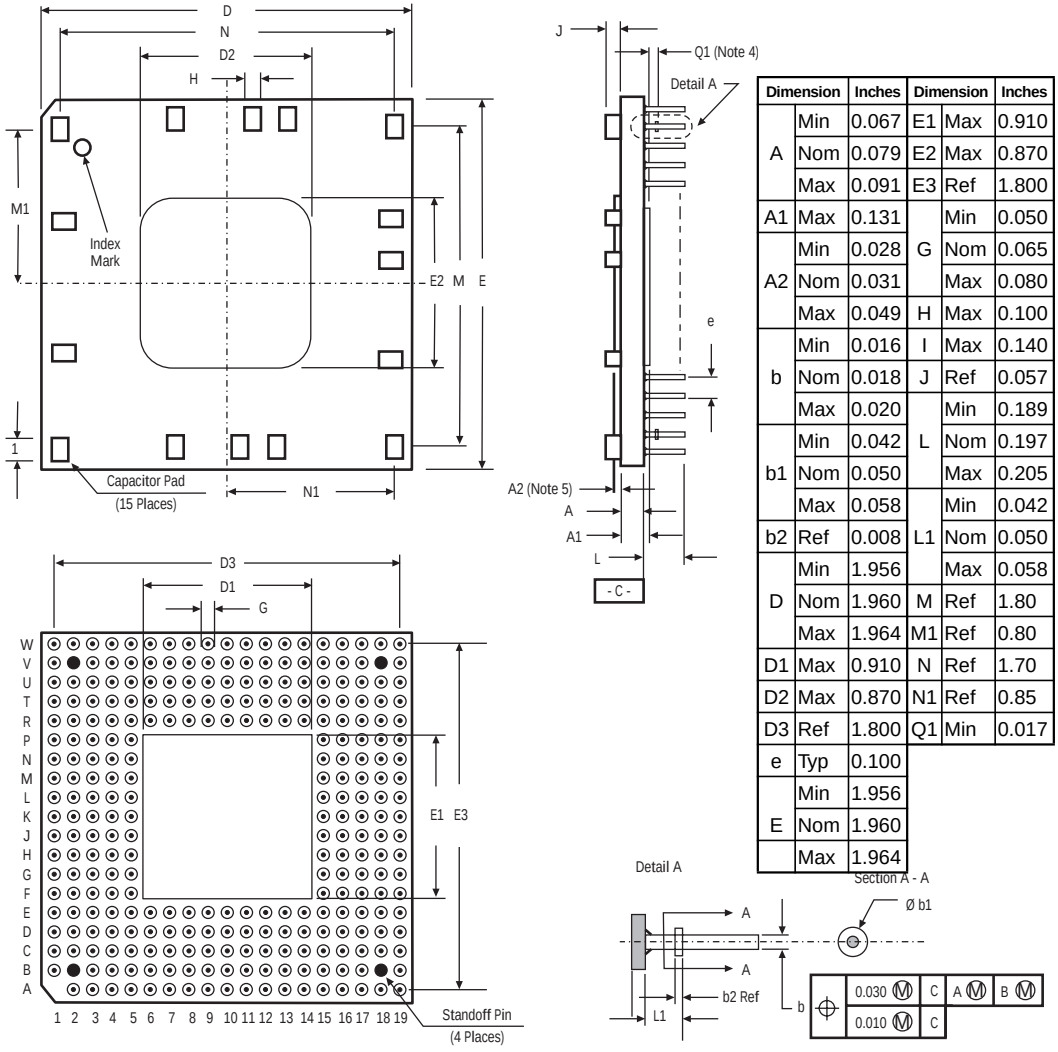
Figure 7 shows the STP3010 pinout. Note that there is no pin 1 on the STP3010; it is intentionally omitted to eliminate any possibility of misalignment.

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18
A		V_{CC}	SB_AB4	SB_AB0	SB_SIZ1	SB_DB29	SB_DB25	GND	V_{CC}	GND	SB_DB19	SB_DB15	SB_DB11	SB_DB7	SB_DB2	SBUS_CLK	V_{CC}	GND
B	V_{CC}	GND	SB_AB5	SB_AB1	$\overline{SB\_IRQ5}$	SB_DB31	SB_DB27	SB_DB23	SB_DB21	SB_DB20	SB_DB17	SB_DB13	SB_DB9	SB_DB5	SB_DB1	$\overline{SB\_SEL}$	GND	V_{CC}
C	SB_AB9	SB_AB8	SB_AB6	SB_AB2	$\overline{TCLK\_EN}$	SB_SIZ2	SB_DB30	SB_DB26	SB_DB22	SB_DB18	SB_DB14	SB_DB10	SB_DB6	SB_DB4	$\overline{SB\_AS}$	VA7	VA6	VA5
D	$\overline{CAS1}$	$\overline{OE1}$	SB_AB11	SB_AB7	SB_AB3	SB_RD	SB_SIZ0	SB_DB28	SB_DB24	SB_DB16	SB_DB12	SB_DB8	SB_DB3	SB_DB0	VA8	VA3	VA2	VA1
E	SB_AB15	SB_AB13	SB_AB12	SB_AB10											VA4	PDB_7F6	PDB_7F4	PDB_7F2
F	SB_AB19	SB_AB17	SB_AB14	$\overline{RAS1}$											VA0	PDB_7F7	PDB_7F0	PDB_6E7
G	SB_AB22	SB_AB21	SB_AB18	SB_AB16											PDB_7F5	PDB_7F3	PDB_6E5	PDB_6E3
H	GND	SB_AB23	MAIN_OSC	SB_AB20											PDB_7F1	$\overline{WR7}$	PDB_6E2	PDB_6E1
J	V_{CC}	$\overline{SB\_RESET}$	DOT_CLK	ALT_OSC											PDB_6E6	PDB_6E4	$\overline{WR6}$	V_{CC}
K	GND	EXT_TXFR	$\overline{SB\_ACK0}$	$\overline{SB\_ACK2}$											PDB_5D7	PDB_6E0	PDB_5D6	GND
L	DSF_VSYNC	$\overline{SB\_ACK1}$	$\overline{CS\_ROM}$	$\overline{CS\_ALT}$											PDB_5D3	PDB_5D5	PDB_5D4	V_{CC}
M	$\overline{B1\_SOE0}$	$\overline{B1\_SOE1}$	LD	$\overline{CS\_DAC}$											$\overline{WR5}$	PDB_5D1	PDB_5D0	PDB_5D2
N	$\overline{B0\_SOE0}$	$\overline{B0\_SOE1}$	$\overline{BLANK}$	SCK1											PDB_4C4	PDB_4C6	PDB_4C5	PDB_4C7
P	$\overline{CSYNC}$	SCK0	WE_DSF1	$\overline{CAS0}$											PDB_3B7	PDB_4C1	PDB_4C2	PDB_4C3
R	VSYNC_TXD	WE_DSF0	$\overline{RAS0}$	$\overline{ID2}$	OL0B	OL1A	OL1E	$\overline{WR0}$	PDB_083	PDB_192	PDB_196	PDB_2A1	PDB_2A4	$\overline{WR3}$	PDB_3B3	PDB_3B6	$\overline{WR4}$	PDB_4C0
T	$\overline{OE0}$	$\overline{ID0}$	$\overline{ID1}$	OL0C	OL0F	OL1C	OL1G	PDB_081	PDB_085	PDB_190	PDB_194	$\overline{WR2}$	PDB_2A3	PDB_2A2	PDB_2A7	PDB_3B2	PDB_3B4	PDB_3B5
U	V_{CC}	GND	OL0A	OL0D	OL0G	OL1B	OL1F	PDB_080	PDB_082	PDB_084	PDB_087	PDB_191	PDB_195	PDB_2A0	PDB_2A6	PDB_3B1	V_{CC}	GND
V	GND	V_{CC}	$\overline{TEST\_MODE}$	OL0E	OL0H	OL1D	OL1H	GND	V_{CC}	GND	PDB_086	$\overline{WR1}$	PDB_193	PDB_197	PDB_2A5	PDB_3B0	GND	V_{CC}

Top View

Figure 7. STP3010 Pinout

223-Lead CPGA Package Dimensions



Dimension		Inches	Dimension		Inches
A	Min	0.067	E1	Max	0.910
	Nom	0.079	E2	Max	0.870
	Max	0.091	E3	Ref	1.800
A1	Max	0.131	G	Min	0.050
A2	Min	0.028		Nom	0.065
	Nom	0.031		Max	0.080
	Max	0.049	H	Max	0.100
b	Min	0.016	I	Max	0.140
	Nom	0.018	J	Ref	0.057
	Max	0.020	L	Min	0.189
b1	Min	0.042		Nom	0.197
	Nom	0.050		Max	0.205
	Max	0.058	L1	Min	0.042
b2	Ref	0.008		Nom	0.050
D	Min	1.956		Max	0.058
	Nom	1.960	M	Ref	1.80
	Max	1.964	M1	Ref	0.80
D1	Max	0.910	N	Ref	1.70
D2	Max	0.870	N1	Ref	0.85
D3	Ref	1.800	Q1	Min	0.017
e	Typ	0.100			
E	Min	1.956			
	Nom	1.960			
	Max	1.964			

Note:
1. Drawing is not to scale.
2. Size of array is 19 x 19. Corner detail and index mark are options.
3. Total number of pins is 279.
4. Envelope for maximum lid.
5. Envelope for integral heat slug.

ORDERING INFORMATION

Part Number	Description
STP3010PGA	223-Pin Ceramic Pin Grid Array (CPGA)

Document Part Number: STP3010